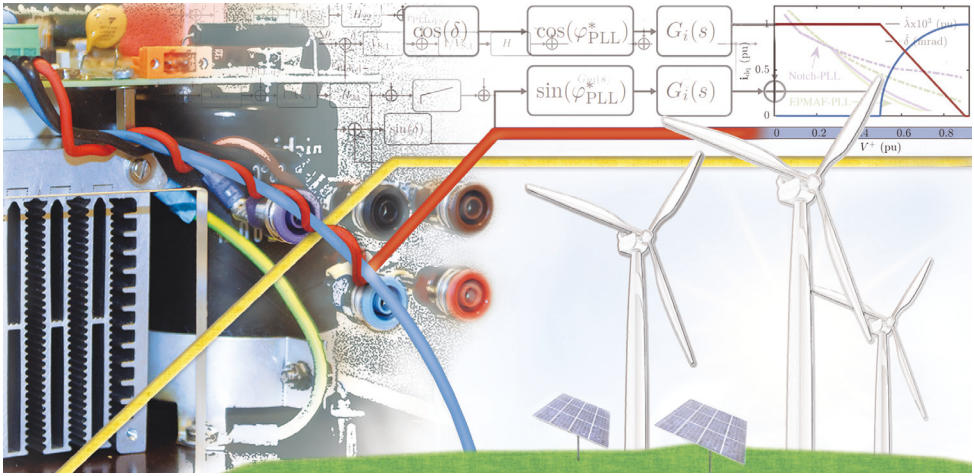
Elektrische Energietechnik an der TU Berlin Band 12

Hendrik Just

Modeling and control of power converters in weak and unbalanced electric grids



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Modeling and control of power converters in weak and unbalanced electric grids

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Abstract

Grid converters increasingly affect power system operation due to the increasing share of renewable energy sources and less conventional power plants with synchronous machines connected to the grid. This shift in power generation leads to converter-dominated weak grids, which show critical stability phenomena but also enable converters to contribute to grid stability and voltage support actively. The interaction between converters and the power system is predominantly affected by the converter control, which must handle even severe operational scenarios such as unbalanced faults that require sophisticated control schemes and modeling techniques.

Grid-following and grid-forming converter controls have attracted much attention in previous research, and various sophisticated control schemes for grid converters have been developed. However, these control schemes are mainly analyzed and designed with small-signal models showing insufficient accuracy for severe transient processes such as unbalanced grid faults. Accordingly, large-signal dynamics and transient stability phenomena of grid converters are rarely addressed in the literature. In order to assess transient stability, recent research started to analyze simplified mature converter controls in weak grids that may not sufficiently represent real systems with state-of-the-art controllers. Consequently, this thesis focuses on modeling and control of grid converters in weak grids and during unbalanced faults considering large-signal dynamics and transient stability of sophisticated control schemes. The main objectives are: (i) identify critical operational scenarios and interactions of converters with the electric grid; (ii) improve the control structures and their design; (iii) develop analysis techniques to assess large-signal dynamics and transient stability.

The Phase-Locked Loop (PLL) is identified as critical controller part of grid-following controls that predominantly affects converter control performance and stability during grid faults. In order to predict the fault dynamics, a model is derived that describes the coupling of PLLs with the converter current control. Based on this model, it is proved that conventional worst-case scenarios are not representing the worst-case for converter controls, and thus they are redefined in this thesis. Then, the control requirements are extracted from the grid codes, and an extended design process based on small-signal models is proposed. This process shows improved control performance in comparison to the conventional designs but also reveals that some PLLs with prefilter are prone to transient instability. For these PLLs,

a multi-fidelity design process using large-signal and small-signal models is proposed, which identifies empirically the unstable design space that cannot be predicted by the small-signal model. To assess the transient stability analytically, a PLL with prefilter is analyzed with Lyapunov's direct method, and an analytical stability criterion for the design parameters is derived. Based on Lassalle's invariance principle, a Lyapunov function is proposed to determine the stable state-space region for grid-following converters in weak grids, which indicates that particularly weak inductive grids are prone to instability of the converter control during grid voltage transients.
The most severe grid voltage transients occur during faults that require dual sequence current control to achieve different objectives such as rejecting active power oscillation or supporting the grid voltage. The dominant indicators for these objectives are derived, and a current reference generator is proposed that achieves satisfactory results for realizing both objectives simultaneously. The current reference generator is combined with a current and voltage limitation that shows improved dynamics without suffering from distortions in the steady-state and conserves the control objective during unbalanced grid faults. Current reference generators have a large impact on the stability, so the minimum short-circuit ratio is determined for which the system is stable, indicating that grid-following controls can be used in weak grids while showing insufficient stability for very weak grids.
Grid-forming controls enable converters to operate stably in very weak grids, and they can also achieve control objectives during unbalanced faults regarding power oscillations and grid voltage support. Accordingly, a voltage reference generator for the negative sequence of the droop control is proposed that rejects the active power oscillations. The control performance is compared with a voltage support scheme to show the trade-off between rejecting active power oscillations and supporting grid voltages.
These results and findings are experimentally validated with three different test benches introduced in this thesis.

Based on the findings, the main conclusions of this research are: First, converters must be evaluated in different worst-case operational scenarios than conventional generation units. Second, PLLs should be designed considering the current control by taking into account critical transient stability phenomena in weak grids and during severe grid faults. Therefore, nonlinear analysis techniques are crucial to assess large-signal dynamics and transient stability. Third, grid-following controls can only be used to a minimum short-circuit ratio that is affected by the converter control scheme and its design. Fourth, grid-forming controls can be stable even in very weak grids and are also able to provide comprehensive grid services during unbalanced faults. Consequently, converter-dominated grids in the current state should rely on both grid-following and grid-forming converters to safely operate during weak and stiff grid conditions.

Kurzfassung

Der steigende Anteil an erneuerbaren Energien in den Energieversorgungsnetzen führt zu der Verdrängung konventioneller Kraftwerke basierend auf Synchrongeneratoren, die direkt mit dem Netz verbunden sind. Diese Entwicklung lässt umrichterdominierte und schwache Netzabschnitte entstehen, die kritischen Stabilitätsmechanismen unterliegen, allerdings auch ermöglichen, dass Umrichter aktiv zur Netzstützung und Netzstabilität beitragen können. Vor allem die Umrichterregelung hat einen signifikanten Einfluss auf die Wechselwirkung mit dem Netz und muss den sicheren Betrieb jederzeit gewährleisten, was vor allem in schwachen Netzen und während unsymmetrischer Netzfehler eine Herausforderung darstellt.
Die aktuelle Forschung im Bereich Netzumrichterregelung arbeitet an der Weiterentwicklung von netzfolgenden und netzbildenden Regelungsstrukturen. Meistens werden diese Regelungen mit Kleinsignal-Modellen analysiert und ausgelegt, die vor allem bei kritischen Netzfehlern keine hinreichende Genauigkeit erzielen. Das Großsignalverhalten wird meistens nicht in die Auslegung der Regelung mit einbezogen und die Untersuchung der transienten Stabilität nur exemplarisch mit Zeitbereichssimulationen durchgeführt. Es existieren erste Untersuchungen der transienten Stabilität von Umrichtern in schwachen Netzen. Diese basieren allerdings auf vereinfachten Regelungsstrukturen, die für reale Systeme nur unzureichend anwendbar sind. Um die genannten Lücken zu schließen, beschreibt die vorliegende Arbeit die Modellierung und Regelung von Netzumrichtern in schwachen Netzen und während unsymmetrischer Netzfehler unter Einbeziehung des Großsignalverhaltens und moderner Regelungsstrukturen. Die Hauptziele dieser Arbeit sind: (i) Identifizierung kritischer Betriebsszenarien bei der Interaktion von Umrichtern mit dem Netz; (ii) Weiterentwicklung der Regelungsstrukturen mit zugehörigen Auslegungskriterien; (ii) Erforschung von Analysemethoden zur Bewertung des Großsignalverhaltens und der transienten Stabilität.
In dieser Arbeit wird die Phase-Locked Loop (PLL) als elementare Regelungskomponente identifiziert, die die netzfolgende Umrichterregelung vor allem während Netzfehlern signifikant beeinflusst. Um dieses Verhalten beschreiben zu können, wird ein Simulationsmodell vorgestellt, welches die Kopplung zwischen Stromregelung und PLL beschreibt. Dieses Modell zeigt, dass die konventionellen Worst-Case Betriebsszenarien im Netz nicht für Umrichter gültig sind und angepasst werden müssen. Basierend auf dem Modell und den angepassten Betriebsszenarien, werden die Netzanforderungen für Umrichter aus den Netznormen diskutiert

und eine Reglerauslegung basierend auf Kleinsignalmodellen vorgestellt. Die vorgeschlagene Auslegung führt zu einem schnelleren Ausregelvorgang als konventionelle Auslegungsansätze. Allerdings sind einige PLLs mit Vorfilter während kritischer Netzfehler instabil, da das Kleinsignalmodell für diese nur unzureichend genau ist. Aus diesem Grund wird ein Multi-fidelity Auslegungsprozess vorgestellt. Dieser basiert auf Kleinsignal- und Großsignalmodellen, wobei das Großsignalmodell empirisch die Auslegungsparameter identifiziert, die zur transienten Instabilität führen. Um die transiente Stabilität analytisch zu untersuchen, werden die PLLs mit Lyapunov's Direct Method analysiert. Dies führt zu einem analytischen Stabilitätskriterium für PLLs mit Vorfilter. Darauf aufbauend wird mit Hilfe Lasalle's Invariance Principle eine Lyapunov-Funktion berechnet, die für netzfolgenden Umrichter in schwachen Netzen die stabile Region im Zustandsraum ermittelt. Diese Untersuchung zeigt, dass vor allem Umrichter in schwachen, induktiven Netzen durch transiente Vorgänge in den Netzspannungen instabil werden können.

Netzfehler führen zu den kritischsten transienten Vorgängen. Vor allem unsymmetrische Netzfehler setzen voraus, dass der Umrichter zuverlässig den Mit- und Gegensystemstrom regeln kann. Aus diesem Grund wird eine Regelung vorgestellt, die den Strom in beiden Systemen regelt und zusätzlich bei Netzfehlern Wirkleistungsoszillationen minimiert oder die Netzspannung stützt. Dazu werden Stromsollwertberechnungen präsentiert, um diese Regelungsziele zu erreichen. Diese werden mit einer Strom- und Spannungsbegrenzung kombiniert, die die Unterdrückung der Leistungsoszillationen nicht verhindert und das dynamische Regelungsverhalten verbessert, ohne dabei zu zusätzlichen Verzerrungen im stationären Bereich zu führen. Darüber hinaus hat die Stromsollwertberechnung einen großen Einfluss auf die Stabilität. Um dies zu untersuchen, wird die minimal notwendige Netzkurzschlussleistung für einen stabilen Betrieb ermittelt. Das Ergebnis zeigt, dass netzfolgende Umrichter stabil in schwachen Netzen betrieben werden können, allerdings sehr schwache Netze wahrscheinlich zur Instabilität führen.

Netzbildende Regelung ermöglichen den Umrichterbetrieb in sehr schwachen Netzen und können darüber hinaus auch bei unsymmetrischen Netzfehlern die Wirkleistungsoszillationen unterdrücken oder die Netzspannungen stützen. Dafür wird eine Spannungssollwertberechnung für die Droop-Regelung vorgestellt, die die Wirkleistungsoszillationen unterdrückt. Der Vergleich mit einem Regelungskonzept für Netzspannungsstützung zeigt, dass die beiden Regelungsziele nicht simultan erreicht werden können, sodass deren Anwendung davon abhängt welches der beiden Regelungsziele eine höhere Priorität hat.

Die präsentierten Modelle und Ergebnisse sind mit Hilfe von drei entwickelten Prüfaufbauten experimentell validiert worden.

Basierend auf diesen Erkenntnissen, können folgende Schlussfolgerungen gezogen werden: Erstens, für Umrichter ergeben sich andere Worst-Case Betriebsszenarien als für konventionelle Generatoren am Netz. Dies muss vor allem bei der Auslegung und Bewertung der Regelung beachtet werden. Zweitens, PLLs müssen unter Berücksichtigung der Stromregelung

ausgelegt werden, wobei zusätzlich die transiente Stabilität in schwachen Netzen und bei kritischen Netzfehlern mitberücksichtigt werden muss. Dafür müssen durch die Struktur der Umrichterregelung vor allem Analyseverfahren für nichtlineare Systeme zum Einsatz kommen. Drittens, netzfolgende Umrichter können einen stabilen Betrieb nur bis zu einer bestimmten minimalen Netzkurzschlussleistung gewährleisten, die maßgeblich von der Regelungsstruktur und der Stromsollwertberechnung abhängig ist. Viertens, für sehr schwache Netze sollten netzbildende Regelungen eingesetzt werden, um das System stabil zu halten. Diese können darüber hinaus auch zusätzliche Netzdienstleistungen während unsymmetrischer Fehlerfälle bereitstellen. Es ist davon auszugehen, das umrichterbasierte Netzabschnitte im derzeitigen Stadium von netzfolgenden als auch netzbildenden Umrichter profitieren, um bei hohen als auch bei kleinen Kurschlussleistungen stabil betrieben werden zu können.

Contents

Abbreviations

AARC Average Active–Reactive Control, 131, 136 f., 141 f., 158 f., 166, 207
ADC Analog-Digital-Converter, 53, 87
ANS Amplitude Normalization Scheme, 59 f., 65, 79, 81, 95, 103
BPSC Balanced Positive Sequence Control, 131, 136 f., 141, 158
CPU Central Processing Unit, 40, 47, 53 f., 87
DI Digital Input, 53
DO Digital Output, 53
DSOGI Dual-Second-Order-Generalized Integrator, 10, 57, 71 f., 74, 80, 85, 103, 105 f., 112 f., 115, 118, 122, 124, 135, 153, 165
DSRF Dual Synchronous Reference Frame, 10, 33, 57 f., 68–74, 80, 82, 85, 88, 90 ff., 99, 103, 105 ff., 165
EAC Equal Area Criterion, 107, 145, 148, 151
EMI Electromagnetic Interference, 40, 47 f.
EPMAF Enhanced Moving Average Filter with Prefiltering Stage, 74 f., 80 ff., 85, 92, 99, 105
EXP Experiment, 90
FFT Fast Fourier Transformation, 28, 137
FOH First-Order-Hold, 54
FPGA Free Programmable Gate Array, 40, 47, 53 ff., 87
FPNSC Flexible Positive and Negative Sequence Control, 131 f., 141
FRT Fault Ride-Through, 6, 24 f., 29 ff., 39, 42, 50, 63, 67, 97, 113 f., 118, 127, 140, 153, 156
GUI General User Interface, 47
HVRT High-Voltage Ride-Through, 8, 29
IARC Instantaneous Active–Reactive Control, 131
IGBT Insulated Gate Bipolar Transistor, 5, 16, 42, 47 f., 50, 52, 124, 197
ISC Instantaneous Symmetrical Components, 19 f., 23, 198
LOS Loss of Synchronization, 6, 107, 145, 148, 150 f.
LPF Low-Pass Filter, 153, 159
LSM Large-Signal Model, 10, 40 ff., 58, 60 f., 71 f., 74, 76, 87, 90 ff., 95, 99, 101, 103, 105 f., 113, 124, 137

SOGI Second Order Generalized Integrator, 68, 71 f.
SPWM Sinusoidal Pulse-Width Modulation, 16, 87, 115, 117, 197, 202
SRF Synchronous Reference Frame, 22 f., 33 f., 57 ff., 69, 71, 75, 79, 88, 97, 107, 145, 148, 205 f.
SSM Small-Signal Model, 10, 42, 58, 60 f., 65, 69, 71 f., 74–77, 80, 82, 84 f., 87, 90, 92, 97, 99, 103, 105, 113, 118, 124
STATCOM Static Synchronous Compensator, 6
SVM Space Vector Modulation, 16
THD Total Harmonic Distortion, 113, 142
UEP Unstable Equilibrium Point, 41, 107, 148 f.
VCL Vector Current Limitation, 36, 132
VOC Voltage Oriented Control, 10, 32 ff., 36, 46, 52 f., 57, 93 ff., 97, 99, 101, 103, 113 ff., 119, 122, 145, 153, 165 f.
VSC Voltage Source Converter, 6, 16, 48, 57
VSG Virtual Synchronous Generator, 32
VSS Voltage Support Scheme, 131 f., 138, 141, 143, 159, 165 f., 207
VVL Vector Voltage Limitation, 113, 119, 135
ZAPOC Zero Active Power Oscillation Control, 133 f., 136 ff., 141 ff., 165
ZOH Zero-Order-Hold, 54 f.
ZRPOC Zero Reactive Power Oscillation Control, 133 f., 136 f., 141 f.

Nomenclature

$f_{\mathbf{s}}$	Sampling frequency, 54
$f_{\mathbf{sw}}$	Converter switching frequency, 43, 48, 50
$f_{\mathbf{res}}$	Filter resonance frequency, 48
$\mathbf{D}$	Feedthrough matrix, 44
$\mathbf{C}$	Output matrix, 44
$\mathbf{B}$	Input matrix, 44
$\mathbf{A}$	State or system matrix, 44
$\mathbf{y}$	Output vector, 43 f.
$\mathbf{x}$	State vector, 43
$\mathbf{u}$	Input vector, 43 f.
$\cos(\varphi)$	Power factor, 5
m	Modulation index defined as fundamental frequency amplitude to $V_{\mathrm{dc}}/2$ ratio, 5
VUF	Ratio of negative sequence voltage to positive sequence voltage (voltage unbalance factor), 26, 29, 65, 67, 71, 136 f., 157, 159
$\underline{D}$	Complex voltage characteristic factor, 26
T	Period of a time-periodic oscillation, 22
$\mathbf{T}_{\mathrm{dq}^n}$	Park transformation matrix locked on the n-th harmonic, 23
$\mathbf{T}_{\mathrm{dq}^{-1}}$	Park transformation matrix for the negative sequence, 24
$\mathbf{T}_{\mathrm{dq}}$	Park transformation matrix, 22 f., 33, 59
$\mathbf{x}^n_{\mathrm{dq}}$	Vector of the n-th harmonic of the three-phase system in dq-frame, 23
$\mathbf{x}^-_{\mathrm{dq}}$	Negative sequence vector of a three-phase system in dq-frame, 23
$\mathbf{x}^+_{\mathrm{dq}}$	Positive sequence vector of a three-phase system in dq-frame, 23
$\mathbf{x}_{\mathrm{dq}}$	Vector of a three-phase system in dq-frame, 23
$\mathbf{x}^-_{\alpha\beta}$	Negative sequence vector of a three-phase system in $\alpha\beta$-frame, 22
$\mathbf{x}^+_{\alpha\beta}$	Positive sequence vector of a three-phase system in $\alpha\beta$-frame, 22
$\mathbf{T}_{\alpha\beta 0}$	Real Clarke transformation matrix, 21
$\underline{\mathbf{T}}_{\alpha\beta}$	Complex Clarke transformation matrix, 21
x_0	Complex common mode component of an arbitrary three-phase system, 20 f.
x_β	Complex β component of an arbitrary three-phase system in $\alpha\beta$-frame, 20 ff.

1 Introduction

Increasing electrification in most areas of life leads to more process efficiency and comfort, and thus prosperity for all people. Especially, efforts in automotive electro-mobility, electric aircraft, and industrial automation will enable higher mobility, less pollution, and increasing sustainability. Prosperity often leads to increased energy consumption that seems to be in contrast with sustainability. However, this is not always true and consuming more electrical power could be sustainable, if the power is generated by Renewable Energy Sources (RES). This sustainable power consumption requires high efforts in efficient power generation, conversion, and transportation. Solving and improving these key elements will pave the way to reliably, robustly, and sustainably generated and distributed power, and thus lasting prosperity by electrifying most areas of life.

RES with their power electronic front ends are the backbone of sustainable electrification. Already 46% of the electric energy is generated by RES in Germany [1]. Particularly, wind power and Photovoltaic (PV)-generators rely on power electronic front ends that start to affect power system operation and stability. Hence, the power electronic dominated grid is a plausible future scenario and already real in some grid parts with a large share of RES. The problem with fluctuating power of RES attracts much attention in recent research. Proposed solutions, such as increasing energy storage integration or transportation capacity, are discussed by a broad research community and are followed by a large public. However, present and future power systems are also adversely affected by less obvious phenomena that are closely related to power electronic components, their control, and their interaction with other power system components.

A spectacular power system disruption caused by power converters happened in 2016 in California. Due to the tripping of several transmission lines during a fire, 1.2 GW PV generation also tripped that caused power outage in a large area [2]. Surprisingly, it was not the decreased transmission capacity of the power system that induced the interruption, but a special instability phenomenon of PV converters. This example highlights the importance of the fast-evolving research field of grid converters. Understanding these power electronic components and their interactions with power systems is crucial to safely operate present and

future power systems. Consequently, this thesis focuses on developing models and analysis methods to understand these interactions, deriving design processes and enhancing existing controls to improve the control performance of grid converters.

2 Critical Converter Properties Concerning Weak Grids and Fault Ride-Through

Shifting our electricity generation towards PV and wind power leads to a tremendously increasing number of power electronic converters in the power systems. Two essential properties dominate how converters interact with the grid: first, converter characteristics are predominantly affected by their control; second, their maximum output current is very limited compared to conventional synchronous generators. Converter control is getting more complex and diverse to sufficiently handle most of the occurring grid scenarios. Two basic control concepts are the grid-following and grid-forming control, where the grid-following concept controls the output current of the converter and the grid-forming concept controls the output voltage. Particularly, adverse grid conditions, such as unbalanced grid faults, may critically affect stability and performance of these controls. Unbalanced faults cause voltage magnitudes and angles to differ from the normal operation and demand complex control structures and sophisticated modeling of the converter. The small maximum output current of converters leads to weak grid parts, where the grid voltages are prone to disturbances and sensitive to power variations. Weak grid parts are vulnerable to new instability mechanisms and power quality problems. Consequently, this thesis focuses on the modeling, analysis, and control of grid converters in weak electric grids and during unbalanced grid faults.

A suitable system topology is the starting point of the analysis. Here, a trade-off between system complexity and sufficiently representing the original system behavior must be considered. The chosen topology contains at least two RES-converters fed by a current source with i_{dc} ($i_{\mathrm{dc},n}$) and connected to a Point of Common Coupling (PCC), as shown in Fig. 2.1. The PCC connects several converters to the grid through a line impedance $\underline{Z}_{\mathrm{L}}$ ($\underline{Z}_{\mathrm{L},n}$). The grid is modeled by a voltage source $\mathbf{v}_{\mathrm{S}}$ and source impedance $\underline{Z}_{\mathrm{S}}$, which can be used to emulate weak grids by increasing $\underline{Z}_{\mathrm{S}}$, as presented in section 3.1.1. The fault models include different types of short-circuits and varying fault impedances $\underline{Z}_{\mathrm{F}}$ according to section 3.3. This small multi-converter system can be used to investigate parallel converter scenarios without extensive complexity. Based on this topology, the critical converter characteristics in weak and unbalanced grid scenarios are described throughout this chapter.

Converter characteristics during faults are part of several standards (see section 3.3). However, these standards do not address limits of converter hardware and control, and they typically

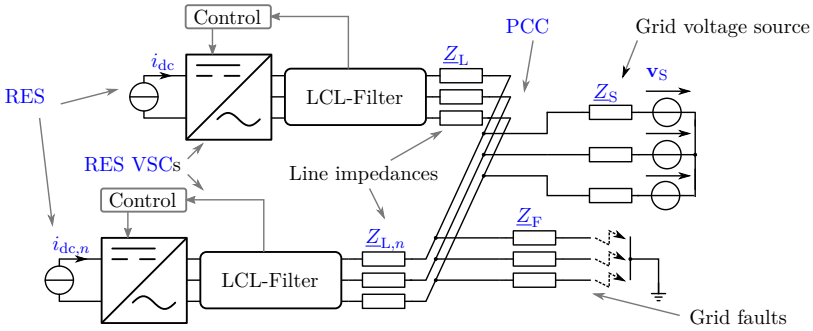


Figure 2.1: Multi-converter setup with line impedance ($\underline{Z}_L$, $\underline{Z}_{L,n}$), grid and fault model.

do not consider different grid scenarios such as fault types and line impedances. Requirements based on a single grid scenario simplify the control design, but do not necessarily achieve the desired support of the grid voltage. An example of this is the requirement to inject reactive power during voltage sags. The standards recommend that the converters should inject reactive power to recover the voltage at the PCC, but injecting reactive and active power depending on the line impedance ratio achieves much better voltage recovery [3, pp.116-119]. This example highlights that the grid codes must be extended, and further investigations on converter hardware and control are crucial for operating converter dominated grids safely and reliably. Therefore, the following investigations are categorized into: safe converter operation, optimized converter utilization, and optimized grid support. Safe converter operation prevents converter tripping and is crucial for the converter to continue injecting power and supporting the grid voltage. Optimized utilization mainly focuses on optimizing converter operation regarding aging of components or efficiency. In contrast, the optimized grid support mainly addresses how the converter can support the grid voltages.

2.1 Safe Converter Operation

Safe converter operation requires that converter currents and voltages are limited. The maximum current is closely related to the thermal limits of semiconductors, whereas the voltage limits primarily depend on their maximum blocking voltages. Exceeding these values may damage the semiconductors or trip fuses. Although state-of-the-art converter control typically limits the converter currents and voltages, the control may be unstable during critical operational scenarios, which may also trip the converter.
The maximum converter rating and a stable control are crucial for safe grid operation. The converter rating mainly depends on losses and the thermal limits of the converter. Hence,

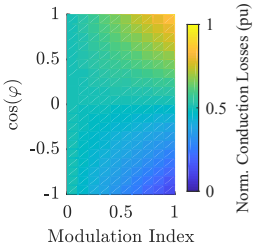


Figure 2.2: IGBT conduction losses dependent on m and $\cos(\varphi)$.

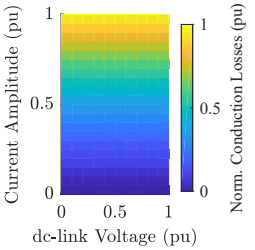


Figure 2.3: Overall conduction losses dependent on V_{dc} and $\hat{I}$.

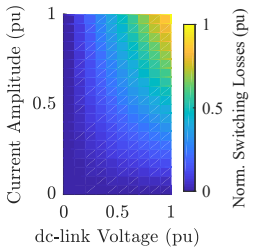


Figure 2.4: Characteristics of IGBT switching losses dependent on V_{dc} and $\hat{I}$.

semiconductor losses are discussed to assess thermal limits without considering the details of the converter cooling system and mechanical design. Some practical details on converter design are provided in chapter 4. Control stability predominantly depends on the control structure and operational scenarios. Consequently, two critical instability phenomena are introduced at the end of this section.

Especially during grid faults, converters may need to provide maximum current, and the broad operation range of the modulation index m, power factor $\cos(\varphi)$, and current make fault scenarios even more critical. From the converter's point of view and considering only electrical parameters, particularly m, $\cos(\varphi)$, the dc-link voltage V_{dc}, and the maximum current affect the converter losses. These losses include conduction losses and switching losses of the typically applied Insulated Gate Bipolar Transistors (IGBTs) and diodes. The overall conduction losses may not change significantly with m and $\cos(\varphi)$, but the loss distribution between diodes and IGBTs is changing [4], [5, pp.277-279]. Conduction losses predominantly depend on the current magnitude if the collector-emitter threshold voltage of the IGBT is similar to the forward threshold voltage of the diode and the on-state resistance of the IGBT is similar to the on-state resistance of the diode, as shown in Fig. 2.2 and 2.3. A proof for this characteristic is given in appendix A.1. The switching losses of the converter do not depend on m and $\cos(\varphi)$ but change with V_{dc} and the current amplitude as presented in Fig. 2.4 [4], [5]. In most RES converters, the dc-link voltage is kept near a constant reference, and thus only the maximum current significantly affects the losses and defines the thermal limits of the converter.
The specification of the maximum current is mainly restricted by costs and efficiency. However, designing converters for higher current rating becomes necessary for supporting the grid voltages. For grid-following converters, typical current ratings vary in the range of 1-2 pu of the rated current [3], [6], [7]. Grid-forming converters have current ratings up to 3-5 pu [3], [7]. Particularly in weak grids, the converter rating significantly affects the grid voltages and must be selected thoroughly, which is discussed in chapter 7.

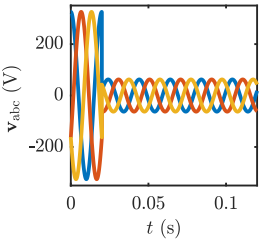


Figure 2.5: Fault voltages during a balanced three-phase fault in the low voltage grid.

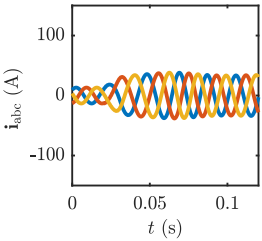


Figure 2.6: Converter currents during a balanced three-phase fault with a stable response.

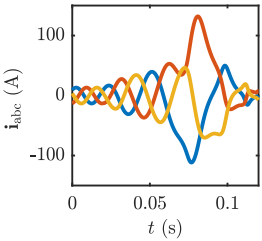


Figure 2.7: Converter currents during a balanced three-phase fault with an unstable response.

Current limitation concepts significantly alter steady-state characteristics, control dynamics, and thus stability. Since the limitation methods depend on the current control, the necessary background and analysis on these controller components is presented in chapter 5. Then, detailed investigations on their impact on the control under unbalanced grid faults are presented in chapter 6 and chapter 7. These chapters answer two main questions:

1. How to limit the converter current during severe, unbalanced grid faults?
2. How to design a limitation with minimum effect on the power control or grid support functionality?

Converter tripping may occur due to limitation failure or unstable converter control. Notably, severe grid faults are critical for control stability due to severe grid voltage transients. For example, in Fig. 2.5 a three-phase fault may result in grid voltage waveforms that contain a severe magnitude step and grid angle jump. During these severe grid voltage transients, two stability related mechanisms are the Loss of Synchronization (LOS) [8], [9] and controller latch-up [10]. The LOS is predominantly caused by the PLL and its interaction with the current control under weak grid conditions. Exemplary, Fig. 2.6 and 2.7 show the phase currents for a stable and unstable PLL design, respectively. In the unstable case, converters may trip due to overcurrent, which leads to failing of the Fault Ride-Through (FRT) requirements. Unlike LOS, the latch-up is critical for cascaded control structures that are often used for grid-forming converters. However, the two instability mechanisms have one thing in common: the involved controller parts are nonlinear, since PLLs contain trigonometric terms and limitations often consist of magnitude calculations and saturation blocks. Following this, two main questions concerning stability are answered in chapters 5 and 6:

3. Which models can be used to describe these instability mechanisms, and does an analytical stability requirement exist?
4. How to design and evaluate the critical controller parts to achieve a stable and fast converter current step response during grid faults?

2.2 Optimized Converter Utilization

As discussed before, RES-Voltage Source Converters (VSCs) must operate within safety limits at any time, and especially during faults. But what is the optimum converter operating point during grid faults? From the converter's point of view, the faults demand high currents that must comply with the standards [11], [12], [13]. Additionally, unbalanced grid faults lead to unbalanced power in the three converter phases causing double fundamental frequency power oscillations. These oscillations give rise to harmonics in the output power, degradation of the dc-link capacitors, and overvoltages [14], [15]. These phenomena are particularly critical for PV-systems, wind farms, or Static Synchronous Compensators (STATCOMs) [16], [17], [18]. The modified *pq*-theory can describe power in unbalanced multi-phase systems according to [19, pp.82-87]. This theory reveals that the instantaneous active power propagates to the dc-link of the converter and causes currents with double fundamental frequency. These currents will change the dc-link voltage depending on the dc-link capacitor design. Hence, fault scenarios, converter power setpoints, and the capacitor design affect dc-link voltage oscillation magnitudes, and thus their impact on the control characteristics.
An exemplary simulation of a two-phase-to-ground fault demonstrates this behavior, and Fig. 2.8 shows the corresponding fault voltages and currents. In this test, the converter balances output currents, and the resulting instantaneous power oscillations cause dc-link voltage oscillations, as shown in Fig. 2.9. Since the grid voltages and converter currents determine these oscillations, they can be minimized by adequately choosing the converter current reference depending on the grid voltage.
Based on the presented characteristics, the following questions are of major interest and are discussed for the grid-following and grid-forming control in chapters 6 and 7, respectively:

5. How can dc-link voltage oscillations be described accurately by a generic model?

6. What influence does the dc-link capacitor design process have on the dc-link oscillations?

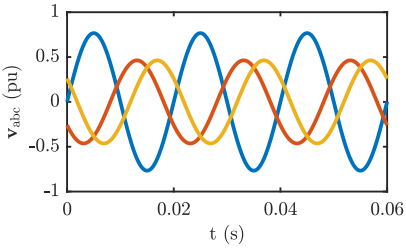


Figure 2.8: Grid voltages during a two-phase-to-ground fault.

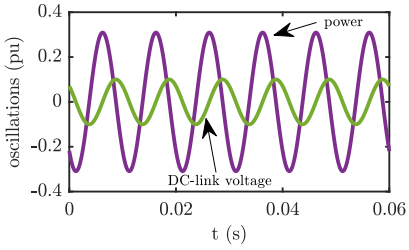


Figure 2.9: DC-link and power oscillations during a two-phase-to-ground fault with balanced current injection.

7. How should the converter be controlled to limit dc-link voltage oscillations during unbalanced grid faults?

2.3 Grid Voltage Support

Nowadays, almost all RES converters must support the grid voltage and frequency. Operating RES with Maximum Power Point Tracking (MPPT) or maximum power injection without any grid support is not suitable for stable and reliable electric grid operation anymore due to the large share of RES. Injecting active and reactive power based on voltage and frequency deviations compared to their nominal values may keep voltages and frequencies in their predefined tolerance band. That means converters support the grid voltage and frequency during steady-state by injecting active and reactive power according to the standards [11], [12], [13]. During grid faults, generators should recover grid voltages into the normal state tolerance band, but this demands high currents depending on the grid strength. Complete voltage recovery is often not possible due to the low current rating of converters. At least, the grid voltages should stay in the Low-voltage Ride-Through (LVRT) and High-Voltage Ride-Through (HVRT) voltage tolerance band to prevent tripping of nearby loads or other RES [20].
Various fault scenarios may occur in power systems that basically differ in the three-phase voltage magnitudes and angles. Particularly, unbalanced faults, i.e., different magnitudes, and phase angles in the three phases compared to the nominal voltage waveform, demand complex reference calculation to achieve the support objectives mentioned above. Various research contributions propose current reference generators for faults [21], [22], [23], [24], [25]. Based on these current reference generators, strategies for optimum voltage support can be derived, and it is analyzed how they alter the grid voltages in steady-state. Some publications focus on current reference generators that recover the voltages during unbalanced faults, but they typically do not consider critical converter parts or stability [26], [27], [28], [20]. As mentioned before, the communication is out of scope but could further enhance grid support, due to reference calculation based on fault bus voltage and current data [29]. Fig. 2.10 and 2.11 show how the inverter could inject currents to keep the phase voltages in the tolerance band during an unbalanced fault. If the converter current is limited to its nominal value, the control cannot recover the voltages, as shown in Fig. 2.12 and 2.13. This example highlights the advantages of supporting grid voltages by adjusting the current references and reveals limits of the support due to the maximum current.
The previous example shows satisfactory steady-state behavior but high undershoots and overshoots of the voltages during fault initiation and clearing. Only few contributions analyze the converter dynamics during fault transients [30], [31]. However, these dynamics are crucial to quickly recover the grid voltages and sufficiently limit converter currents. Especially during severe grid faults, the current and voltage limitation and grid synchronization predominantly

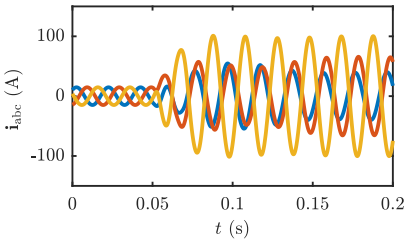


Figure 2.10: Converter currents during an unbalanced grid fault with voltage support control.

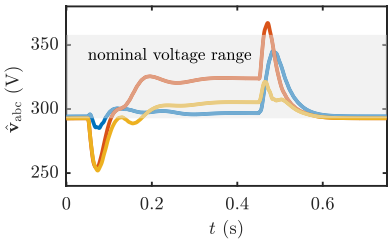


Figure 2.11: PCC voltage magnitudes during an unbalanced grid fault with voltage support control.

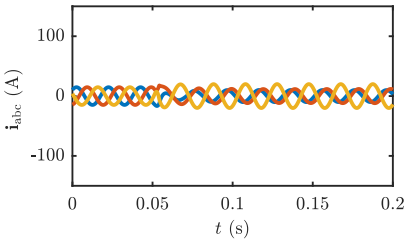


Figure 2.12: Converter currents during an unbalanced three-phase fault with voltage support control and current limitation.

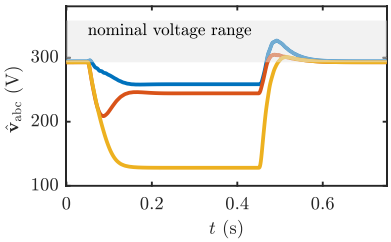


Figure 2.13: PCC voltage magnitudes during an unbalanced three-phase fault with voltage support control and current limitation.

affect the dynamics of the converter control [16], [21]. Accordingly, mainly three questions arise that will be answered in chapters 5, 6, and 7 for the different control strategies:

8. Which controller parts critically affect the dynamics of the grid supporting control?
9. How to design critical controller parts to achieve an optimum stationary and transient performance?
10. What are the objectives of the converter control regarding grid support, and which current reference generator achieves them?

2.4 Thesis Structure and Contributions

The thesis is structured as follows: first, chapter 3 presents the theoretical framework to describe power electronics in power systems and their modeling and control in weak and unbalanced grids. Second, the analysis framework based on analytical models, offline-simulations, and experimental test benches is introduced in chapter 4. The positive and negative sequence decomposition using PLLs is analyzed in chapter 5. Then, the grid-following control in weak grids and during unbalanced faults is presented in chapter 6. Finally,

grid-forming converter control under adverse grid conditions is designed and investigated in chapter 7. Based on the research questions, this thesis covers the following goals and solutions:

1. PLLs are the control bottle-neck due to comparably slow grid voltage detection and sequence decomposition. In order to overcome this problem, a general design framework and process is proposed to optimize the control speed and distortion immunity. This framework includes Small-Signal Models (SSMs), Large-Signal Models (LSMs), and a thoroughly determined worst-case grid scenario. Additionally, the typically applied Symmetrical Optimum (SO) design is discussed for PLLs with prefilter, and its limits are exposed. Finally, five different PLLs are designed, and their performance is evaluated under various fault scenarios.

2. PLLs dominate the power injection characteristics of grid-following converters during severe grid faults. Therefore, LSMs and SSMs were developed to accurately describe the transfer characteristics of the Voltage Oriented Control (VOC) during large grid angle jumps. These models indicate a coupling between the converter's active and reactive current references, which predominantly determines the settling time of currents in response to grid faults. The results point out that only a faster PLL can sufficiently decrease the settling time of the reactive current if a fault occurs. Contrarily, a delay of the active current after fault clearing significantly reduces the settling time of the reactive current.

3. The phase portrait and numerical LSMs are identified as a suitable tool to analyze nonlinear controller parts of power electronics. Lyapunov's direct method can be used to derive analytical stability criteria based on design parameters. If analytical solutions are not available, numerical simulations can extract the transient stability boundary. This analysis reveals that Dual Synchronous Reference Frame (DSRF)- and Dual-Second-Order-Generalized Integrator (DSOGI)-PLLs are prone to instability due to their adaptive filter structures. The general applicability of Lyapunov's method is proved for PLLs and grid converters with VOC under weak grid conditions by determining an analytical stability criterion and an estimate of the Region of Attraction (ROA).

4. A limitation scheme for the converter currents is proposed that accurately limits the phase current magnitude during unbalanced grid faults. This limitation scales the output power of the converter, and thus conserves characteristics of the power control and objectives of the voltage support even if the converter reaches limits of the current. Compared to conventional approaches, it is not necessary to change reference values, which typically rely on sequence decomposition. Decomposing of the sequences often causes control dynamics to deteriorate. The proposed limitation is extensively tested under various fault and grid scenarios.

5. A model for the nonlinear characteristics of dc-link oscillations is developed. Based on this, criteria to evaluate the linearized model are derived and applied to the capacitor design. Critical assumptions for the dc-link capacitor design are discussed, pointing out that the converter current references are suitable means to limit dc-link voltage oscillations. Therefore, a current reference generator is proposed that rejects these oscillations in any power reference setpoint, fault scenario, and even during current limitation. Finally, the trade-off between rejecting the dc-link oscillation, supporting the grid voltage, and stability is discussed, which is crucial to respect converter utilization and grid support objectives simultaneously.

6. There are various current reference generators for grid-following converters particularly designed for unbalanced faults. However, converters are typically controlled with grid-forming control if the grid connection becomes too weak. Hence, the current reference generators for unbalanced faults were adapted to grid-forming converters in this thesis. These reference generators result in a potent power control framework in positive and negative sequence to optimize the system support. The trade-off between dc-link oscillation rejection, grid voltage support and stability is also crucial for the grid-forming control and thus is discussed considering the maximum current rating of the converter.

Several related papers were published during my work in the department of power electronics at TU Berlin. A complete publication list can be found in the appendix 8.

3 Theoretical Framework

3.1 Power Electronics in Power Systems

Germany's electricity generation relied on 46% renewables in 2019 [1]. This massive integration of PV and wind power increases power converter density in power systems. Power systems are divided into transmission and distribution grids [32], and differ in their voltage levels. Power transmission typically relies on medium voltage to high voltage grids, whereas power distribution often is based on low voltage to medium voltage grids. Voltage levels are of major interest for power converters because they determine converter topology, transformer configuration, and grid integration standards.
Converter density in different grid types can be approximated using the installed power of renewables. At the end of 2014, approximately 90% RES were connected to the distribution grid in Germany [33]. Wind generators typically feed into medium and high-voltage networks [34], whereas PV generators are mainly connected to low and medium voltage grids [34]. Fig. 3.1 gives an overview of the shares of installed power and their voltage level distribution. Power system voltage levels determine steady-state operating points and transient characteristics of the grid voltages that are important to define operational scenarios for grid converters. These scenarios are distinguished between the normal state and abnormal state [32]. In the normal state, the voltages and frequencies are in their predefined boundaries around the nominal operating point. In contrast, the grid voltages leave their safety limits during severe disturbances like faults or outages. These operational scenarios must be analyzed and modeled to understand their impact on power converters.

3.1.1 Power System Model

Power systems consist of transmission lines, transformers, generation units, and loads, and are very complex and diverse in their structure. To analyze the characteristics of RES interfacing power converters efficiently, the complexity of the grid model must be limited. In some applications like wind parks, a local PCC serves as a reference bus to split the grid into smaller parts. A voltage source, containing harmonics and disturbances, with a

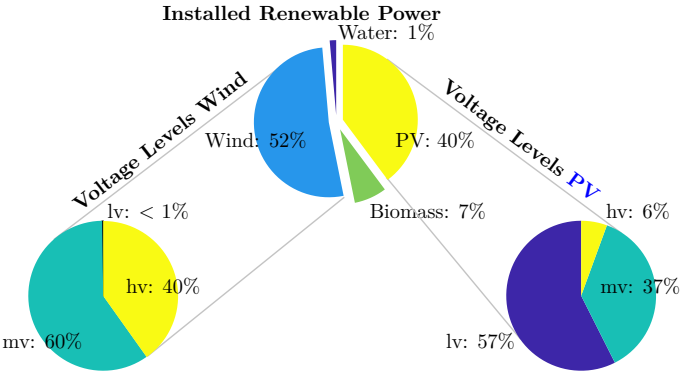


Figure 3.1: Installed power of RES 2018 in Germany divided into energy sources and voltage levels [34].

source impedance models the interaction with the rest of the power system [35]. The voltages are defined using the phase amplitudes $\hat{V}_\mathrm{S}$, the phase angle $\theta{=}\omega_1\, t$, and the fundamental frequency f_1 or angular frequency ω_1. Additionally, the grid harmonics are described by $\hat{V}_{\mathrm{S},n}$, and f_n. Accordingly, the grid voltages v_a, v_b, and v_c are defined as follows:

$$v_\mathrm{a}(t) = \sum_{n=1}^{m} \hat{V}_{\mathrm{Sa},n} \cos\left(n\left(\omega_1 t\right) + \delta_n\right) \quad , \tag{3.1}$$

$$v_\mathrm{b}(t) = \sum_{n=1}^{m} \hat{V}_{\mathrm{Sb},n} \cos\left(n\left(\omega_1 t - \frac{2\pi}{3}\right) + \delta_n\right) \quad , \tag{3.2}$$

$$v_\mathrm{c}(t) = \sum_{n=1}^{m} \hat{V}_{\mathrm{Sc},n} \cos\left(n\left(\omega_1 t + \frac{2\pi}{3}\right) + \delta_n\right) \quad . \tag{3.3}$$

Grid voltages predominantly affect the PCC voltages of RES-converters. However, generation units or loads may also affect PCC voltages depending on the source impedance, which is described in the following.

Weak Grids

The increasing amount of RES leads to a growing number of weak grids. Particularly large offshore wind farms with an ac-connection offer interesting weak grid scenarios due to their large electrical distance from the main grid with its conventional power plants [36]. Weak grids include two main characteristics: first, generators' injected power critically affects the voltage magnitude and angle at the PCC if the source impedance is too large. The second characteristic is related to the inertia at the PCC. Conventional power plants, e.g. coal-fired plants, consist of large synchronous generators, which provide large inertia due to their

mechanical structure. Due to low inertia at the PCC or fewer conventional power plants, active power changes can severely affect the frequency, which may cause instability.
The short circuit power S_{sc} indicates how the grid voltage depends on the injected power. It is defined as power provided by the main grid during a short circuit at the PCC (see 3.4). Hence, S_{sc} indicates grid strength at this feeder and how the power provided by the generation unit changes the PCC voltage. This impact also depends on generators' power rating. Therefore, S_{sc} is extended to the Short Circuit Ratio (SCR) as normalized quantity considering the sum of the generated power S_k connected to the PCC. For the grid model, the SCR can be adjusted by changing the source impedances $\underline{Z}_S$. Commonly, grid connections with SCR<6 are weak [37], whereas SCR>20 correspond to stiff grids [37]. However, weak grids and strong grids are not well defined. Some literature considers SCRs<3 as weak grid and any SCRs>3 as strong grid [32].

$$S_{sc} = \frac{V_g^2}{|\underline{Z}_S|} \tag{3.4}$$

$$SCR = \frac{S_{sc}}{\sum_{k=1}^{l} S_k} \tag{3.5}$$

The inertia of the grid is defined by the Rate of Change of Frequency (ROCOF) and the corresponding criterion typically describes frequency gradients in Hz/s/MVA as response to active power steps [37]. Additionally, steady-state frequency deviations may occur in the grid. In most 50 Hz power systems, the steady-state frequency varies in the range of 49.5 Hz$<f_1<$50.5 Hz. This frequency range can be even larger during grid faults with 47.5 Hz$<f_1<$51.5 Hz [38]. This deviation can be modeled by changing the frequency of the grid voltage source. Fig. 3.2 shows the simplified grid model, which assumes that the line impedances dominate the simplified power system characteristics and neglects the ROCOF criterion.

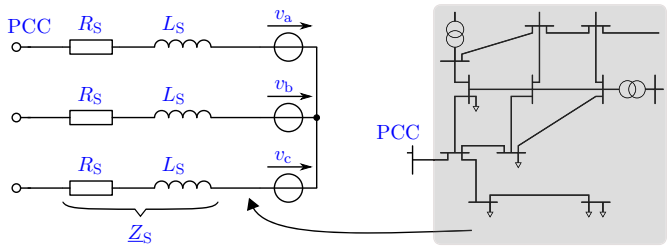


Figure 3.2: Simplified equivalent circuit of a complex exemplary power system considering resistive and inductive line impedances.

Several standards provide the parameters for line and source impedances [13], [12], [38]. In most systems, overhead lines connect the different buses. Hence, the capacitances from line to ground C_S are negligible [35], [39]. The ratio of the resistive and inductive part of the line impedances depends on the voltage level. In the low voltage grid, the line impedance is mainly resistive. In contrast, inductances dominate impedance characteristics in high voltage grids. The impedance of medium voltage grids has similar parts of resistance and inductance, and thus neither component can be neglected. Typical values for the equivalent inductance L_S and resistance R_S are summarized in Table 3.1 [35], [3], [40]. The exemplary test scenarios throughout the thesis use these values.

Table 3.1: Equivalent quantities of typical line impedances for different voltage levels depending on the current rating.

Voltage Level	I_N (A)	L_S (mH/km)	R_S (Ω/km)	C_S (nF/km)	$r_S = X_{LS}/R_S$ (pu)
Low (400-690 V)	142	0.26	0.642	n/a	0.129
Medium (3.3-33 kV)	396	0.60	0.161	n/a	1.2
High (36-765 kV)	840-1380	0.77-0.91	0.026-0.090	12	>10

Transformer and Grounding Types

Power systems grounding affects grid operation during grid faults. The tradeoff between safety and reliability determines the grounding strategy. High fault currents occur in low impedance grounded systems, which makes the fault identification easy but leads to immediate tripping of the circuit breaker of faulty feeders [41]. In low-voltage grids and consumer areas, this is important due to safety regulations [42, p.565-571]. In contrast, reliability is more critical in transmission and industrial distribution grids. Hence, these systems are typically grounded with high impedances or operate isolated. The drawbacks are difficult fault identification and overvoltages, caused by the varying potential of the star-point connection.
The investigated scenarios in this thesis consider a high-impedance grounding or open star-point connection, respectively. 85% of the medium voltage grids use a resonant grounding [41], which corresponds to high impedance or isolated systems. The ground capacitances are not negligible for long lines. Therefore, the star-point connection of the transformer contains an inductance to compensate for capacitive fault currents. An open star-point connection sufficiently approximates the overall behavior of a resonant grounding.
Most RES applications use low-voltage converters as a grid interface. YNd-transformers typically interface RES-converters with medium or high voltage grids [43], [44]. The transformer causes coupling of the three-phase voltages due to the winding configuration and grounding concept. Notably, under fault conditions, this leads to a transformation of the fault type [45], [35] that is presented in detail in section 3.3. In normal operation, the transformer is modeled by an ideal voltage level transformation, which neglects parasitics of the transformer.

3.1.2 2-Level Converter with LCL-Filter

The vast majority of PV and wind power generation units include Voltage Source Converters (VSCs) as dc/ac front-ends to inject the generated power into the electric grid. In wind power generation systems, VSCs increase power output by enabling generators with variable rotor frequency. VSCs are necessary to connect PV-systems or fuel cells to the ac grid since these systems operate on dc voltage, which needs to be converted to ac to exchange power with the ac grid [46].

Three-phase, two-level VSCs are widely adopted in different RES applications, due to the simple topology and high reliability [47, pp.131-134]. They are composed of three half-bridges with a dc-link capacitor, as shown in Fig. 3.3. These half-bridges switch the positive or negative dc-link potential to the output to approximate the desired output voltage waveform. Since the output voltages intrinsically contain harmonics, almost all converters rely on output filters to comply with power quality requirements of grid codes. The vast majority of two-level converters use LCL-filters to suppress harmonics [48]. The IGBT control signals are typically generated by Pulse-Width Modulation (PWM) such as Space Vector Modulation (SVM) or Sinusoidal Pulse-Width Modulation (SPWM) [49].

Fig. 3.3 presents the electric circuit including the converter and filter, as well as the source impedance and grid connection. The converter input source is modeled as a controlled current source to emulate the injected power of the RES. The grid model was presented in section 3.1.1. The LCL-filter dominates converter plant characteristics and its parasitics

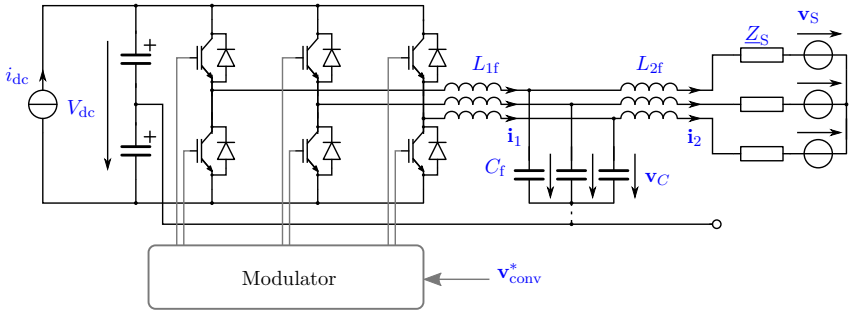


Figure 3.3: Three-phase two-level grid converter with LCL output filter.

significantly alter control characteristics. Fig. 3.4 shows the filter and grid plant considering these parasitic resistances. Moreover, this circuit illustrates the control plant from the converter point of view. For balanced three-phase systems, the vector description used in Fig. 3.4 is redundant. If one phase is defined in a balanced system, the other phases are just 120° phase-shifted copies of it. Consequently, one single-phase equivalent circuit accurately describes three-phase balanced systems and is widely adopted in the power system analysis.

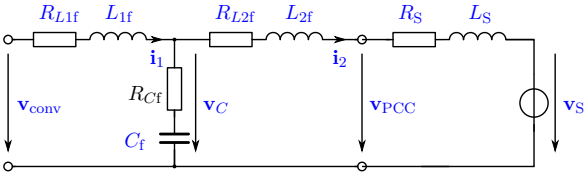


Figure 3.4: LCL output filter with parasitic resistances.

Unfortunately, this assumption is not valid for adverse grid conditions such as unbalances, so more sophisticated analysis techniques must be applied.

3.2 Phasors, Space Vectors and Symmetrical Components to Describe Grid Converter Dynamics during Faults

Most grid faults are single and two-phase faults and thus lead to unbalanced three-phase voltage systems [45]. Two basic methods are applicable to analyze these systems. The first method describes the three phases independently, whereas the second method is based on the symmetrical component theory and handles unbalanced three-phase systems by replacing them with three balanced systems [50], [32]. This technique enables three single-phase equivalent circuits to describe a four-wire system. These equivalent circuits represent the positive sequence rotating counter-clockwise, the negative sequence system rotating clockwise and the zero sequence components, which are related to the common mode. During grid faults, these sequences may be coupled depending on the fault conditions and grid grounding. Ref. [51] and [52] present a historical overview of the evolution of the theory since 1918.
Online calculation of the positive and negative sequence components is crucial for converter control to handle unbalanced grid faults. The zero sequence component is negligible because of the YNd-transformer configuration presented in section 3.1.1. The subsequent analysis uses the following notations:

- Bold upright letters define vector or matrix quantities, e.g. $\underline{\mathbf{x}}_a^{+-0}$,
- Vector arrows denote phasors, e.g $\vec{\mathbf{x}}_a^{+-0}$,
- Complex quantities are underlined, e.g. $\underline{a}$.

3.2.1 Positive, Negative and Zero-Sequence in abc-Frame

The abc-frame can sufficiently describe three-phase systems in the time domain. Symmetrical component decomposition splits the system into balanced components using the phasors of the grid quantities. These phasors are based on the analytical representation, which can

be generically described by 3.6. It contains the description of the fundamental frequency component and the n-th harmonic up to the m-th order, i.e., $n \in \mathbb{Z}\backslash\{-1;1\}$. The fundamental frequency component of the positive sequence serves as reference, i.e., $\delta_1 = 0$. The harmonics occur in positive and negative sequences or with positive or negative frequencies, respectively.

$$\underline{\mathbf{x}}_{\mathrm{abc}} = \begin{bmatrix} \hat{X}_{\mathrm{Sa},1}\mathrm{e}^{\mathrm{j}(\omega_1 t)} + \hat{X}_{\mathrm{Sa},-1}\mathrm{e}^{\mathrm{j}(-\omega_1 t+\delta_{-1})} + \sum_{n=-m}^{m} \hat{X}_{\mathrm{Sa},n}\mathrm{e}^{\mathrm{j}n(\omega_1 t+\delta_n)} \\ \hat{X}_{\mathrm{Sb},1}\mathrm{e}^{\mathrm{j}\left(\omega_1 t-\frac{2\pi}{3}\right)} + \hat{X}_{\mathrm{Sb},-1}\mathrm{e}^{\mathrm{j}\left(-\omega_1 t+\frac{2\pi}{3}+\delta_{-1}\right)} + \sum_{n=-m}^{m} \hat{X}_{\mathrm{Sb},n}\mathrm{e}^{\mathrm{j}n\left(\omega_1 t-\frac{2\pi}{3}+\delta_n\right)} \\ \hat{X}_{\mathrm{Sc},1}\mathrm{e}^{\mathrm{j}\left(\omega_1 t+\frac{2\pi}{3}\right)} + \hat{X}_{\mathrm{Sc},-1}\mathrm{e}^{\mathrm{j}\left(-\omega_1 t-\frac{2\pi}{3}+\delta_{-1}\right)} + \sum_{n=-m}^{m} \hat{X}_{\mathrm{Sc},n}\mathrm{e}^{\mathrm{j}n\left(\omega_1 t+\frac{2\pi}{3}+\delta_n\right)} \end{bmatrix} \tag{3.6}$$

$$\Rightarrow \vec{\mathbf{x}}_{\mathrm{abc}} = \left[\hat{X}_{\mathrm{Sa},1} \;\; \hat{X}_{\mathrm{Sb},1}\mathrm{e}^{\mathrm{j}\left(-\frac{2\pi}{3}\right)} \;\; \hat{X}_{\mathrm{Sc},1}\mathrm{e}^{\mathrm{j}\left(\frac{2\pi}{3}\right)}\right]^{\mathrm{T}} \tag{3.7}$$

Only considering the fundamental frequency component of $\underline{\mathbf{x}}_{\mathrm{abc}}$ and separating the time-dependency $\omega_1 t$ leads to the phasor representation according to 3.7. Complex Clarke's transformation given in 3.8 decomposes these phasors in their sequence components [53]. $\vec{\mathbf{x}}_{\mathrm{a}}^{+-0}$ and $\vec{\mathbf{x}}_{\mathrm{abc}}$ denote a set of voltage and current phasors. Hence, the presented transformations are valid for all three-phase steady-state quantities.

$$\vec{\mathbf{x}}_{\mathrm{a}}^{+-0} = \begin{bmatrix} \vec{x}_{\mathrm{a}}^{+} \\ \vec{x}_{\mathrm{a}}^{-} \\ \vec{x}_{\mathrm{a}}^{0} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \underline{a} & \underline{a}^2 \\ 1 & \underline{a}^2 & \underline{a} \\ 1 & 1 & 1 \end{bmatrix} \vec{\mathbf{x}}_{\mathrm{abc}} = \frac{1}{3}\underline{\mathbf{T}}_{+-0}\vec{\mathbf{x}}_{\mathrm{abc}} \tag{3.8}$$

Phase a in the positive, negative, and zero sequence ($\vec{\mathbf{x}}_{\mathrm{a}}^{+-0}$) completely describes the overall system. Information of the other two phases is redundant due to the fixed phase shift and magnitude of balanced systems. The complete description, e.g. $\vec{\mathbf{x}}_{\mathrm{abc}}^{+}$, is achieved by rearranging the transformation matrix $\underline{\mathbf{T}}_{+-0}$ to define $\underline{\mathbf{T}}_{+}$ as follows:

$$\vec{\mathbf{x}}_{\mathrm{abc}}^{+} = \begin{bmatrix} \vec{x}_{\mathrm{a}}^{+} \\ \vec{x}_{\mathrm{b}}^{+} \\ \vec{x}_{\mathrm{c}}^{+} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \underline{a} & \underline{a}^2 \\ \underline{a}^2 & 1 & \underline{a} \\ \underline{a} & \underline{a}^2 & 1 \end{bmatrix} \vec{\mathbf{x}}_{\mathrm{abc}} = \frac{1}{3}\underline{\mathbf{T}}_{+}\vec{\mathbf{x}}_{\mathrm{abc}} \tag{3.9}$$

The matrices $\underline{\mathbf{T}}_{-}$ and $\underline{\mathbf{T}}_{0}$ are given in the appendix A.2. The presented decomposition mainly consists of the complex transformation constant $\underline{a}$, which cannot be applied to real quantities and instantaneous time-domain waveforms. In order to overcome this problem, $\underline{a}$ can be interpreted as $2\pi/3$ phase lead, and thus applied to time-domain measurements, which leads

to the Instantaneous Symmetrical Components (ISC) [54]. Then, $\underline{a}$ can be calculated with a 90° phase lag, which is denoted by $\underline{q}$ according to:

$$\underline{a} = \mathrm{e}^{\mathrm{j}\frac{2\pi}{3}} = -\frac{1}{2} - \frac{\sqrt{3}}{2}\underline{q} \quad , \qquad \underline{a}^2 = \mathrm{e}^{-\mathrm{j}\frac{2\pi}{3}} = -\frac{1}{2} + \frac{\sqrt{3}}{2}\underline{q} \qquad \Rightarrow \underline{q} = \mathrm{e}^{-\mathrm{j}\frac{\pi}{2}} = -\mathrm{j} \quad . \tag{3.10}$$

Various filter algorithms or decoupling structures are proposed in the literature to realize the operator $\underline{q}$ that is necessary for online sequence decomposition of time-domain waveforms. None of them guarantees ideal transfer characteristics without time-delay, and the analysis and evaluation of these algorithms is presented in chapter 5.

Eq. 3.11 presents the resulting calculation of the positive sequence in the abc-frame. The relations for the negative and zero sequences are given in the appendix A.6 and A.7, respectively. These are simple algebraic expressions except for the $\pi/2$ lagged signals expressed by $\underline{q}\mathbf{x}_{\mathrm{abc}}$. $\vec{\mathbf{x}}^{+}_{\mathrm{abc}}$ is expressed in the phase domain and the real part corresponds to the time-domain waveform. This definition is essential for the further analyzed reference frames because the real and imaginary parts have a different physical meaning there.

$$\vec{\mathbf{x}}^{+}_{\mathrm{abc}} = \frac{1}{3}\begin{bmatrix} \vec{x}_{\mathrm{a}} - \frac{1}{2}(\vec{x}_{\mathrm{b}} + \vec{x}_{\mathrm{c}}) + \frac{\sqrt{3}}{2}(\underline{q}\vec{x}_{\mathrm{c}} - \underline{q}\vec{x}_{\mathrm{b}}) \\ \vec{x}_{\mathrm{b}} - \frac{1}{2}(\vec{x}_{\mathrm{c}} + \vec{x}_{\mathrm{a}}) + \frac{\sqrt{3}}{2}(\underline{q}\vec{x}_{\mathrm{a}} - \underline{q}\vec{x}_{\mathrm{c}}) \\ \vec{x}_{\mathrm{c}} - \frac{1}{2}(\vec{x}_{\mathrm{a}} + \vec{x}_{\mathrm{b}}) + \frac{\sqrt{3}}{2}(\underline{q}\vec{x}_{\mathrm{b}} - \underline{q}\vec{x}_{\mathrm{a}}) \end{bmatrix} \tag{3.11}$$

In summary, positive, negative, and zero sequence components accurately represent arbitrary three-phase or four-phase power systems. The ISC extends the symmetrical component theory to deal with instantaneous quantities and transients. ISC works for different reference frames such as $\alpha\beta$ or dq-frame, which are described in the following sections.

3.2.2 Positive, Negative and Zero-Sequence in $\alpha\beta$-Frame

Clarke's transformation was introduced in 1943 to describe transient processes in ac multiphase power systems [55]. It transforms any three or four-wire system into an equivalent space vector with the components: x_α, x_β, and x_0. These components are often interpreted in the complex domain, where x_α represents the real part and x_β the imaginary part. However, these components are instantaneous quantities in the time-domain in contrast to phasors. This interpretation extends the phasor theory to describe transient processes. The arbitrary three-phase system in 3.6 can be described in the $\alpha\beta$-domain as follows:

$$\mathbf{x}_{\alpha\beta 0} = \frac{1}{3}\begin{bmatrix} \Re\left\{\hat{X}_{\mathrm{Sabc},1}\mathrm{e}^{\mathrm{j}(\omega_1 t)} + \hat{X}_{\mathrm{Sabc},-1}\mathrm{e}^{\mathrm{j}(-\omega_1 t+\delta_{-1})} + \sum_{n=-m}^{m}\hat{X}_{\mathrm{Sabc},n}\mathrm{e}^{\mathrm{j}n(\omega_1 t+\delta_n)}\right\} \\ \Im\left\{\hat{X}_{\mathrm{Sabc},1}\mathrm{e}^{\mathrm{j}(\omega_1 t)} + \hat{X}_{\mathrm{Sabc},-1}\mathrm{e}^{\mathrm{j}(-\omega_1 t+\delta_{-1})} + \sum_{n=-m}^{m}\hat{X}_{\mathrm{Sabc},n})\mathrm{e}^{\mathrm{j}n(\omega_1 t+\delta_n)}\right\} \\ \Re\left\{\underline{x}_{\mathrm{a}} + \underline{x}_{\mathrm{b}} + \underline{x}_{\mathrm{c}}\right\} \end{bmatrix} \tag{3.12}$$

with

$$\hat{X}_{\mathrm{Sabc},1} = \hat{X}_{\mathrm{Sa},1} + \hat{X}_{\mathrm{Sb},1} + \hat{X}_{\mathrm{Sc},1} \quad , \tag{3.13}$$

$$\hat{X}_{\mathrm{Sabc},-1} = \hat{X}_{\mathrm{Sa},-1} + \hat{X}_{\mathrm{Sb},-1}\mathrm{e}^{-\mathrm{j}\frac{2\pi}{3}} + \hat{X}_{\mathrm{Sc},-1}\mathrm{e}^{\mathrm{j}\frac{2\pi}{3}} \quad , \tag{3.14}$$

$$\hat{X}_{\mathrm{Sabc},n} = \hat{X}_{\mathrm{Sa},n} + \hat{X}_{\mathrm{Sb},n}\mathrm{e}^{\mathrm{j}(n-1)\left(-\frac{2\pi}{3}\right)} + \hat{X}_{\mathrm{Sc},n}\mathrm{e}^{\mathrm{j}(n-1)\frac{2\pi}{3}} \quad . \tag{3.15}$$

The transformation matrix form depends on the chosen domain: First, the transformation matrix can be a complex matrix $\underline{\mathbf{T}}_{\alpha\beta}$ based on the Fortescue operator $\underline{a}$ (see 3.16 and 3.17). Symmetrical component decomposition uses a similar transformation in the abc-frame. The scaling factor of the transformation depends on the input vector definition. If the input is a phasor vector $\vec{\mathbf{x}}_{\mathrm{abc}}$, as in 3.16, then the factor must be 1/3. In contrast, the factor changes to 2/3, if the input quantities are time-domain vectors such as $\mathbf{x}_{\mathrm{abc}}$ in 3.6.

$$\underline{x}_{\alpha\beta} = x_\alpha + \mathrm{j}x_\beta = \frac{1}{2}\underline{\mathbf{T}}_{\alpha\beta}\vec{\mathbf{x}}_{\mathrm{abc}} = \frac{1}{3}\begin{bmatrix}1 & \underline{a} & \underline{a}^2\end{bmatrix}\vec{\mathbf{x}}_{\mathrm{abc}} \tag{3.16}$$

$$\underline{x}_{\alpha\beta} = \underline{\mathbf{T}}_{\alpha\beta}\Re\left\{\vec{\mathbf{x}}_{\mathrm{abc}}\right\} = \frac{2}{3}\begin{bmatrix}1 & \underline{a} & \underline{a}^2\end{bmatrix}\mathbf{x}_{\mathrm{abc}} \tag{3.17}$$

The second transformation matrix form splits real and imaginary parts of the complex transformation $\underline{\mathbf{T}}_{\alpha\beta}$ that leads to the real matrix $\mathbf{T}_{\alpha\beta0}$ with zero sequence components. Eq. 3.18 presents the matrix and its real output vector with the components x_α, x_β, and x_0. In this form, the scaling factor is independent of the chosen input quantity domain. The inverse transformation is given in appendix A.8.

$$\mathbf{x}_{\alpha\beta0} = \begin{bmatrix}x_\alpha\\ x_\beta\\ x_0\end{bmatrix} = \mathbf{T}_{\alpha\beta0}\Re\left\{\vec{\mathbf{x}}_{\mathrm{abc}}\right\} = \mathbf{T}_{\alpha\beta0}\mathbf{x}_{\mathrm{abc}} = \frac{2}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}\mathbf{x}_{\mathrm{abc}} \tag{3.18}$$

For now, the $\alpha\beta$ components are obtained, which are not decomposed into different sequences. Clarke's matrix $\mathbf{T}_{\alpha\beta0}$ can be combined with the symmetrical component decomposition matrices $\underline{\mathbf{T}}_{+}$ or $\underline{\mathbf{T}}_{-}$ (see 3.19 and 3.20) to derive the positive and negative sequence in the $\alpha\beta$-domain, respectively, as described by:

$$\underline{\mathbf{x}}^{+}_{\alpha\beta} = \frac{1}{3}\mathbf{T}_{\alpha\beta}\underline{\mathbf{T}}_{+}\mathbf{x}_{\mathrm{abc}} = \frac{1}{3}\mathbf{T}_{\alpha\beta}\underline{\mathbf{T}}_{+}\mathbf{T}^{-1}_{\alpha\beta}\mathbf{x}_{\alpha\beta} \quad , \tag{3.19}$$

$$\underline{\mathbf{x}}^{+}_{\alpha\beta} = \frac{2}{9}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}1 & \underline{a} & \underline{a}^2\\ \underline{a}^2 & 1 & \underline{a}\\ \underline{a} & \underline{a}^2 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ -\frac{1}{2} & \frac{\sqrt{3}}{2}\\ -\frac{1}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\mathbf{x}_{\alpha\beta} \quad . \tag{3.20}$$

Finally, a compact transformation matrix to calculate the positive sequence using $\underline{q}$ can be derived as follows [56], [52]:

$$\underline{\mathbf{x}}^{+}_{\alpha\beta} = \begin{bmatrix} \underline{x}^{+}_{\alpha} \\ \underline{x}^{+}_{\beta} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & -\underline{q} \\ \underline{q} & 1 \end{bmatrix} \begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix} \Rightarrow \qquad \mathbf{x}^{+}_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} 1 & -\Gamma(s) \\ \Gamma(s) & 1 \end{bmatrix} \mathbf{x}_{\alpha\beta} \quad . \tag{3.21}$$

The matrix given in 3.21 seems to enable straight-forward sequence decomposition but contains a severe problem during implementing $\underline{q}$ and interpreting the resulting $\underline{\mathbf{x}}^{+}_{\alpha\beta}$. Applying this time-lagging operator $\underline{q}$ to a phasor is simple, but x_{α} and x_{β} are components of a space-vector. Hence, the components $\underline{q}x_{\alpha}$ and $\underline{q}x_{\beta}$ should be interpreted as $T/4$-lagging signals to the original ones x_{α} and x_{β}. The time-shift of $T/4$ can be implemented with filter algorithms that can be described generically by a real transfer function $\Gamma(s)$ resulting in the real positive sequence components $\mathbf{x}^{+}_{\alpha\beta}$ according to 3.21. Unfortunately, the filter transfer characteristic alters the dynamic of the transformation, as discussed in chapter 5.
Once the positive sequence components $\mathbf{x}^{+}_{\alpha\beta}$ are obtained, the negative sequence quantities $\mathbf{x}^{-}_{\alpha\beta}$ can be simply derived by 3.22 and 3.23, and the zero sequence calculation is the same as for the abc-frame according to A.5. The further analysis and applied control schemes will show that it may be convenient to directly calculate the positive and negative sequence components in the $\alpha\beta$-frame.

$$\underline{\mathbf{x}}_{\alpha\beta} = \underline{\mathbf{x}}^{+}_{\alpha\beta} + \underline{\mathbf{x}}^{-}_{\alpha\beta} \tag{3.22}$$

$$\underline{\mathbf{x}}^{-}_{\alpha\beta} = \begin{bmatrix} \underline{x}^{-}_{\alpha} \\ \underline{x}^{-}_{\beta} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & \underline{q} \\ -\underline{q} & 1 \end{bmatrix} \mathbf{x}_{\alpha\beta} \Rightarrow \qquad \mathbf{x}^{-}_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} 1 & \Gamma(s) \\ -\Gamma(s) & 1 \end{bmatrix} \mathbf{x}_{\alpha\beta} \tag{3.23}$$

3.2.3 Positive, Negative and Zero-Sequence in dq-Frame

Park's transformation or dq-transformation is the third well-known analysis domain for three-phase systems and was invented in 1929 [57]. Nowadays, the domain is also called Synchronous Reference Frame (SRF). The abc or $\alpha\beta$ components are transformed into a rotating reference frame to obtain dc quantities for the fundamental frequency oscillation. This transformation is not linear unlike the Clarke transform and depends on the grid angle θ or frequency ω_1, respectively.
Two Park transformations exist: the complex definition has a compact form, using only the rotation operator $\mathrm{e}^{-\mathrm{j}\omega_1 t}$ in 3.24. However, the vast majority prefers the transformation with the real matrix $\mathbf{T}_{\mathrm{dq}}$ to derive the time-domain signals $\mathbf{x}_{\mathrm{dq0}}$ according to 3.25. The further description neglects the zero sequence since it is not necessary for this application background. The inverse transformation is given in A.8.

$$\underline{x}_{\mathrm{dq}} = x_{\mathrm{d}} + \mathrm{j}x_{\mathrm{q}} = \mathrm{e}^{-\mathrm{j}\omega_1 t}\underline{x}_{\alpha\beta} \tag{3.24}$$

$$\mathbf{x}_{\mathrm{dq0}} = \begin{bmatrix} x_{\mathrm{d}} \\ x_{\mathrm{q}} \\ x_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\omega_1 t) & \cos(\omega_1 t - \frac{2\pi}{3}) & \cos(\omega_1 t + \frac{2\pi}{3}) \\ -\sin(\omega_1 t) & -\sin(\omega_1 t - \frac{2\pi}{3}) & -\sin(\omega_1 t + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\mathbf{x}_{\mathrm{abc}} = \frac{2}{3}\mathbf{T}_{\mathrm{abc/dq0}}\mathbf{x}_{\mathrm{abc}} \tag{3.25}$$

In most applications, Clarke's and Park's transformation are used sequentially leading to the expression for fundamental frequency components:

$$\mathbf{x}_{\mathrm{dq0}} = \begin{bmatrix} \cos(\omega_1 t) & \sin(\omega_1 t) & 0 \\ -\sin(\omega_1 t) & \cos(\omega_1 t) & 0 \\ 0 & 0 & 1 \end{bmatrix}\mathbf{x}_{\alpha\beta 0} = \mathbf{T}_{\mathrm{dq0}}\mathbf{x}_{\alpha\beta 0} \quad . \tag{3.26}$$

The inverse transformation can be found in A.10. The SRF can also be extended to ISC decomposition by combining the sequence calculation in $\alpha\beta$-frame with the matrix $\mathbf{T}_{\mathrm{dq}}$, which leads to the positive and negative sequence quantities $\mathbf{x}^{+}_{\mathrm{dq}}$ and $\mathbf{x}^{-}_{\mathrm{dq}}$ in 3.27 and A.11.

$$\mathbf{x}^{+}_{\mathrm{dq}} = \begin{bmatrix} x^{+}_{\mathrm{d}} \\ x^{+}_{\mathrm{q}} \end{bmatrix} = \mathbf{T}_{\mathrm{dq}}\mathbf{x}^{+}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} \cos(\omega_1 t) & \sin(\omega_1 t) \\ -\sin(\omega_1 t) & \cos(\omega_1 t) \end{bmatrix}\begin{bmatrix} 1 & -\underline{q} \\ \underline{q} & 1 \end{bmatrix}\mathbf{x}_{\alpha\beta} \tag{3.27}$$

Another decomposition method focuses on how Park's transformation affects the positive and negative sequence components of the $\alpha\beta$-frame. Park's transformation works for different frequencies, and thus can lock on different grid voltage harmonics, e.g., $\mathbf{T}_{\mathrm{dq}^n}$ denotes the matrix locked on the n-th harmonic. Symmetry exists between positive and negative frequencies of the same order according to:

$$\mathbf{T}_{\mathrm{dq}^{+\mathrm{n}}} = \left(\mathbf{T}_{\mathrm{dq}^{-\mathrm{n}}}\right)^{\mathrm{T}} \quad , \tag{3.28}$$

$$\mathbf{T}_{\mathrm{dq}^{+\mathrm{n}}}\mathbf{T}_{\mathrm{dq}^{-\mathrm{n}}} = \mathbf{T}_{\mathrm{dq}^{+\mathrm{n}}}\mathbf{T}^{\mathrm{T}}_{\mathrm{dq}^{+\mathrm{n}}} = \mathbf{1} \quad . \tag{3.29}$$

This symmetry helps to split the different frequency components of 3.6 into the corresponding components in the SRF. The components of $\mathbf{x}_{\mathrm{dq}}$ contain positive sequence ($\mathbf{x}^{+}_{\mathrm{dq}}$), negative sequence ($\mathbf{x}^{-}_{\mathrm{dq}}$), and harmonic components ($\mathbf{x}^{n}_{\mathrm{dq}}$). If the time-domain input is transformed, all these components experience a frequency shift. Only harmonics with the same frequency as Park's transformation lead to a dc output such as $\overline{\mathbf{x}}^{+}_{\mathrm{dq}+}$. Notably, the negative sequence components have negative frequencies due to the opposite rotation direction. Hence, the

negative or positive sequence quantity appears as double fundamental frequency oscillation after applying $\mathbf{T}_{\mathrm{dq}}$ according to:

$$\begin{aligned}\mathbf{x}_{\mathrm{dq}^+} = \mathbf{T}_{\mathrm{dq}}\mathbf{x}_{\alpha\beta} &= \mathbf{T}_{\mathrm{dq}}\mathbf{x}^+_{\alpha\beta} + \mathbf{T}_{\mathrm{dq}}\mathbf{x}^-_{\alpha\beta} + \sum_{n=-m}^{m} \mathbf{T}_{\mathrm{dq}}\mathbf{x}^n_{\alpha\beta} \\ &= \overline{\mathbf{x}}^+_{\mathrm{dq}} + \mathbf{T}_{\mathrm{dq}}\mathbf{T}^{\mathrm{T}}_{\mathrm{dq}^{-1}}\overline{\mathbf{x}}^-_{\mathrm{dq}^+} + \sum_{n=-m}^{m} \mathbf{T}_{\mathrm{dq}}\mathbf{T}^{\mathrm{T}}_{\mathrm{dq}^n}\overline{\mathbf{x}}^n_{\mathrm{dq}^+} \\ &= \overline{\mathbf{x}}^+_{\mathrm{dq}} + \mathbf{T}_{\mathrm{dq}^{+2}}\overline{\mathbf{x}}^-_{\mathrm{dq}} + \sum_{n=-m}^{m} \mathbf{T}_{\mathrm{dq}^{(1-n)}}\overline{\mathbf{x}}^n_{\mathrm{dq}} \quad . \end{aligned} \tag{3.30}$$

The transformation can also be based on $\mathbf{T}_{\mathrm{dq}^{-1}}$ leading to the relations for $\mathbf{x}_{\mathrm{dq}^-}$ presented in A.12. Finally, the vector from 3.6 is transformed to highlight the output characteristics of Park's transformation, see 3.31 and A.13. Again, the fundamental frequency part manifests as dc-component $\overline{\mathbf{x}}^+_{\mathrm{dq}+}$, whereas other harmonics, i.e., $\mathbf{x}^-_{\mathrm{dq}+}$ and $\mathbf{x}^n_{\mathrm{dq}+}$, change their frequency according to 3.30 with $n \in \mathbb{Z}\backslash\{-1;1\}$. The presented algorithm in section 5 exploits these characteristics to obtain the sequence information.

$$\begin{aligned}\mathbf{x}^+_{\mathrm{dq}} = \mathbf{T}_{\mathrm{dq}}\left(\mathbf{x}^+_{\mathrm{abc}} + \mathbf{x}^-_{\mathrm{abc}}\right) &= \underbrace{\hat{X}_{\mathrm{S},1}\begin{bmatrix}\cos(\delta)\\ \sin(\delta)\end{bmatrix}}_{\overline{\mathbf{x}}^+_{\mathrm{dq}+}} \\ &+ \underbrace{\hat{X}_{\mathrm{S},-1}\begin{bmatrix}\cos(-2\omega_1 t + \delta + \delta_{-1})\\ \sin(-2\omega_1 t + \delta + \delta_{-1})\end{bmatrix}}_{\mathbf{x}^-_{\mathrm{dq}+}} + \underbrace{\sum_{n=-m}^{m} \hat{X}_{\mathrm{S},n}\begin{bmatrix}\cos((n-1)\omega_1 t + \delta + \delta_n)\\ \sin((n-1)\omega_1 t + \delta + \delta_n)\end{bmatrix}}_{\mathbf{x}^n_{\mathrm{dq}+}}\end{aligned} \tag{3.31}$$

In summary, the section presented the symmetrical components based on the phasor theory to analyze and model arbitrary three-phase systems accurately. Furthermore, different reference frames can describe unbalanced three-phase systems with space vectors. Space vectors enable the analysis and control to handle transient processes by using time-domain measurements as input.

3.3 Grid Voltage Characteristics and Faults

The normal operation of ac power systems is characterized by the grid voltage magnitude and frequency that vary in a narrow tolerance band around the nominal values [12], [13], [58], as already discussed in section 3.1.1. During the abnormal state, the voltages leave this tolerance band typically due to grid faults that are mainly caused by failing of transmission lines or substations [59]. The fault characteristics mainly depend on the affected phases, grid

configuration, location, SCR, and the grounding scheme [43] that leads to various possible fault types defined in [45], [52]. The fault location predominantly affects the impact of the fault on generation units. If the fault occurs on the generator feeder, the generator will likely trip and no further control strategies are necessary. Faults more distant from the generator require grid support to quickly recover the voltages and return to normal operation. This scenario is called Fault Ride-Through (FRT) and is critical for the generator hardware and control, due to the wide operating range and severe transient processes.
Depending on the fault scenario, grid codes may require FRT of generators for up to 1.5 s before they may disconnect [58]. During this time, fault detection mechanisms identify the faulty phase and try to localize the fault based on detecting an overcurrent. Therefore, it is important that generation units inject their maximum current during faults. Fuses will trip due to these overcurrents and will disconnect faulty feeders. Typical fault-clearing times depend on the protective device and vary from 10 ms up to 1 s [45, p.168].
The fault statistics show that single-phase faults have the highest occurrence probability and fault durations vary in the range of tens of milliseconds to several seconds with decreasing voltage sag depth [43]. However, the converter and its control must handle all different fault types according to several standards [12], [13], [58]. In most cases, YNd-transformers connect the generation units with the faulty feeder that leads to fault transformation, e.g., single-phase faults transform to phase-to-phase faults [43], [44]. Consequently, phase-to-phase faults are the most frequent faults occurring at the terminals of RES converters.

The remainder of this section is organized as follows: first, the different fault types and configurations are analyzed. Second, FRT regulations are discussed to derive operational scenarios and requirements for the converter control and hardware. The last part focuses on the voltage harmonics in the grid voltage, which affect the magnitude, phase, and sequence calculation covered in section 5.

3.3.1 Definition and Characterization of Fault Types

A fault impedance $\underline{Z}_\mathrm{F}$ and neutral connection extend the three-phase voltage system to model the impact of short circuits in power systems. The source impedance $\underline{Z}_\mathrm{S}$ forms a voltage divider with $\underline{Z}_\mathrm{F}$ that describes the PCC-voltages $v_\mathrm{a,PCC}$, $v_\mathrm{b,PCC}$, and $v_\mathrm{c,PCC}$ during short-circuit events (Fig. 3.5). During the normal state, the fault impedance does not affect the system due to the open circuit.
Fig. 3.5 shows different short circuit events, indicated with lightning symbols. Based on symmetrical components theory, the equivalent circuit of the short circuit is divided into its sequence components to characterize the voltage divider in steady-state. This model assumes that the impedance in the positive and negative sequence are equal, load currents are zero, and the zero-sequence component does not propagate to the terminal voltage of loads or RES

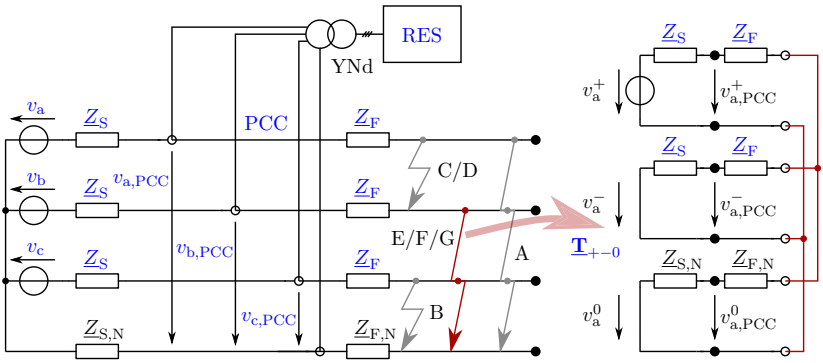


Figure 3.5: Equivalent circuit of an exemplary power system with a RES in abc-frame during different line faults with symmetrical components representation for a two-phase-to-ground fault.

due to the transformer configuration [45, p.187]. The grid voltage source does not contain negative nor zero sequence components, i.e.,$\vec{\mathbf{v}}_{\mathrm{abc}} = \vec{\mathbf{v}}^{+}_{\mathrm{abc}}$.

The symmetrical component model in Fig. 3.5 enables the calculation of phase voltage phasors during faults. Several references already presented these calculations extensively [45, pp.174-187], [52], [60]. Thus, fault voltages are only derived exemplary for a two-phase-to-ground fault (type E fault) to present the fundamental methodology and to introduce the definitions and notations that are used throughout the thesis. Two parameters essentially determine fault voltages. First, the voltage divider formed by $\underline{Z}_{\mathrm{S}}$ and $\underline{Z}_{\mathrm{F}}$ is described by the characteristic voltage factor $\underline{D}$ proposed in [52], [61]. For integrity in this thesis, but in contradiction to [52], $\underline{D}$ is complex and not a phasor. $\underline{D}$ for type E faults is given by

$$\underline{D} = \frac{\underline{Z}_{\mathrm{F}}}{\underline{Z}_{\mathrm{F}} + \underline{Z}_{\mathrm{S}}} \quad . \tag{3.32}$$

The second crucial parameter to describe fault voltages is the voltage unbalance factor VUF:

$$VUF = \frac{\hat{V}^{-}_{\mathrm{a}}}{\hat{V}^{+}_{\mathrm{a}}} \quad . \tag{3.33}$$

It represents the ratio between negative and positive sequence voltage at the PCC [62]. In normal operation, this factor is lower than 0.03 pu and increases during unbalanced faults up to 1 pu [58].

The final expressions for the PCC voltages, presented in 3.34 and 3.35, describe voltage phasors in the Gauss plane according to [52, p.178]. The voltage vector $\vec{\mathbf{v}}^{+-0}_{\mathrm{a,PCC}}$ contains the voltages of phase a in the positive, negative, and zero sequence, whereas $\vec{\mathbf{v}}_{\mathrm{abc,PCC}}$ consists of the voltage phasors for all three phases (a, b, c). The magnitude of $\underline{D}$ corresponds to the sag depth of the positive sequence voltage, whereas the phase of $\underline{D}$ determines the phase

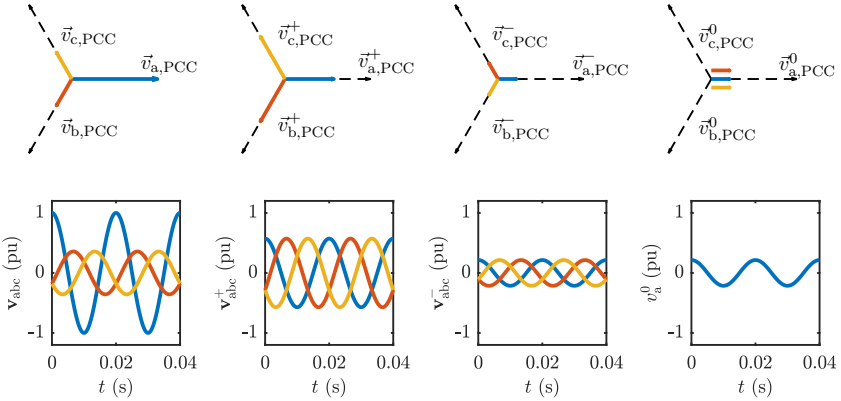


Figure 3.6: Sequence phasors of voltage sag type E and corresponding time-domain waveform with $|\underline{Z}_F|$=0.5 pu and $|\underline{Z}_S|$=0.9 pu and $\angle\underline{Z}_S$=$\angle\underline{Z}_F$ (without phase jump).

jump. The phase jump is zero if the impedance ratio X/R is the same before and during the fault. The impedance ratio may change significantly if faults propagate across different voltage levels (see Table 3.1).

$$\vec{\mathbf{v}}^{+-0}_{a,PCC} = \frac{1}{3}\begin{bmatrix} 1+2\underline{D} & 1-\underline{D} & 1-\underline{D} \end{bmatrix}^{T} \vec{v}_a \tag{3.34}$$

$$\vec{\mathbf{v}}_{abc,PCC} = \begin{bmatrix} 1 & \underline{a}^2\underline{D} & \underline{a}\ \underline{D} \end{bmatrix}^{T} \vec{v}_a \tag{3.35}$$

Fig. 3.6 presents the results for the type E fault with $|\underline{Z}_F|$=0.5 pu and $|\underline{Z}_S|$=0.9 pu. Three balanced systems in positive, negative, and zero sequences accurately describe the unbalanced three-phase fault voltages. The time-domain waveforms result from the real parts of the presented phasors.
Based on this methodology, Bollen [45] categorizes the grid faults into six basic voltage sag types:

- Type A: three-phase fault (balanced)
- Type B: single-phase-to-ground fault
- Type C/D: phase-to-phase fault (star/ delta connection)
- Type E/F: two-phase-to-ground fault (star/delta connection)

As already presented, the terminal connection in delta or star and transformer winding configurations affect the fault propagation to the utility terminals [45, p.187]. Note that the clock number of the transformer does not affect the sag type in any case [45, p.190]. The

Table 3.2: Fault propagation through transformers and corresponding fault type transformation [45, p.197].

Transformer	A	B	C	D	E	F	G
Yd or Dy	A	C	D	C	F	G	F

fault propagation through transformers adds another sag type, leading to seven different types of voltage sags in total. The type G occurs during a type E or type F fault depending on the number of the passed transformers. Two cases are possible:

- Type G (case 1): Type F fault at the low voltage terminals of Yd or Dy transformers
- Type G (case 2): Type E fault at the low voltage terminals of Yd or Dy transformers after passing another Yd or Dy transformer

The further analysis only considers YNd-transformers, and the Table 3.2 summarizes how this configuration transforms the fault types. An overview of the voltage phasors is presented in Fig. 3.7.

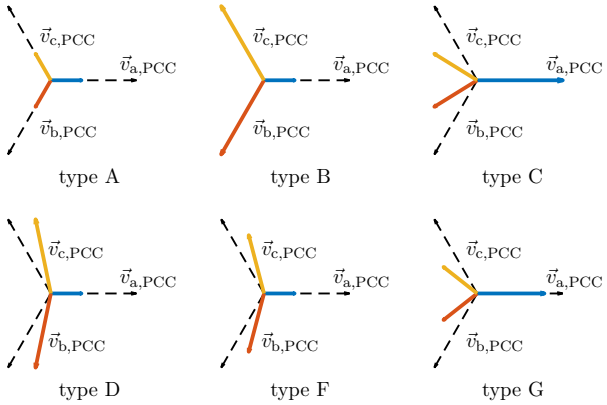


Figure 3.7: Phasors of voltage sag types A-D, F and G with $|\underline{Z}_F|$=0.5 pu and $|\underline{Z}_S|$=0.9 pu and $\angle\underline{Z}_S=\angle\underline{Z}_F$ (without phase jump).

For power system operation and monitoring, Fast Fourier Transformation (FFT)-based algorithms typically categorize fault types by online measurements. Different algorithms are feasible to achieve this. Most of them use an analysis window or cycle to derive Root-Mean-Square (RMS) values of the fundamental frequency components of voltages and currents [63]. Recent approaches apply enhanced methods like ellipse parameter extraction or deep learning algorithms based on phasor representations [64], [65]. All of them rely on RMS quantities in a predefined monitoring cycle. These RMS-based algorithms are often not sufficient

for converter control that needs instantaneous voltages and currents. Therefore, online sequence decomposition relies on closed-loop algorithms such as PLLs, which are discussed in chapter 5.

3.3.2 Fault Ride-Through (FRT)

Fault Ride-Through (FRT) is the converter ability to stay connected to the grid during fault events. Several grid codes define the corresponding voltage profiles and how RES converters should react during grid faults, which are critical for converters and their control due to severe voltage transients, the wide voltage operating range, power oscillations, and high currents. But which fault scenarios must be considered? So far, the fault categorization given in section 3.3.1 does not address durations and fault profiles over time in detail.
Bollen proposes a segmentation to describe fault events and defines five different segments [61]. The fault starts with the pre-event segment (I), which defines the pre-fault voltages, and ends with the voltage-recovery segment (V) or post-fault operating point, respectively. Two transition segments occur during fault initiation (II) and clearing (IV). The time period where the fault voltages defined in section 3.3.1 are in steady-state is called during-event segment (III). These characteristics are summarized in Fig. 3.8 for an arbitrary fault scenario.
Grid codes define RMS voltage profiles for the fault segments considering the positive sequence voltage $\hat{V}_{\mathrm{a}}^{+}$ normalized to the nominal grid voltage $\hat{V}_{\mathrm{a,n}}$ [12], [11], [58], [66] [43]. Fig. 3.9 summarizes the different regulations exemplary for the German transmission grid, including the BDEW 2008 Code [12] and the VDE AR-N-4110 [11]. The converter-based generation units must stay connected to the grid for voltages above the given voltage ratio profile. Moreover, they must guarantee stable operation in the faulty network and must support the grid voltage with reactive current [12], [11]. The standard in [12] provides two boundaries: The first one is mandatory (nec.), and the grid operator can require the second one (tbd.) if necessary. The most recent grid code in Germany even distinguishes between three-phase faults (3-ph) and phase-to-phase faults (2-ph) to guarantee specific system support [11].
The grid codes differ significantly in the minimum grid voltage that is acceptable during the first fault segment. The ENTSO-E standard [13] defines voltage drops down to 0.05 pu and the VDE down to 0.15 pu. The strictest standard is the BDEW [12] because it demands a stable operation down to 0 pu. This scenario is critical for voltage detection and control since there is no voltage system to synchronize on. All these events represent the scenarios for Low-voltage Ride-Through (LVRT). The High-Voltage Ride-Through (HVRT) includes overvoltages at the PCC that are particularly challenging for converter systems, due to the fixed dc-link voltage and the critical blocking voltage of the semiconductor switches. The corresponding voltage profile is also shown in Fig. 3.9.
In summary, fault categorization in steady-state and the grid code requirements define the operational scenario for the converter during FRT. Furthermore, several grid codes require converters to support the voltage at the PCC by injecting reactive current in the

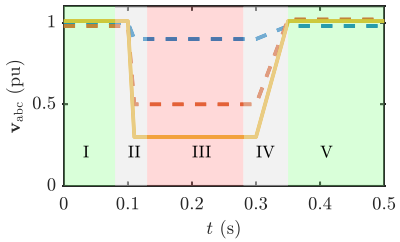


Figure 3.8: Transient process of exemplary fault with time segment definitions: I - pre-event; II - transient; III - during-event; IV - transient; V - voltage recovery [61].

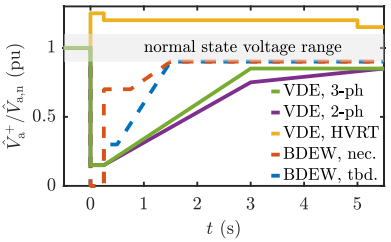


Figure 3.9: FRT requirements defined in different grid codes. (nec. - necessary, tbd. - to be determined)

positive sequence [12], [11], [13], [58]. This support strategy works mainly for inductive line impedances and balanced faults as derived in section 7. However, this assumption is not valid for all grid types, as shown in Table 3.1, and does not consider unbalanced faults. Current grid codes in Germany provide requirements for injecting reactive current in the negative sequence [11], which decreases the negative sequence voltage or VUF in inductive grids, respectively. Fig. 3.10 presents the relation between voltage drop and demanded reactive current $\hat{I}_{a,Q}^+$ considering an active current $\hat{I}_{a,P}^+$ and rated current $\hat{I}_{a,r}$ according to 3.36-3.38. Moreover, some grid codes provide a dead-band of 10% around the nominal grid voltage $\hat{V}_{a,n}^+$, where no reactive current should be injected [43].

$$\hat{I}_{a,Q}^+ = \begin{cases} k^+ \hat{I}_{a,r} & k^+ > -0.5 \text{ pu} \\ \hat{I}_{a,r} & k^+ < -0.5 \text{ pu} \end{cases} ; \; k^+ = \frac{\hat{V}_a^+ - \hat{V}_{a,n}^+}{\hat{V}_{a,n}^+} \tag{3.36}$$

$$\hat{I}_{a,Q}^- = \begin{cases} k^- \hat{I}_{a,r} & k^- > 0.5 \text{ pu} \\ \hat{I}_{a,r} & k^< - 0.5 \text{ pu} \end{cases} ; \; k^- = \frac{\hat{V}_a^-}{\hat{V}_{a,n}^+} \tag{3.37}$$

$$\hat{I}_{a,r} \geq \sqrt{\left(\hat{I}_{a,Q}^+\right)^2 + \left(\hat{I}_{a,P}^+\right)^2} + \hat{I}_{a,Q}^- \tag{3.38}$$

Additionally, grid operators may require frequency support, as shown in Fig. 3.11. In order to support the grid frequency, the active power must be adjusted depending on the deviation of the fundamental frequency [11]. Generation units with storage capabilities above $30 \text{ s} \cdot P_r$, where P_r is the rated converter power, are engaged to inject active power if the frequency is too low [11]. In summary, all of the presented requirements focus on the grid support during small and large deviations from the nominal voltage or frequency operating point of the power system.

Almost every grid code provides steady-state requirements for FRT operation, but most of them do not address transient characteristics in detail. Some grid codes, i.e. [11], [13], [67], provide maximum settling times for step responses of the reactive and active current

during faults. There, the maximum settling time of 60 ms for the reactive current in a 10% tolerance band is required to limit the voltage drop at the PCC [11], [13, p.15], [67, p.18]. After fault clearing, the reactive current should decrease to its pre-fault value as fast as possible to prevent overvoltages at the PCC. These dynamic requirements demand fast and robust control algorithms for a great variety of fault scenarios.

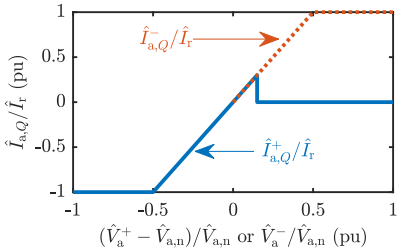


Figure 3.10: Reactive current support for the positive and negative sequence voltage.

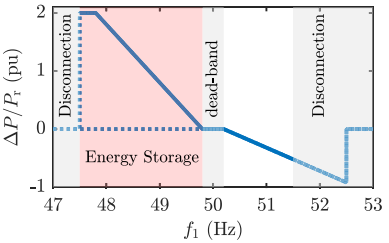


Figure 3.11: Active current support for frequency deviations.

3.3.3 Grid Operating Range and Voltage Harmonics

In absence of faults, grid voltages only vary in a narrow band but may contain harmonics that critically affect the converter control. The harmonics highly depend on the characteristics of real loads and sources, but IEEE519 [68] or EN50160 [38] provide limits for voltage harmonics, which are summarized in Table 3.3 [38] [52, p.35]. The harmonics not just differ in their frequency, but occur in a balanced three-phase system in positive (n^+), negative (n^-) and zero sequences (n^0) as defined in [69, p.195]. The allocation of the single harmonics in positive, negative, and zero sequences is much more complex for unbalanced systems [69]. Therefore, the following analysis assumes the sequence categorization of the n-th harmonic according to 3.39 (see Table 3.3), which is valid for balanced grid voltages. To the best of the author's knowledge, a detailed description of the harmonics during abnormal state or FRT is not available.

$$n^0 = 3n; \qquad n^+ = 3n - 2; \qquad n^- = 3n - 1, \quad n \in \mathbb{Z}_{>0} \tag{3.39}$$

The magnitude and frequency of the positive sequence voltage define the steady-state operating point of the grid. They are typically in the range of:

$$\hat{V}^+_a = \{0, 0.05, 0.15\}...1.25\ \hat{V}^+_{a,n} \text{ and } 47.5 \text{ Hz} < f_1 < 51.5 \text{ Hz} \quad . \tag{3.40}$$

in German power systems considering faults [38]. These operating ranges are valid for other power systems with just minor changes. In addition to the positive sequence voltage operating

Table 3.3: Limits of voltage harmonics of low and medium voltage grid (EN 50160) with corresponding sequence [38].

Odd harmonics				Even harmonics	
Not Multiples of 3		Multiples of 3			
n-th harmonic	voltage / pu	n-th harmonic	voltage / pu	n-th harmonic	voltage / pu
5 (-)	0.060	3 (0)	0.050	2 (-)	0.02
7 (+)	0.050	9 (0)	0.015	4 (+)	0.01
11 (-)	0.035	15 (0)	0.005	6(0), 8(-), 10(+) ... 24(0)	0.005
13 (+)	0.03	21 (0)	0.005		
17 (-)	0.02				
19 (+)	0.015				
23 (-)	0.015				
25 (+)	0.015				

point, large negative sequence voltages occur in the grid according to the fault types. The major challenge for RES-converters and their control is to handle these diverse operational scenarios without tripping and simultaneously supporting grid voltages and frequency.

3.4 Feedback Control for Grid Converters

The main task of grid converters is to inject active and reactive power respecting power quality regulations. Various control structures are proposed in the literature to achieve desired power characteristics and auxiliary control objectives. The vast majority of grid converters rely on feedback control that guarantees stable steady-state operation and fast dynamics. The advantages of feedback control or closed-loop control systems, respectively, in comparison to open-loop control is the low steady-state control error and low sensitivity to control plant uncertainties [70], [71].

Voltage Oriented Control (VOC) is a typical approach for grid converter control to inject power according to a given reference into the grid [72], [52]. This control type is often referred to as grid-following control since it synchronizes to the grid voltage and injects the current necessary to achieve the desired power reference. Therefore, it consists of a current control with Phase-Locked Loop (PLL). Moreover, the control scheme often contains MPPT for PV-systems or wind farms. Unfortunately, it often lacks grid support and affects the stability of power electronic dominated grid parts.

Due to this drawback of VOC, grid-forming control was proposed to control the voltage at the PCC and to realize islanded operation. Additionally, this control scheme may stabilize multiple generators in larger grid topologies and enhances the power-sharing between the generator units. Droop control is a typical control scheme for grid-forming converters [73]. In addition to droop control, the swing equation of synchronous generators may be implemented in grid-forming units. These algorithms are called Virtual Synchronous Generators (VSGs) and provide virtual inertia to enhance stability in comparison to the conventional droop control, particularly, in weak grids [74], [75].

Most of these control schemes rely on auxiliary voltage or current controls that may contain additional structures (e.g., feed-forwards, virtual impedances) to enhance their performance. The primary question arises, how to realize a feedback controller that accomplishes accurate control of the converter current or capacitor voltage. State-of-the-art controllers are Proportional-Resonant (PR) and Proportional-Integral (PI)-controllers. Additionally, some approaches utilize Proportional (P)- or hysteresis controllers for inner current loops. Because of their wider dissemination, PR- and PI-controllers are analyzed in detail. This section presents the control schemes that are analyzed and implemented throughout this thesis.

3.4.1 Voltage Oriented Control with PI- and PR-controllers

VOC typically operates in the $\alpha\beta$-domain or SRF to control the converter currents. It relies on the grid voltage measurement $\mathbf{v}_{\mathrm{PCC}}$. By knowing the grid voltage magnitude $\hat{V}_{\mathrm{S}}$ and its angle θ, the control can accurately inject active and reactive power into the grid by controlling the converter's output currents. In most VOC applications, PLLs are used to determine $\hat{V}_{\mathrm{S}}$ and θ. Different controllers may be suitable, such as PI-controllers or PR-controllers, to realize the control in the $\alpha\beta$ or SRF. These controllers are introduced and discussed briefly in the following sections.

Controllers in SRF with PI-Controllers

VOC in SRF contains a PLL, Clarke transformations, Park transformations, two PI-controllers, and a saturation block, as shown in Fig. 3.12. The PLL estimates the grid angle θ that is necessary to perform the Park transformation $\mathbf{T}_{\mathrm{dq}}$ in 3.25. $\mathbf{T}_{\mathrm{dq}}$ transforms the voltage components with the fundamental frequency ω_1 into dc-components. Thus, two PI-controllers can be used to control the converter current $\mathbf{i}_1$. The PI transfer function presented in 3.41 guarantees infinite gain at 0 Hz, which leads to the desired zero steady-state control error for dc-quantities.

$$G_{\mathrm{PI}} = k_{\mathrm{p}} + k_{\mathrm{i}}\frac{1}{s} \tag{3.41}$$

The controller output is the converter voltage $\mathbf{v}^*_{\mathrm{conv}}$, which is limited depending on the maximum dc-link voltage V_{dc} and forwarded to the modulator. A feed-forward of the filter capacitor voltage $\mathbf{v}_C$ improves the dynamics during grid voltage transients. This basic structure is extendable with a power control by calculating $\mathbf{i}^*_{\mathrm{dq}}$ from the power references. These calculations are extensively discussed in chapter 6.
This control structure cannot sufficiently deal with unbalanced three-phase systems, making it vulnerable to unbalanced grid faults. The control in the DSRF with four PI-controllers for the dq-currents in positive and negative sequence can solve this problem [76], [52]. Unfortunately, the DSRF current control shows slow dynamics during severe grid faults, as will be shown in chapter 6.

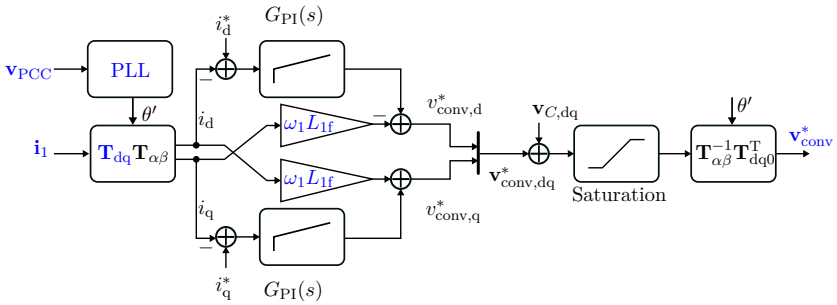


Figure 3.12: VOC in dq-frame with PLL, two PI-controller, and $\mathbf{v}_C$ voltage feed-forward.

Controllers in $\alpha\beta$-Frame with Proportional-Resonant PR-Controllers

VOC can also operate in $\alpha\beta$-frame by utilizing Clarke's transformation and two PR-controllers. The PR-controller can control sinusoidal signals with zero steady state error at defined frequencies. The transfer function is shown in 3.42 and contains a proportional gain k_{p}, and the resonant part with k_{i} tuned to the fundamental grid frequency ω_1. The rest of the control structure is similar to VOC in dq-frame, as shown in Fig. 3.13. For VOC in $\alpha\beta$-frame, the PLL only transforms the reference values into the dq-frame to determine i_{d}^* and i_{q}^*. If the reference values were calculated in $\alpha\beta$-frame, the PLL would not be necessary.

$$G_{\mathrm{PR}} = k_{\mathrm{p}} + k_{\mathrm{i}} \frac{s}{s^2 + \omega_1^2} \tag{3.42}$$

Since the PR-controller can track sinusoidal signals, it can intrinsically deal with unbalanced grid voltages. This capability is the main advantage in comparison to the PI-controller. But in contrast to the PI-controller, the PR-controller cannot intrinsically track signals with varying frequency. For this problem, two solutions exist: first, the quasi-PR controller with an additional damping term can be used to adjust the bandwidth of the gain peak. Second, a frequency-adaptive PR-controller can be applied. The first approach has the advantage of limited complexity but shows only accurate tracking in a small frequency band [77]. The second approach guarantees sufficient signal tracking in a wide frequency range but introduces more complex dynamics caused by the frequency feedback [78]. At first sight, the PR-controller may be the better choice to control unbalanced systems. However, PI-controller and PR-controller both have advantages and extensions to overcome their drawbacks, so their performance, especially during unbalanced grid scenarios is discussed in chapter 6.

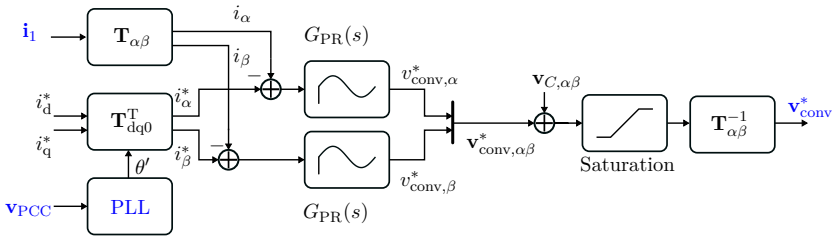


Figure 3.13: VOC in $\alpha\beta$-frame with PLL, two PR-controller, and $\mathbf{v}_C$ voltage feed-forward.

3.4.2 Grid-forming Converter Control: Droop-Control

VOC depends on the grid voltage detection and therefore shows critical instability mechanisms under weak grid conditions. Hence, grid stiffness is crucial to operate converters with VOC reliably. The grid-forming control overcomes the VOC's drawbacks under weak grid conditions and is able to form a grid. Originally, most of these converter control schemes were invented for microgrids [79], but they are also applicable for grid support in larger power systems. Controlling the converter output voltage instead of the converter current is the main feature to realize grid-forming characteristics. In most applications, an additional power control improves power-sharing and grid support.
Cascaded voltage and current control ensures accurate control of converter output voltages [80]. The structure is shown in Fig. 3.14 and is particularly advantageous for converters with *LCL*-filters since it splits up the control plant to achieve better dynamic performance and stability. Moreover, the low-level current control can sufficiently limit the converter current. The cascaded control operates in SRF or $\alpha\beta$-frame with PI-controllers or PR-controllers, respectively [80]. A crucial restriction of this scheme is the requirement that the voltage control loop is approximately ten times slower than the current control, but most systems can meet this requirement.

Based on an accurate voltage control, droop control is a well-known concept for power-sharing between different generation units [81], [79], [82]. Originally used in synchronous generators for power plants, it can be adapted to converters considering the inductive line impedance as the control plant. Assuming two voltage sources with the magnitudes $\hat{V}_\mathrm{S}^+$ and $\hat{V}_C^+$ and a angle difference of δ^+ that are connected by an inductive line impedance $\omega_1 L_\mathrm{S}$ lead to the following expressions for the exchanged power:

$$P = \frac{\hat{V}_\mathrm{S}^+ \hat{V}_C^+}{\omega_1 L_\mathrm{S}} \delta^+ \sim \delta^+ \quad , \qquad Q = \frac{\hat{V}_\mathrm{S}^+ \hat{V}_C^+ - (\hat{V}_\mathrm{S}^+)^2}{\omega_1 L_\mathrm{S}} \sim \hat{V}_C^+ \quad . \tag{3.43}$$

These characteristics indicate that the active power P predominantly depends on the angle difference δ^+ of the converter voltage V_C^+ and grid voltage V_S^+. In contrast, the reactive

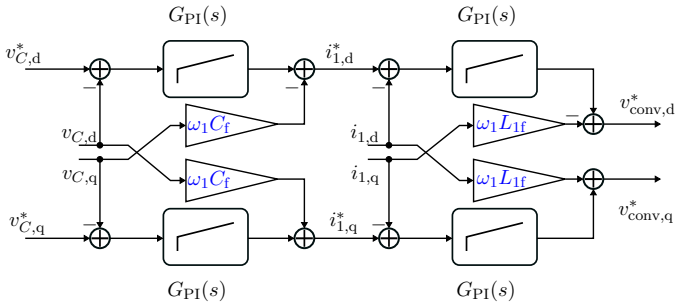


Figure 3.14: Cascaded voltage control in dq-frame.

power Q mainly depends on the converter voltage magnitude $\hat{V}_C^+$. The main objective for power-sharing can be summarized as follows:

$$P_\mathrm{S} \approx \sum_{n=1}^{\infty} \frac{P_{\mathrm{r},n}}{d_{P,n}} \quad , \qquad Q_\mathrm{S} \approx \sum_{n=1}^{\infty} \frac{Q_{\mathrm{r},n}}{d_{Q,n}} \quad . \tag{3.44}$$

The overall grid power P_S and Q_S should be equally supplied by $n-$generators according to their rated power $P_{\mathrm{r},n}$, or $Q_{\mathrm{r},n}$, respectively. The droop coefficients d_P and d_Q adjust the power sharing between the generators. The plant characteristics in 3.43 and the control objective in 3.44 define the control law to calculate the reference voltage magnitude $\hat{V}_C^{+*}$ and the corresponding angle δ^{+*} according to:

$$\hat{V}_C^{+*} = \hat{V}_{C,\mathrm{n}}^{+} + d_Q^+ \left(Q_\mathrm{r}^+ - Q^+ \right) \quad , \tag{3.45}$$

$$\delta^{+*} = \int \left(\omega_\mathrm{n}^+ + d_P^+ \left(P_\mathrm{r}^+ - P^+ \right) \right) \mathrm{d}t \quad . \tag{3.46}$$

Based on these relations, the well-known control scheme in Fig. 3.15 is derived. The control structure consists of the power calculation and P-controllers. Additional low-pass filters G_F adjust the control speed and immunity to distortions. Droop control may show a lack of inertia if low-pass filters are not included [83], which is not of practical relevance. The cut-off frequency of the filter and droop coefficients determine the stationary and dynamic characteristics of the power droop. Typically, the low-pass filter frequency is in the range of 1-10 Hz and does not affect the cascaded voltage and current control [3]. The droop coefficients depend on the grid requirements, but alter the system stability during transients. Hence, the design is not straight-forward and depends on the operational scenarios. A detailed discussion on the droop control parameter design and its performance during unbalanced faults is given in chapter 7.

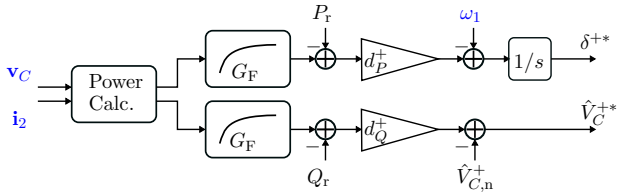


Figure 3.15: Droop control with power calculation and LPFs.

3.4.3 Peak Current and Peak Voltage Limitation with Anti-Windup

Current and voltage limitation alter the control characteristics of the converter significantly. However, these limitations are crucial for preventing converter damage. The peak phase currents should not exceed the maximum current defined by the power semiconductors. This phase current limitation requires accurate control of positive and negative sequence currents. If the control is not able to handle positive and negative sequences, the converter may exceed its safety current limits [84].

There are two basic limitation ideas: first, the Peak Current Limitation (PCL) simply limits the phase current reference to the maximum current. This method, in combination with a fast current control, sufficiently limits the current for any transient process but gives rise to low-frequency harmonics due to clipping of the waveform [10]. In order to overcome this problem of the PCL, the second method, which is labeled here as Vector Current Limitation (VCL), prevents clipping by limiting the fundamental frequency component of the current [85], [86], [87], [3], [10], [88]. Particularly in unbalanced cases, the detection of the fundamental components introduces some delay that leads to short periods of unlimited current during severe transient processes [16].

These limitation methods are applicable for VOC, but if additional control layers are involved, they may lead to unstable characteristics. Hence, limiting the current with a virtual impedance may solve these problems because it prevents current saturation from the controller point of view [87], [3], [89], [90]. However, the virtual impedance-based limitation changes the reference currents during normal operation, which may be unacceptable in some applications. Adjusting the references of the outer control loops may correct these steady-state errors. A solution is proposed in [31], but it only focuses on balanced faults.

In most applications, a saturation block tuned to the maximum values realizes the limitation of the controller output. The limitation affects the control characteristics in two different ways: First, it changes the dynamics in comparison to the dynamics without limitation, which typically slows down the step response. Second, the controller partly looses control over the plant, leading to integrator windup since control errors do not converge to zero. An anti-windup structure compensates the impact of the saturation on the integrator and

prevents the controller from winding up. Exemplary, a PI-controller with anti-windup is shown in Fig. 3.16. The limited quantity u_{sat} is compared to the controller output u and fed back to the integrator input [91, p.80]. The anti-windup is only active if u exceeds the limit of the saturation block and then manipulates the integrator input accordingly. The reset time of the integrator T_{aw} is derived in 3.47 and can be adjusted by the factor k_{aw}.

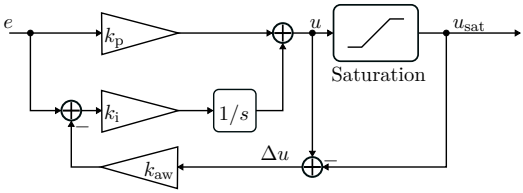


Figure 3.16: Anti-Windup for PI-controller saturation.

$$u = e \cdot k_{\text{p}} + e \cdot \frac{k_{\text{i}}}{s} - \Delta u \cdot k_{\text{aw}} \cdot \frac{k_{\text{i}}}{s} = e \cdot k_{\text{p}} + e \cdot \frac{k_{\text{i}}}{s} - \Delta u \cdot \frac{1}{T_{\text{aw}} s} \tag{3.47}$$

The design parameter k_{aw} depends on the desired reset time T_{aw}. Choosing $T_{\text{aw}} = T_{\text{i}}$ leads to the general design rule [3, p.59]:

$$T_{\text{aw}} = T_{\text{i}} = \frac{k_{\text{p}}}{k_{\text{i}}} = \frac{1}{k_{\text{aw}} k_{\text{i}}} \qquad \Leftrightarrow \qquad k_{\text{aw}} = \frac{1}{k_{\text{p}}} \quad . \tag{3.48}$$

The anti-windup for PR-Controllers is more complex but follows a similar approach [92]. The impact of the limitation is discussed in more detail in chapter 6 for grid-following control and chapter 7 for grid-forming control.

4 Simulation and Rapid Control Prototyping Framework for Grid Converters

As presented in previous chapters, the main research goal of this thesis is to model grid converters and develop control structures for FRT, weak grids, and grids with a high content of voltage harmonics. Therefore, a methodology framework to describe control systems and to design control parameters is developed. This framework consist of analytical models to predict parameter impacts, high-fidelity numerical models to verify the analytical models, and full-fidelity test benches to validate the simulation models experimentally. Moreover, the models with higher fidelity identify critical effects that cannot be captured by the low-fidelity models. This model categorization fits well in the widely adopted V-diagram for model-based design in different applications [93], [94], [95, p.35]. The V-diagram is a standard approach for different development processes to link development phases with a corresponding testing phase to validate the results [93], [94].

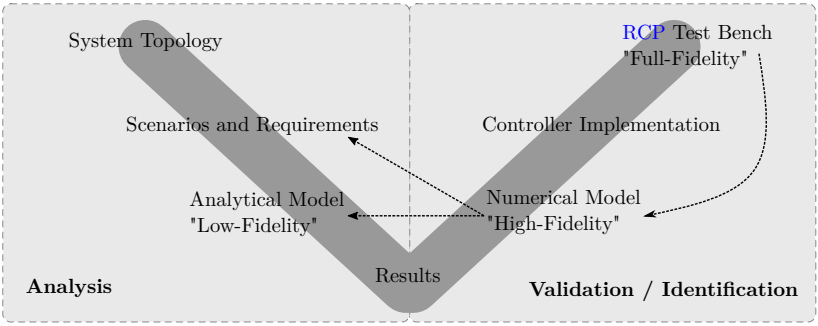


Figure 4.1: Analysis concept according to the model-based design with V-diagram.

An analytical model enables deep physical insight but lacks in fidelity due to simplifying assumptions. In contrast, a high-fidelity model lacks in physical insight but accurately predicts the system behavior. Hence, both high and low-fidelity models are used to enable

in-depth physical understanding as well as validating system characteristics. Fig. 4.1 shows how the V-diagram is applied to the research question and highlights the analysis phases or testing phases with the corresponding fidelity-level. The testing phases typically rely on models with high fidelity to validate the findings from the analytical models.

The following chapter discusses these phases and corresponding model types. At first, the different simulation methods and their analysis techniques are explained. The second section presents the Rapid Control Prototyping (RCP) test bench based on a *dSPACE MicroLabBox* and the control implementation in the Central Processing Unit (CPU) and Free Programmable Gate Array (FPGA) using *MATLAB Simulink* and *Xilinx System Generator*.

4.1 Simulation - Multi-Fidelity Modeling Approach

This thesis focuses on models that accurately predict the characteristics of RES converter systems. A proper validation technique to prove model accuracy is provided by a multi-fidelity approach using different model types. Therefore, numerical models, nonlinear time-invariant models, and linear time-invariant models are implemented, which significantly differ in their analysis techniques and model accuracy.

4.1.1 Numerical Models - Large-Signal Models

In this thesis, numerical models are implemented in *MATLAB Simulink*. This program enables modeling with two abstraction layers that consist of almost arbitrary mathematical expressions and dependencies. Fig. 4.2 shows the model of a grid converter with LC-filter, digital cascaded control, and measurements. This model is a nonlinear time-variant data-sampled system [96], and thus contains two modeling layers. First, the digital control is implemented in Laplace- or z-domain, and second, the model of the physical system is implemented with *SimPowerSystems* in the continuous time-domain. The simulation platform distinguishes between signal and power paths, which can be connected by voltage and current measurement blocks.
The model is rather complex even for one grid-connected converter, but accurately describes the most influential system components such as limitations, modulators, measurement delays, and nonlinear control calculations. Since the focus is on the control characteristic, the model intentionally neglects switching slopes and on-state characteristics of the semiconductors, temperature dependencies, and Electromagnetic Interference (EMI) phenomena.
The model accurately predicts the system characteristics due to its low number of assumptions, and thus its high complexity. Unfortunately, this complexity makes it difficult to analyze its characteristics. All controller and scenario parameters must be defined in the generic model to perform a simulation, and then, only time-domain input-output characteristics can be determined for single scenarios. With the time-domain waveforms, system behavior can be

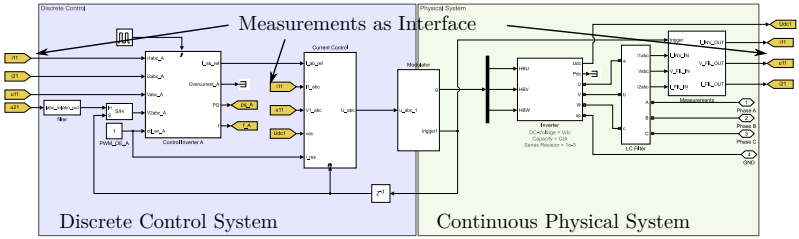


Figure 4.2: Model of an RES-converter with cascaded control implemented in *MATLAB Simulink*.

evaluated according to rise time, falling time, settling time and steady-state deviation [70]. Due to necessary specific parameters and scenario definitions, the simulation results are often not adaptable to other system configurations. Hence, these models are mainly used to validate the findings derived from analytical models.

4.1.2 Nonlinear Time-Invariant - Large-Signal Models

The numerical model is often too complex to sufficiently analyze the impact of controller parts or design parameters on system characteristics. Nonlinear time-invariant models may overcome this problem. The advantage is that they can achieve the same fidelity as numerical models and simultaneously enable analytical interpretations such as phase portraits and Lyapunov's direct method [97], [98]. However, the analysis methods are often only practicable for simplified structures or single controller components.
Nonlinear systems can be described in the state-space where the system states mainly define the structure of the model. In contrast to linear state-space models, the state derivative may depend on nonlinear combinations of states that leads to state-dependent dynamic matrices such as $\mathbf{A}(\mathbf{x})$. The system matrix can then be directly analyzed with nonlinear analysis techniques, i.e., phase portrait or Lyapunovs direct method.

The phase portrait can be used to analyze nonlinear differential equations without solving them [97]. This technique visualizes system trajectories and can identify Stable Equilibrium Points (SEPs) and Unstable Equilibrium Points (UEPs), and thus predict stability. However, phase portrait analysis is usually only applicable to systems with orders smaller than three. This limitation is restrictive for grid converter systems since the order of the models typically exceeds this limit. This is even true for comparatively simple controllers, such as the PLL (see Fig. 5.86).

Lyapunov's direct method is suitable for analyzing nonlinear systems of higher order, but does not provide a straightforward application to arbitrary systems. It relies on an arbitrarily chosen energy function $V(\mathbf{x})$ that must fulfill the requirements according to [98]:

$$V(\boldsymbol{x}_0) = 0 \quad , \quad V(\boldsymbol{x}) > 0, \boldsymbol{x} \neq \boldsymbol{x}_0 \quad , \quad \dot{V}(\boldsymbol{x}) \leq 0 \quad . \tag{4.1}$$

If V fulfills these requirements, the system is locally or globally asymptotically stable, dependent on the analyzed state-space region [98]. Finding the system energy function is a challenging task since these functions are not generally valid. However, this method principally allows to extract the large-signal characteristics of nonlinear systems with analytical methods, which is crucial for analyzing converter systems during FRT. Its application on PLLs and grid-following control in weak grids is discussed in chapters 5 and 6.

4.1.3 Linear Time-Invariant Models - Small-Signal Models

In contrast to Lyapunov's direct method, Linear Time-Invariant (LTI) theory consists of more convenient techniques to analyze system characteristics based on system equations. If the equilibrium point or operating point of the nonlinear system is known, the first-order Taylor series can linearize the system around this equilibrium. This linearized model is an LTI system that is usually only accurate in a narrow range around the equilibrium, therefore, linearized models are often used as SSMs. Unfortunately, it is not practical for most systems to derive the accuracy range without extensive LSM simulations.
Once an LTI model is derived for one operating point, several analysis methods can extract the system characteristics. The most common techniques are eigenvalue analysis, Nyquist plots, and Bode plots. Of course, the input-output characteristics can be obtained by time-domain simulations with Ordinary Differential Equation (ODE) solvers as well. However, other methods are more potent since they derive system characteristics without solving differential equations. Eigenvalue analysis is a useful tool to derive small-signal stability, modes of oscillation, and damping ratios. Nyquist plots and Bode diagrams describe small-signal stability and stability margins. Moreover, Bode plots are suitable for determining the disturbance rejection as shown in chapter 5. Even though very effective analysis methods exist for LTI models, their results may only be valid under very restrictive assumptions dependent on the SSM accuracy. This uncertainty makes it crucial to validate SSMs with LSMs or experiments.

Since the grid converter plant is of major interest in this thesis, this section reviews the basic nonlinear terms and derives the linear model. The modulator and IGBTs switching patterns introduce nonlinearity and time-variant characteristics, causing the grid converter to be a nonlinear, time-variant system. However, averaging of the output voltages $\mathbf{v}_{\text{conv}}$ over one

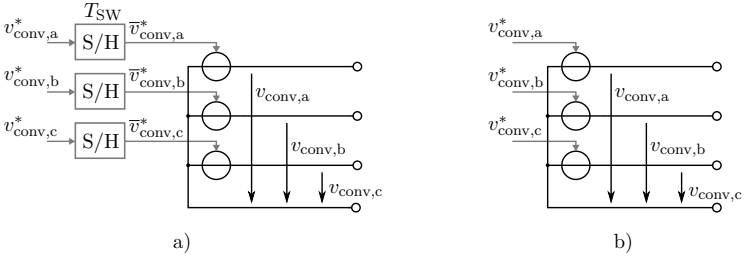


Figure 4.3: Equivalent circuits of the converter neglecting IGBT switching characteristics: a) with sampling emulation b) without sampling - ideal controller voltage output.

switching period T_{sw} removes the time-variant characteristics of the switching function $\mathbf{q}$ according to:

$$\overline{\mathbf{v}}_{conv}(t) = \frac{1}{T_{sw}} \int_{t_n - T_{sw}}^{t_n} \mathbf{v}_{conv}(t) \mathrm{d}t = \frac{1}{T_{sw}} \int_{t_n - T_{sw}}^{t_n} \frac{V_{dc}}{2} \mathbf{q}(t) \mathrm{d}t \approx \frac{V_{dc}}{2} \mathbf{m}(t) = \mathbf{v}^*_{conv}(t) \quad . \tag{4.2}$$

Finally, the linearized converter voltage $\overline{\mathbf{v}}_{conv}$ corresponds to the reference voltage $\mathbf{v}^*_{conv}$ by assuming the averaged switching function $\mathbf{m}$ and the constant dc-link voltage V_{dc}. Since the averaging operator in 4.2 is linear, it does not affect the transfer functions of the rest of the system [99].

Fig. 4.3 presents the Thevenin equivalent circuits of the converter. The circuit in Fig. 4.3a still considers modulator sampling properties such as regular sampling by using a sample and hold block (S/H). This model sufficiently describes frequencies up to one-tenth of the switching frequency ($f_{sw}/10$) [100], [99]. Components of higher frequencies are typically small compared to the operating point variables in most scenarios [99]. The averaged model thus provides an accurate linear, time-invariant model that enables efficient simulation of the power electronic front-end to design and analyze the feedback control.

The passive components of the LCL-filter and source impedances $\underline{Z}_S$ define the converter control plant. Three single-phase equivalent circuits represent the phases a, b, and c in the phase domain. However, only two circuits are independent due to the coupling of the phase voltages. Assuming equal impedances for all three phases, the system description can be unified using vectors, e.g. $\mathbf{i}_1 = [i_{1,a}\ i_{1,b}\ i_{1,c}]^T$. The averaged, linear model of the grid-connected converter in phase domain considering the modulator, the LCL-filter, and the source impedance $\underline{Z}_S$ is presented in Fig. 4.4. This phase domain model contains the ODEs and represents the dynamic characteristics. The system inputs and outputs must be defined to derive the dynamic state-space model in the form according to 4.3. There are two important inputs for the system. First, the grid voltages $\mathbf{v}_S$ are the interface of the RES-converter to the power system. Second, the converter reference voltages $\mathbf{v}_{conv}$ are the interface to the converter control system. Consequently, the input vector $\mathbf{u}$ is formed by $\mathbf{v}_S$

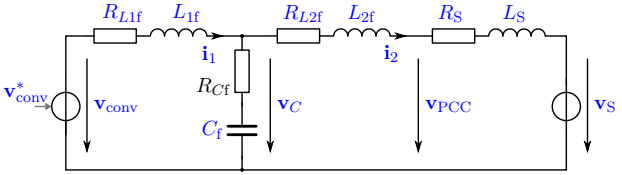


Figure 4.4: Averaged phase domain model of the grid converter with LCL-filter and source line impedance.

and $\mathbf{v}_{conv}$ (see 4.4). The state vector $\mathbf{x}$ and output vector $\mathbf{y}$ contain the converter currents $\mathbf{i}_1$ and $\mathbf{i}_2$, and the capacitor voltages $\mathbf{v}_C$, since they are of major interest for the control characteristics.

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}\ ;\ \mathbf{x}(0) = \mathbf{x}_0 \qquad \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \tag{4.3}$$

$$\mathbf{u} = \begin{bmatrix} \mathbf{v}_{conv} & \mathbf{v}_S \end{bmatrix}^T \qquad \mathbf{x} = \mathbf{y} = \begin{bmatrix} \mathbf{i}_1 & \mathbf{i}_2 & \mathbf{v}_C \end{bmatrix}^T \tag{4.4}$$

Rearranging the differential equations derived from Fig. 4.4, according to the definitions of $\mathbf{u}$ and $\mathbf{y}$ leads to the system matrix $\mathbf{A}$, the input matrix $\mathbf{B}$, the output matrix $\mathbf{C}$, and the feedthrough matrix $\mathbf{D}$ in 4.5 and 4.6. This state-space model in the time domain accurately describes the system dynamics of the grid converter with LCL-filter. However, for some analysis techniques, it is more convenient to derive the state-space model in the Laplace domain.

$$\mathbf{A} = \begin{bmatrix} -\frac{R_{Cf}+R_{1f}}{L_{1f}} & \frac{R_{Cf}}{L_{1f}} & -\frac{1}{L_{1f}} \\ \frac{R_{Cf}}{L_{2f}} & -\frac{R_{Cf}+R_{2f}}{L_{2f}} & \frac{1}{L_{2f}} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 1 \end{bmatrix} \tag{4.5}$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{L_{1f}} & 0 \\ 0 & -\frac{1}{L_{2f}} \\ 0 & 0 \end{bmatrix} \qquad \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \qquad \mathbf{D} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{4.6}$$

The transformation rule given in 4.7 transforms the system in the Laplace domain by using the inverse operator and the identity matrix $\mathbf{I}$. Rearranging the results leads to the transfer function matrix $\mathbf{G}(s)$ containing all combinations of transfer functions of $\mathbf{u}$ and $\mathbf{y}$ according

to 4.8. All these transfer functions have the same poles and only differ in their zeros. This characteristic indicates same stability properties but different dynamics.

$$\mathbf{y} = \Big(\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\cdot\mathbf{B}+\mathbf{D}\Big)\,\mathbf{u} + \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\,\mathbf{x}_0 = \mathbf{G}(s)\mathbf{u} + \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\,\mathbf{x}_0 \tag{4.7}$$

$$\mathbf{G}(s) = \frac{1}{H(s)}\begin{bmatrix} \frac{1}{L_{1f}}\left(s^2 + \frac{R_{2f}+R_{Cf}}{L_{2f}}\,s + \frac{1}{L_{2f}\cdot C_f}\right) & -\frac{R_{Cf}}{L_{1f}\cdot L_{2f}}\left(s+\frac{1}{R_{Cf}\cdot C_f}\right) \\ \frac{R_{Cf}}{L_{1f}\cdot L_{2f}}\left(s+\frac{1}{R_{Cf}\cdot C_f}\right) & -\frac{1}{L_{2f}}\left(s^2 + \frac{R_{1f}+R_{Cf}}{L_{1f}}\,s + \frac{1}{L_{1f}\cdot C_f}\right) \\ \frac{1}{L_{1f}\cdot C_f}\left(s+\frac{R_{2f}}{L_{2f}}\right) & \frac{1}{L_{2f}\cdot C_f}\left(s+\frac{R_{1f}}{L_{1f}}\right) \end{bmatrix} \tag{4.8}$$

with

$$H = s^3 + a_1\,s^2 + a_2\,s + a_3 \qquad a_1 = \left(\frac{R_{2f}}{L_{2f}} + \frac{R_{1f}}{L_{1f}} + \frac{R_{Cf}}{L_{2f}} + \frac{R_{Cf}}{L_{1f}}\right) \qquad L' = \frac{L_{1f}\cdot L_{2f}}{L_{1f}+L_{2f}} \tag{4.9}$$

$$a_2 = \left(\frac{1}{C_f\cdot L'} + \frac{R_{1f}\cdot R_{2f}}{L_{1f}\cdot L_{2f}} + \frac{R_{1f}\cdot R_{Cf}}{L_{1f}\cdot L_{2f}} + \frac{R_{2f}\cdot R_{Cf}}{L_{1f}\cdot L_{2f}}\right) \qquad a_3 = \frac{R_{1f}+R_{2f}}{C_f\cdot L_{1f}\cdot L_{2f}} \tag{4.10}$$

Rockhill derived the state-space model without parasitic components (R_{L1f} and R_{L2f}) [48], and the model given in 4.8 is identical under the assumption $R_{1f} = R_{2f} = 0$ pu, as presented in 4.11. This comparison verifies the extracted model.

$$\mathbf{G}'(s) = \frac{1}{s\;\Gamma(s)}\begin{bmatrix} \frac{1}{L_{1f}}\left(s^2 + \frac{1}{L_{2f}\cdot C_f}\right) & -\frac{R_{Cf}}{L_{1f}\cdot L_{2f}}\left(s+\frac{1}{R_{Cf}\cdot C_f}\right) \\ \frac{R_{Cf}}{L_{1f}\cdot L_{2f}}\left(s+\frac{1}{R_{Cf}\cdot C_f}\right) & -\frac{1}{L_{2f}}\left(s^2 + \frac{1}{L_{1f}\cdot C_f}\right) \\ \frac{1}{L_{1f}\cdot C_f}\;s & \frac{1}{L_{2f}\cdot C_f}\;s \end{bmatrix} \tag{4.11}$$

$$\Gamma(s) = s^2 + \frac{R_{Cf}}{L'}\,s + \frac{1}{C_f\cdot L'} \tag{4.12}$$

The transfer functions can also be directly calculated by describing the electrical components in the Laplace domain. This calculation can be more convenient if the plant contains electrical components and control blocks. The block diagram of Fig. 4.4 is shown in Fig. 4.5, and two essential steps are necessary to extract the transfer functions. First, the block diagram should be rearranged to canonical form. Refer to Fig. A.1 for more details on this. In the second step, the transfer function for every input and output combination is derived by setting all neglected inputs to zero. This process leads to G_{conv} for the $\mathbf{v}_{\text{conv}}$ to $\mathbf{i}_2$ transfer functions and G_S for the $\mathbf{v}_S$ to $\mathbf{i}_2$ transfer functions, which are exemplarily given for one phase:

$$G_o = \frac{G_{1f}G_C}{1+G_{1f}G_C}G_{2f} \tag{4.13}$$

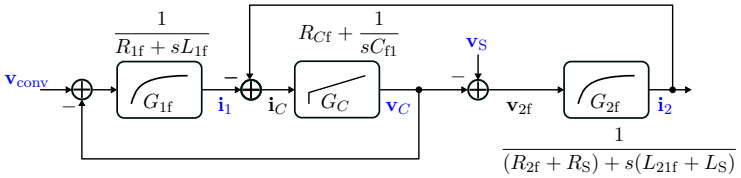


Figure 4.5: Averaged Laplace domain model of grid converter with LCL-filter and source line impedance.

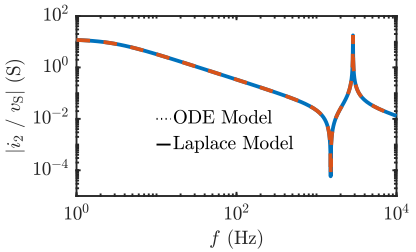


Figure 4.6: Bode plot of the transfer function G_S derived with ODEs or Laplace block scheme.

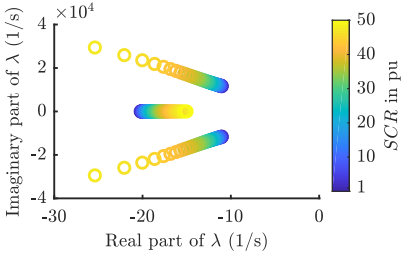


Figure 4.7: Evaluation of eigenvalues of G_S for sweeping L_S and R_S or the SCR (with constant L_S/R_S-ratio), respectively.

$$\Rightarrow G_{conv} = \frac{i_2(s)}{v_{conv}(s)} = \frac{G_{1f}G_o}{G_{1f}+G_o} \quad , \qquad G_S = \frac{i_2(s)}{v_S(s)} = \frac{-G_{1f}G_{2f}}{G_{1f}+G_o} \quad . \tag{4.14}$$

To verify the two extraction methods, Fig. 4.6 contains the Bode plots for the magnitudes of G_S for both models. The frequency characteristics are identical, confirming the equivalence of both models. To highlight the effectiveness of the models for analysis, Fig. 4.7 shows the poles of G_S for different SCRs or R_S and L_S, respectively. These results indicate that the SCR critically affects system stability since the poles tend to move to the imaginary axis with decreasing SCR. These are only preliminary results since the presented models neglect the converter control. The overall characteristics of the VOC will be discussed in detail throughout chapter 6.

4.2 Grid Converter Test Bench with Rapid Control Prototyping

Known model assumptions can be verified using simulation models with higher fidelity. However, this approach does not work for unknown model assumptions or uncertainties. Measurements with the original system or a laboratory test bench, which represents the original system, must identify these unknown aspects. Therefore, three grid converter test

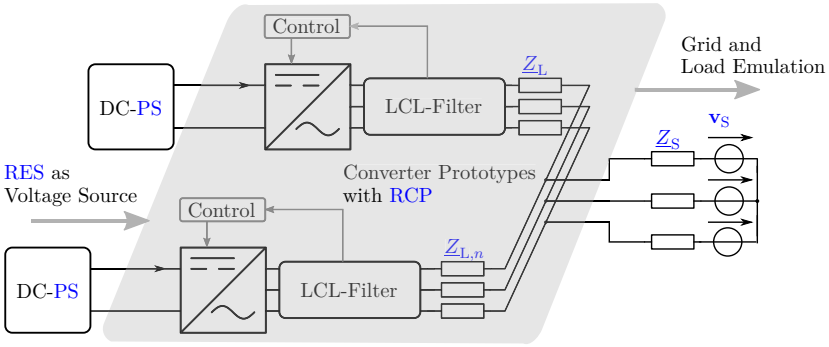


Figure 4.8: Basic structure of the RCP test bench with *dSPACE* System

benches with Rapid Control Prototyping (RCP) systems were designed and built to verify controllers, models and their results. Each test bench is optimized for different purposes or application scenarios, respectively:

1. Parallel converters with shared controller hardware
2. State-of-the-art IGBT converter with flexible filter configurations
3. Silicon Carbide (SiC)-Metal-oxide-semiconductor field-effect transistor (MOSFET) converter for high-frequency applications

This section presents the basic validation concept, the different test benches with specifications, and the generic controller implementation for RCP systems.

4.2.1 Basic Concept: Converter Prototypes with Rapid Control Prototyping and Grid Emulation

The grid converter test bench used in this thesis contains three basic components, i.e., the dc-side hardware, the ac-side hardware and the converters providing an interface between the two sides. On the dc-side, a constant voltage is provided by a Power Supply (PS) from *Elektro-Automatik*. A constant voltage source is considered sufficient, because the focus of this thesis is on the ac-side. For the ac-side, there are three options: passive loads, a low-voltage connection to the public electricity grid and a grid emulator. The grid emulator is required for reproducible results as well as fault scenarios that cannot easily be produced from the public grid. A grid emulator from *Cinergia* is used in the setups. The third component is the converter prototype with RCP system that is the key element of the investigation.

The three different converter prototypes are based on the same concept and consist of the power hardware, measurements, signal conditioning, and a *dSPACE MicroLabBox* as RCP

system. The overall system is shown in Fig. 4.9, and the power hardware contains dc-link capacitors, three semiconductor half-bridges, and the output LCL-filter. A precharge/discharge circuit with resistors and relays, and the output circuit breaker S_{PCC} with fuses complete the setup to guarantee safe operation.
The measurements slightly differ in the three converter prototypes due to changing requirements on bandwidth and immunity to EMI. However, the dc-link voltage V_{dc}, the output filter voltages $\mathbf{v}_C$, the PCC voltages $\mathbf{v}_{\mathrm{PCC}}$, the converter currents $\mathbf{i}_1$, and grid currents $\mathbf{i}_2$ are measured and send to the *MicroLabBox* in all prototypes. The *MicroLabBox* generates control signals for gate drivers, relays, and circuit breakers, and consists of a CPU and a FPGA to process the measurements and run the control algorithms. Furthermore, it provides a General User Interface (GUI) to visualize instantaneous waveforms and accepts control inputs by test bench operators.
Based on the presented concept, three test benches were built for low-voltage grids with the same voltage rating and similar power rating. The ac output voltage is 400 $\mathrm{V_{RMS}}$, which requires dc-link voltages in the range of V_{dc}= 650 − 720 V depending on the modulation method. This output voltage allows the direct connection to the low-voltage grid in the laboratory. The power rating of each converter is approximately 10 kW.

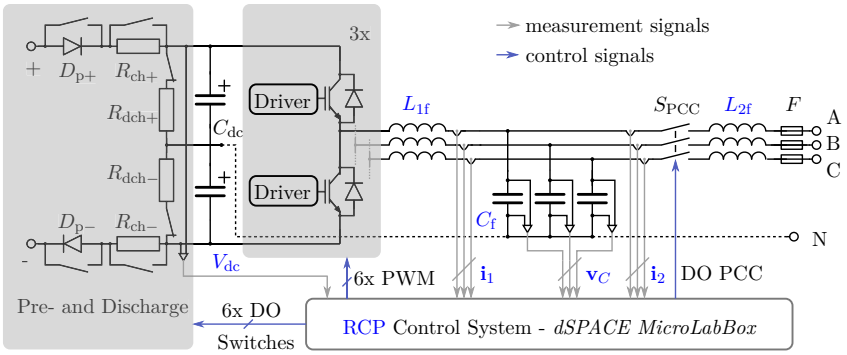


Figure 4.9: Basic structure of the RCP test bench with the *dSPACE* system.

Scaled Parallel Converter Test bench with Shared Control System

The parallel converter test bench contains two converters controlled by one *MicroLabBox* to investigate grid-forming controls and interactions between converters. This setup mainly focuses on scenarios with RES converters in medium or high power applications. Typical systems are wind generators connected to medium-voltage and high-voltage grids. Two-level VSCs for wind generators with power ratings of up to 1.5 MW typically have switching frequencies of up to 3.5 kHz and output voltages of 690 V [101], [102], which leads to dc-link

voltages in the range of 1100-1400 V [103]. These target application specifications serve as an orientation for the test bench design.

The test bench converters are scaled to emulate the control characteristics of the target application. But how to achieve similar converter control characteristics of two setups? First, the converter switching frequency must be equal. Then, the system impedances must be scaled according to different voltage and current ratings to achieve the same time constants and relative voltage drops. Impedance scaling mainly influences output filter components and should conserve filter resonance frequencies.

The test bench contains two converters with measurements and the control rack for signal routing and conditioning in one cabinet, as shown in Fig. 4.10. It was built in cooperation during the supervised master's thesis [104]. Winkelnkemper designed the original converters during his thesis and his work at TU Berlin [105]. Four IGBT half-bridge modules *Semikron SKM 145 GB 123 D* are mounted on a heatsink and are controlled by four half-bridge gate drivers *SKHI 23/12*. The design of Winkelnkemper is extended by current sensors on the converter Printed Circuit Board (PCB) and the optical fiber interface to the control rack.

Grid converters need output filters to attenuate the current harmonics to comply with grid standards. These standards distinguish between low order harmonics up to 2.5 kHz (e.g., DIN EN 61000-3-12, IEEE 519) and the EMI considerations starting at 150 kHz and above (e.g., DIN EN 61000-6-3). Moreover, they distinguish between common mode and differential mode distortions. Low order harmonics predominantly occur as differential mode, and high order harmonics mainly occur as common mode [106]. The converter control dynamics below switching frequency are mainly affected by the grid filter. Hence, the EMI filter is neglected for the control design, and only the *LCL*-filter must be designed.

LCL-filter designs typically rely on the maximum converter current ripple, the reactive power of the filter capacitor, and the resonance frequency according to 4.15 and 4.16 [107], [48]. The requirements on current ripple $\Delta i_{L1f,pu}$, and reactive power q_{pu} are already pu values. If these requirements and the switching and resonance frequency are the same in two setups, their impedances are appropriately scaled to ensure the same control characteristics. The used *LC*-filter is the commercial product *REO CNW 933-16* that achieves $\Delta i_{L1f,pu}$ =20% current ripple at f_{sw}= 5.5 kHz and q_{pu} =1.7%. The grid side filter inductance L_{2f} completes the *LCL*-filter, which leads to a resonance frequency of f_{res}=2.8 kHz. The power part parameters of the test bench are summarized in Table 4.1.

$$L_{1f} = \frac{1}{8\sqrt{3}} \cdot \frac{V_{dc}}{\Delta i_{L1f,pu} \cdot I_r \cdot f_{sw}} \tag{4.15}$$

$$C_f = q_{pu} \cdot \frac{P_r}{3 \cdot 2\pi f_1 \cdot V_r^2} \tag{4.16}$$

Table 4.1: Basic parameters of parallel converter test bench

Parameter	Value	Description / Part
L_{1f}	3.4 mH	*REO* CNW 933-16
C_f	3.3 μF	*REO* CNW 933-16
$L_{2f,1}$/ $L_{2f,2}$	1.3 mH/ 1.46 mH	-
C_{dc}	2.2 mF	*TDK* B43703
f_{sw}	$<$ 8 kHz	*Semikron* SKM 145 GB 123 D with SKHI 23/12
f_V	10 kHz	sensor bandwidth / *LEM* LV 25-P
f_I	120 kHz	sensor bandwidth / *Allegro MircoSystems* ACS 758

The setup needs the measurement feedback to the RCP system to control the converters. Voltage transducers and Hall effect current probes realize the necessary voltage and current measurements, which achieve bandwidths of 10 kHz (f_V) and 120 kHz (f_I), respectively (see Table 4.1). The control rack provides the power supply for the sensors and adjusts the signals to the analog input voltage range of the *MicroLabBox*.

The major purpose of this setup is to investigate parallel converters and their interactions, such as power-sharing accuracy. In a first test case, the two converters are connected to the grid sequentially. Fig. 4.11 shows the output power of both converters with droop-control. Converter 1 is connected to the public grid, mainly injecting active power P_1 with only minor reactive power Q_1 since the voltage magnitude is almost at its nominal value. Converter 2 synchronizes to the grid voltage and connects to the grid at approximately $t = 0.5$ s. After a transient period of approximately 1 s with some oscillation but no overshoot, both active and reactive power converge to stable operating points and verify high power-sharing accuracy without communication. This test bench is mainly used to validate the design for the droop control and the results for FRT operation for unbalanced faults discussed in chapter 7.

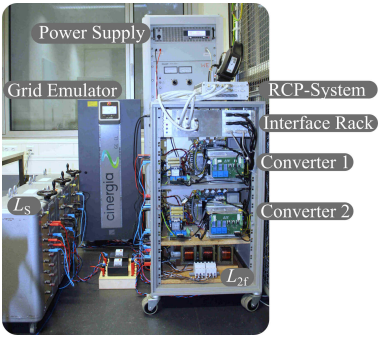


Figure 4.10: Converter test bench consisting of two converters with LCL-filters, interface rack, RCP-system, line impedance, power supply, and grid emulator.

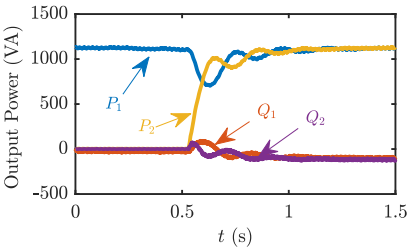


Figure 4.11: Power-sharing of two parallel converters with grid connection.

Table 4.2: Basic system parameters

Specification	Value	Part
L_{1f}	1.2 mH	-
C_f	10 μF	-
C_{dc}	2.2 mF	*TDK* B43703
f_{sw}	<20 kHz	*Semikron* 26ACM12V17

State-of-the-Art IGBT Converter with Flexible Filter Configuration

The semiconductor's performance limits the parallel converter test bench to low switching frequencies of $f_{sw}\leq$8 kHz. As presented before, this is not a drawback to emulate high power applications due to their typically low switching frequencies. However, e.g., PV-inverters often have lower power ratings and higher switching frequencies caused by efficiency, emission, and volume requirements. Consequently, a two-level converter based on IGBT4 technology was designed and built in cooperation during a supervised diploma thesis [108]. It is based on the structure in Fig. 4.9. The main differences compared to the parallel converters are the IGBT module with gate drivers, filter components, and measurements.

The IGBT module and cooling system are chosen based on a hybrid electrical and thermal simulation in *PLECS* using information provided by the semiconductor and heatsink datasheets. The simulation results for the semiconductor losses were verified with a commercial tool provided by *Semikron* and showed just minor differences smaller than 1 % of the total losses [108]. The results lead to the *MiniSKiiP 35NAB12T4V1* module with blocking voltages of 1.2 kV and 72 A rated dc-current. At f_{sw}=20 kHz, the setup can achieve a power rating of approximately 10 kVA.

The gate drivers are based on the driver core *2SC0106T* from *Concept*. These driver cores are mounted on driver PCBs, providing active clamping, desaturation detection, soft shut-down, and low-voltage lockout as safety features. The gate resistors are chosen based on double-pulse switching test results such that the voltage overshoot does not exceed the safe operating range while the switching speed is maximized.

For the LC-filter design, the maximum inverter current ripple was limited to 20% of the rated current to determine L_{1f}. This limit leads to $L_{1f}\approx$ 1.2 mH for f_{sw} = 16 kHz and V_{dc}= 750 V. Then, C_f is given by the maximum output current harmonics defined in several standards such as IEEE-1547 [109]. However, these standards only limit harmonics up to 2.5 kHz and thus enable a wide range of choosing the capacitance C_f. On the one hand, a larger C_f guarantees more stable output voltages $\mathbf{v}_C$, which is an advantage for grid-forming control algorithms. On the other hand, large C_f shift the resonance frequency to low values that may cause critical resonance phenomena with the grid. Since the current harmonics do not provide a sufficient design criterion, the capacitance is calculated based on the reactive power $q_{pu} = 0.05\ pu$, which leads to $C_f\approx$ 10 μF.

Higher switching frequency and smaller filters lead to faster dynamics of the converter. Hence, the measurements must be enhanced to achieve sufficient control characteristics. The *Allegro ACS-730* current sensor has a bandwidth of 1 Mhz with sufficient immunity to distortions. Galvanically isolated op-amps of type *AMC 1301* realize the voltage measurements that achieve bandwidths of up to 200 kHz.
The converter with all components is presented in Fig. 4.12. The output filter and grid connection components such as fuses, circuit breakers, and grid measurements sensors are built into another rack to achieve more flexibility in the filter configuration, as shown in Fig. 4.12.

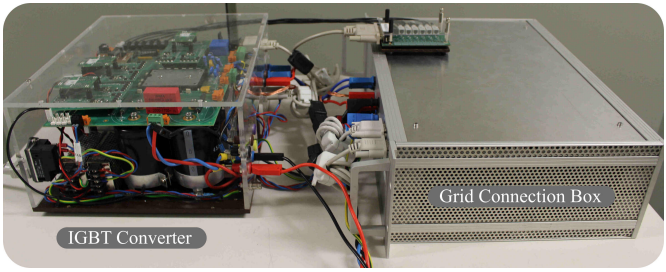


Figure 4.12: IGBT 4 grid converter with peripherals, dSPACE interface, filter, and grid connection box.

A first test case is presented in Fig. 4.13 and 4.14. The converter is controlled with VOC and connected to the grid emulator. At $t \approx 0.18$ s a phase jump of -45° occurs in the grid voltages. After a short transient period, grid currents are controlled to the new stable operating point. During phase jumps, the converter dynamics are predominantly affected by the PLL. This characteristic is thoroughly discussed in chapter 5. The presented setup is capable of testing converter control for converter switching frequencies up to 20 kHz with efficiently adaptable filter configurations.

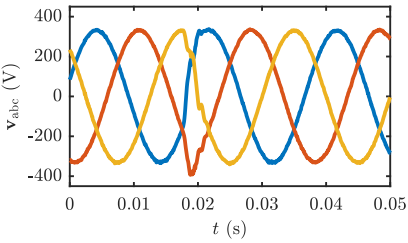


Figure 4.13: Converter voltages during a -45° phase angle jump.

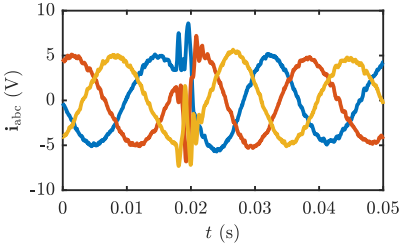


Figure 4.14: Converter currents during a -45° phase angle jump.

SiC-MOSFET Converter for High-Switching Frequencies

New semiconductor devices based on SiC lead to an exceptional increase of switching frequencies without an increase in switching losses. Due to the commercial availability of devices with blocking voltages of up to 1.7 kV and power ratings of several kVAs, SiC-MOSFETs are gaining importance in grid converter applications. Therefore, the third test bench is based on an SiC module and points at applications that require high switching frequencies, such as harmonic emulation or compensation.
This test bench was designed and built during a supervised master's thesis [110] and a detailed comparison to the IGBT4-converter is presented in [111]. The design process is based on the IGBT4-converter design and contains the *MiniSKiiP 26ACM12V17* module. In this case, the converter has smaller gate driver loops and gate drivers with increased $\mathrm{d}v/\mathrm{d}t$ immunity due to the fast switching of the SiC-MOSFETs. For details on the general design process, refer to the preceding section. The SiC-converter achieves switching frequencies up to 100 kHz with a rated power of 10 kVA in grid connection and is shown in Fig. 4.15.

During this thesis, the setup is mainly used for PLL tests that need accurate emulation of high-order voltage harmonics. The standard EN 50160 defines voltage harmonics up to the 25th harmonic. The accurate voltage emulation is presented in Fig. 4.16, which shows only minor differences between the reference voltages $\mathbf{v}^*_{\mathrm{abc}}$ and converter output voltages $\mathbf{v}_C$. This setup can be used to validate controls for converter setups with switching frequencies up to 100 kHz and to emulate voltage harmonics, as presented in chapter 5.

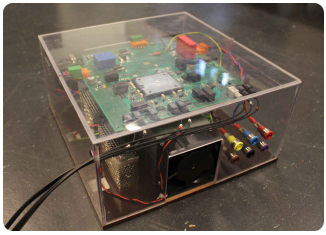


Figure 4.15: SiC-MOSFET based grid converter with peripherals.

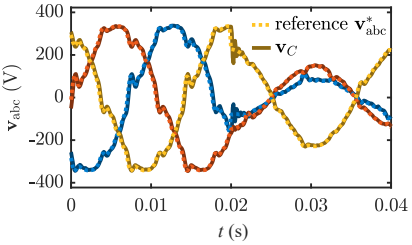


Figure 4.16: Grid voltage emulation up to the 25th harmonic, according to EN 50160.

4.2.2 Generic Controller Implementation

The *MicroLabBox* contains a CPU and FPGA that can process measurement data, control algorithms, and control signals. The algorithms can be implemented with *Xilinx System Generator* using two programming layers each for the CPU and FPGA programs. The FPGA directly processes the measurement data from Analog-Digital-Converters (ADCs) or Digital Inputs (DIs) and controls the output of Digital Outputs (DOs). These signals can then be

Table 4.3: dSPACE control system parameters [112]

Quantity	Value	Description
T_{CPU}	100 µs	Cycle time of CPU
$T_{\mathrm{ADC,A}}$	100 ns	Cycle time of ADC Class A with 14bit resolution
$T_{\mathrm{ADC,B}}$	1 µs	Cycle time of ADC Class B with 16bit resolution
T_{FPGA}	10 ns	Cycle time of FPGA

routed to the CPU. In the setups, two classes of ADCs are used. ADCs of class A convert all converter output currents and voltages, while class B ADCs only convert the dc-link voltages [112]. The ADC conversion times are summarized in Table 4.3.
Maximum execution step times of algorithms mainly determine if the CPU or FPGA must execute the program part. The CPU step time varies according to model complexity and is typically in the range of 100 μs. The algorithms are implemented in *MATLAB Simulink*, where compiling is very time-efficient. The FPGA achieves much lower step times of typically 10 ns, but the programming is more complicated due to strict data type definitions and execution timing requirements. Moreover, the compiling process needs significantly more time. Exemplarily, the VOC algorithm for one converter in the CPU compiles in less than 1 minute, whereas a comparable algorithm in the FPGA compiles in approximately 30 minutes. Since the FPGA implementation is more time-consuming, the necessary time step for every single controller part is evaluated to decide if it must be implemented in the FPGA or can be implemented in CPU.
Since control algorithms on RCP systems must run with fixed step time, controllers must be transformed to the discrete domain. The two model layers, i.e., CPU and FPGA, demand different processes to transform continuous controllers into their discrete counterpart since the available functions in *MATLAB Simulink* and *Xilinx*-blockset differ significantly.

CPU Controller Implementation in *Simulink*

Controller programming in the CPU model is identical to the implementation of discrete *Simulink* models with fixed step time. Two different processes are convenient to transform continuous controllers into their discrete equivalence. The first possibility is to simply replace all integrators $1/s$ in the continuous block diagram by discrete integrator blocks in *Simulink*. Discrete integrator blocks already contain different discrete representations such as forward Euler, backward Euler, or trapezoidal approximation. The second method utilizes discrete transfer function blocks in *Simulink*. This method requires discrete transfer functions of the continuous controller parts. A simple *Matlab* workflow for the z-transform utilizes the function:

```
Gdiscr=c2d(Gcont,Ts,'tustin'),
```

where *Gdiscr* is the discrete form of the continuous transfer function *Gcont*. *Ts* defines the sampling time of the system and, *tustin* exemplarily describes the integration method. Various integration methods are available and according to extensive studies in [113], [114], applying impulse invariant, pole-zero matched, Tustin with pre-warping, Zero-Order-Hold (ZOH) and First-Order-Hold (FOH) formulations yield the most accurate discrete representations for controllers. In this work, Tustin's method is applied predominantly, whereas in some cases, the FOH is used to prevent algebraic loops.
Besides selecting the integration method, the sampling frequency f_s should be at least ten times larger than the controller bandwidth to obtain an accurate representation of the continuous controller [115]. The CPU model is used for controller implementation with lower dynamic requirements such as power controllers, PLLs, and voltage controls. In contrast, the current control requires lower step times, and thus must be executed in the FPGA.

FPGA Implementation with *Xilinx*-Blockset

FPGA models are implemented in *System Generator* by using the *Xilinx*-blockset, which contains several fundamental operators such as adders or multipliers. To implement discrete transfer functions, they must be transformed to difference equations and recursive formulas. These formulas can be programmed by utilizing registers or delay blocks z^{-1}, respectively.
In order to clarify how a controller is realized in the FPGA, the PR-controller is used as an example. First, the ZOH-transform of 3.42 leads to the discrete transfer function of the resonant part of the PR-controller according to:

$$G_{d,\mathrm{res}}(z) = k_\mathrm{i}\frac{z\frac{1}{\omega_1}\sin(\omega_1 T_s) - \frac{1}{\omega_1}\sin(\omega_1 T_s)}{z^2 - z2\cos(\omega_1 T_s) + 1} = k_\mathrm{i}\frac{az - a}{z^2 - bz + 1} = k_\mathrm{i}\frac{a(z^{-1} - z^{-2})}{z^{-2} - bz^{-1} + 1} \quad . \tag{4.17}$$

T_s is the sampling time and ω_1 the fundamental frequency, and thus $a = \frac{1}{\omega_1}\sin(\omega_1 T_s)$ and $b = 2\cos(\omega_1 T_s)$ are constants if ω_1 is assumed to be constant. Second, the proportional part of the controller is added, and the transfer function is rearranged to derive the recursive formula to obtain:

$$u_i = \left(bz^{-1} - z^{-2}\right)u_i + k_\mathrm{i}a\left(z^{-1} - z^{-2}\right)e_i + k_\mathrm{p}e_i \quad , \tag{4.18}$$

where e_i is the controller input and u_i is the controller output of the i-th execution step. This equation can be programmed in the FPGA by using registers and fundamental math operations (e.g., adders, substracters, multipliers), as presented in Fig. 4.17.

The presented programming framework can be used to efficiently implement controllers with different execution step times. The FPGA can meet even challenging time step requirements in the range of a few ns. In this thesis, various PLLs, grid-following controls, and grid-forming controls were realized with this platform, and no critical limits for the target application

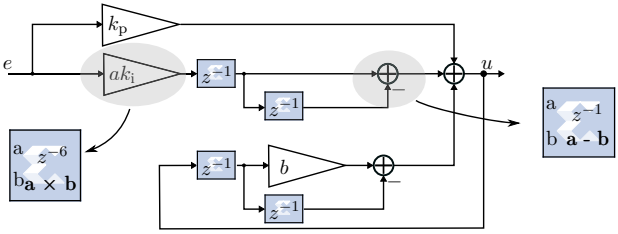


Figure 4.17: PR-controller algorithm in *System Generator* with *Xilinx*-blockset.

were identified. This RCP system, together with the presented hardware test benches, provide a potent framework to validate converter models and analyze grid converter controls experimentally.

5 Modeling, Design, and Characterization of Phase-Locked-Loops during Grid Faults

Fast and robust grid voltage detection is crucial for the control of grid-following converters. Particularly, VOC needs the phase angle of the positive sequence grid voltage to inject active and reactive power accurately. Contrarily, grid-forming converters do not necessarily need a PLL for power control, but a grid synchronization may provide a smooth transient process during connection of grid-forming converters to the grid [3].

In the vast majority of cases, grid synchronization is provided by PLLs, which use feedback control loops to detect the phase angle based on the measured grid voltage. The feedback control is typically realized with PI-controllers to achieve zero steady-state error. The accuracy of the detected phase angle affects separation of injected power into active and reactive power, i.e., the power factor accuracy. The power factor changes significantly during faults with large phase jumps since the PLL must lock on the new phase angle. PLLs thus dominate converter control dynamics during severe grid disturbances.

The simplest PLL structure is the SRF-PLL, which achieves zero steady-state error under ideal grid conditions [116]. However, real three-phase grid voltages contain distortions such as harmonics, unbalances, and frequency variations [58], [38], [45]. These distortions affect voltage magnitude and phase angle estimation of PLLs. If these distortions are not rejected sufficiently by the PLL algorithms, they will impair the steady-state power injection quality of the VSC. Consequently, an error or distortion in the detected grid voltage phase angle propagates to the converter's power factor. These power factor distortions are critical because the VSC must respect the power factor accuracy to comply with grid codes [13].

Severe grid disturbances such as faults pose the most challenging scenarios for PLLs. Faults lead to the most severe transient processes, resulting in large grid voltage steps and phase angle jumps [45]. The PLL must accurately detect these dynamics with small errors to comply with grid codes that demand a fast step response of the reactive current with maximum settling times of 60 ms to reduce the voltage drop at the PCC [13], [67]. Once the fault is cleared, the reactive current must return to its pre-fault value to avoid converter tripping due to overvoltage [58]. Typically, the current control loop is fast enough to comply with grid codes [117], but the PLL time constant is much larger, making it critical for meeting required settling times.

In summary, the major concern of grid synchronization is to realize a PLL with high control bandwidth, high immunity to distortions, and large stability margin. The PLL performance is based on a trade-off between these properties [118]. Various contributions have proposed advanced PLL schemes to enhance the performance under adverse grid conditions, e.g. advanced filter or decoupling structures improve immunity to distortions while trying to preserve the dynamics [72], [119], [120], [56], [121], [122], [118], [123], [124]. S. Golestan has presented an extensive overview of the most popular three-phase PLLs, e.g., the DSOGI-PLL, Moving Average Filter (MAF)-PLL, DSRF-PLL, and Notch-filter (Nf)-PLL [119].
Filter and decoupling structures add complexity to the control system and introduce additional design parameters that demand more sophisticated methods for design and analysis. The vast majority choose the Symmetrical Optimum (SO) to design PLLs [116], [124], [125], [91], [126]. Even though it was originally invented for SRF-PLLs, this design approach can be adapted for PLLs with prefilters [119], [124]. However, the applicability of the SO for PLLs with prefiltering stage is rarely addressed. This discussion is presented in the following chapter and is combined with a detailed design process for a given grid scenario.
Besides enhancing PLLs with filters or decoupling structures, several publications compare and evaluate PLLs during adverse grid scenarios. Ref. [119], [122], [124] and [127] conducted a comparative study with different test cases considering unbalances, harmonics, and frequency variations. However, why these scenarios are chosen and how this choice affects the PLL design is not analyzed in detail. They also do not address the impact of the PLL on the current and power control. Recent research results that present the analysis of PLLs in combination with the current control mainly focus on small-signal stability under ideal voltages and symmetrical faults. Furthermore, they only consider the SRF-PLL without mandatory filters and do not analyze how the design trade-off between immunity to voltage distortions and control bandwidth affects the VSC power factor and its current control [9], [128], [75], [129].

This chapter is intended to fill these gaps and is organized as follows: At first, the general principle of PLLs and their impact on the converter's output power are motivated for the Synchronous Reference Frame with Low-Pass Filters (LSRF)-PLL. The second part introduces critical grid scenarios and addresses converter requirements defined in several grid standards. Then, SRF-PLLs based on sequence decomposition or prefilters are presented, which can detect the positive sequence voltage under severe grid faults considering harmonics, unbalances, and frequency variations. This part further discusses the model fidelity of the SSMs of these PLLs that are used for the SO design. In the fourth section, a general design framework and the corresponding design process is developed to achieve an optimum trade-off between immunity to distortions and control bandwidth. Then, an experiment is designed and conducted to test PLLs and validate their models in various operational scenarios. The model validation indicates significant problems of the SSMs to predict the stability of PLLs with frequency adaptive filters, i.e., DSRF-PLL. Therefore, the proposed design framework

is extended to a multi-fidelity approach that can capture transient stability problems of PLLs. Finally, the optimum design parameters for five different PLLs are derived with the introduced multi-fidelity model-based design, and are evaluated considering immunity to distortions and control bandwidth. This study demonstrates that the design process can determine optimum control parameters for any SRF-based PLL. The design framework contains LSMs that can accurately predict the transient stability boundary even for nonlinear characteristics but fail to provide analytical insight into the mechanisms. Therefore, the last part of this chapter focuses on the transient stability phenomena and how to assess them with nonlinear analysis methods.

The SRF-PLL structure relies on the Clarke and Park transformation presented in section 3.2.3 [130], [119]. The Park transformation contains the unknown phase angle $\theta = \omega_1 t$ (see 3.6) that must be detected by the PLL for grid synchronization. Since Clarke's transformation is linear, the following derivation will assume $\mathbf{v}_{\alpha\beta}$ as measured input voltages in $\alpha\beta$-frame. The estimated phase angle θ' is used for Park's transformation $\mathbf{T}_{\mathrm{dq}}$. So, $\mathbf{T}_{\mathrm{PLL,dq}}$ denotes the transformation with θ' in the following calculations. Describing the grid voltages $\mathbf{v}_{\alpha\beta}$ according to 3.12 and assuming $\delta = \theta - \theta'$ as error of the estimated phase angle leads to the positive sequence voltage in dq-frame:

$$\mathbf{v}^{+}_{\mathrm{PLL,dq}} = \mathbf{T}_{\mathrm{PLL,dq}}\mathbf{v}_{\alpha\beta} = \underbrace{\hat{V}_{\mathrm{S},1}\begin{bmatrix}\cos(\delta)\\ \sin(\delta)\end{bmatrix}}_{\overline{\mathbf{v}}^{+}_{\mathrm{PLL,dq+}}} + \underbrace{\hat{V}_{\mathrm{S},-1}\begin{bmatrix}\cos\left(-2\omega_1 t+\delta+\delta_{-1}\right)\\ \sin\left(-2\omega_1 t+\delta+\delta_{-1}\right)\end{bmatrix}}_{\mathbf{v}^{-}_{\mathrm{PLL,dq+}}} + \underbrace{\sum_{n=-m}^{m}\hat{V}_{\mathrm{S},n}\begin{bmatrix}\cos\left((n-1)\omega_1 t+\delta+\delta_n\right)\\ \sin\left((n-1)\omega_1 t+\delta+\delta_n\right)\end{bmatrix}}_{\mathbf{v}^{n}_{\mathrm{PLL,dq+}}} \quad . \tag{5.1}$$

The harmonics and negative sequence components experience a frequency and angle shift according to $n\omega_1 t+\delta_n-\theta' = n\omega_1 t+\delta_n-\theta+\delta = (n-1)\omega_1 t+\delta_n+\delta$. If δ becomes very small, 5.1 provides an accurate estimation of the phase angle θ and the corresponding amplitude $\hat{V}_{\mathrm{S},1}$. A suitable feedback control with $\mathbf{v}^{+}_{\mathrm{PLL,dq}}$ as input could ensure $\delta \approx 0$ rad in steady-state, so that the linearized dq-components of the voltages $\Delta\mathbf{v}^{+}_{\mathrm{PLL,dq}}$ represent the fundamental grid voltage magnitude and phase angle according to:

$$\Delta\mathbf{v}^{+}_{\mathrm{PLL,dq}} = \hat{V}_{\mathrm{S},1}\begin{bmatrix}1\\ \delta\end{bmatrix} + \mathbf{v}^{-}_{\mathrm{PLL,dq+}} + \mathbf{v}^{n}_{\mathrm{PLL,dq+}} \quad . \tag{5.2}$$

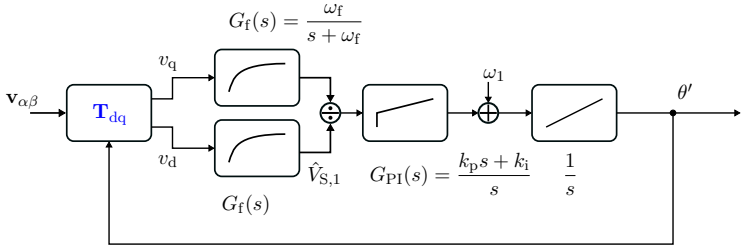


Figure 5.1: LSM of the LSRF-PLL.

Since $\Delta\overline{\mathbf{v}}^{+}_{\mathrm{PLL,dq+}}$ are dc-quantities in the steady-state, a PI-controller can be applied for controlling $\Delta v^{+}_{\mathrm{PLL,q}} = 0$ to achieve $\theta' \approx \theta$. Unfortunately, higher-order harmonics, i.e., $\mathbf{v}^{-}_{\mathrm{PLL,dq+}}$ and $\mathbf{v}^{n}_{\mathrm{PLL,dq+}}$, overlay the fundamental-frequency component and may disturb the controller output θ'.
Fig. 5.1 presents the feedback control for $\Delta v^{+}_{\mathrm{PLL,q}}$, considering Park's transformation. This plant is a type 2 control system, i.e., it includes two free integrators, which introduce two poles at the origin to guarantee zero steady-state error in response to frequency steps or phase angle jumps [131], [132]. Additionally, it contains a low-pass filter G_f with the frequency ω_f to filter out the voltage harmonics and an Amplitude Normalization Scheme (ANS) to normalize the controller input to the voltage magnitude $\hat{V}_{\mathrm{S},1}$ [133], [119]. The analysis of this control system is complex due to the trigonometric and algebraic nonlinearities.

The following investigation focuses on the dynamic characteristics of PLLs during grid faults. Consequently, the LSM is crucial for evaluating the large-signal behavior and the dynamic performance during severe transient processes. The disturbance rejection may affect the maximum control bandwidth of PLLs and can be described more efficiently by SSMs, since voltage harmonics are typically small compared to the fundamental frequency voltage component [38]. The LSM and SSM are thus used for the analysis and parameter design.
The LSM describes the data-sampled system with continuous grid voltage waveforms and discrete PLL algorithms. Tustin's transformation discretizes the PLL filters, and the same discretization is applied to the integrator of the angular frequency at the PLLs output. For some PLLs, Euler Forward discretization is used to prevent algebraic loops during execution. This is necessary since Tustin's transformation does not include an intrinsic delay. The sampling time is $T_\mathrm{s} = 100\ \mu$s and is identical to the execution time $T_\mathrm{s} = 100\ \mu$s of the *dSPACE MicroLabBox*. This sampling time does not critically affect the PLL performance since typical control bandwidths are in the range of 50-100 rad/s.
The LSRF-PLL can be linearized for the operating point $\delta = 0$ rad to obtain the SSM. The SSM simplifies the overall analysis without critically affecting the fidelity for small perturbations around an operating point. The Maclaurin series linearizes the non-linear

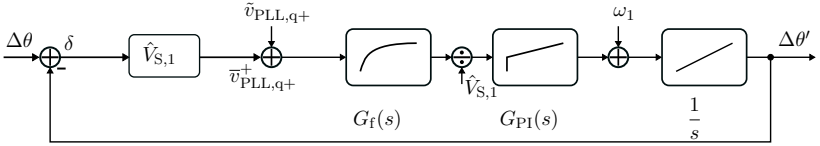


Figure 5.2: SSM of the LSRF-PLL.

trigonometric functions of the fundamental frequency terms $\overline{\mathbf{v}}^{+}_{\mathrm{PLL,dq+}}$. The time-dependent harmonics $\mathbf{v}^{-}_{\mathrm{PLL,dq+}}$ and $\mathbf{v}^{n}_{\mathrm{PLL,dq+}}$ are summed up to $\tilde{v}_{\mathrm{PLL,q+}}$ and serve as disturbance input of the system. The model neglects the dynamics of the ANS. These assumptions result in the SSM of the LSRF-PLL in Fig. 5.2, where Δ denotes the linearized input and output variables.

The structure in Fig. 5.2 contains three linear transfer functions to describe the dynamics of the estimated phase angle $\Delta\theta'$. These are the closed-loop transfer function $G_{\mathrm{cl}}(s)$ with the phase angle $\Delta\theta$ as input, the disturbance transfer function $G_{\mathrm{d}}(s)$ with the voltage harmonics and negative sequence voltage $\tilde{v}_{\mathrm{PLL,q+}}$ as input, and the feed-forward transfer function $G_{\mathrm{fw}}(s)$ with the nominal fundamental angular frequency ω_1 as input.

$$G_{\mathrm{ol}}(s) = G_{\mathrm{f}}\frac{1}{\hat{V}_{\mathrm{S},1}}G_{\mathrm{PI}}\frac{\hat{V}_{\mathrm{S},1}}{s} = \frac{k_{\mathrm{p}}\omega_{\mathrm{f}}\left(s+\frac{k_{\mathrm{i}}}{k_{\mathrm{p}}}\right)}{s^2\left(s+\omega_{\mathrm{f}}\right)} \tag{5.3}$$

$$G_{\mathrm{cl}}(s) = \frac{\Delta\theta'}{\Delta\theta} = \frac{G_{\mathrm{ol}}}{1+G_{\mathrm{ol}}} = \frac{k_{\mathrm{p}}\omega_{\mathrm{f}}s + k_{\mathrm{i}}\omega_{\mathrm{f}}}{s^3+\omega_{\mathrm{f}}s^2+k_{\mathrm{p}}\omega_{\mathrm{f}}s+k_{\mathrm{i}}\omega_{\mathrm{f}}} \tag{5.4}$$

The control transfer function in 5.4, derived from the open-loop transfer function given in 5.3, describes PLL dynamics during transients, such as phase jumps or frequency steps. The disturbance transfer function $G_{\mathrm{d}}(s)$ describes the disturbance rejection and is derived as follows:

$$G_{\mathrm{d}}(s) = \frac{\Delta\theta'}{\tilde{v}_{\mathrm{PLL,q+}}} = \frac{1}{\hat{V}_{\mathrm{S},1}}G_{\mathrm{cl}} \quad . \tag{5.5}$$

The feed-forward transfer function $G_{\mathrm{fw}}(s)$ can be expressed as:

$$G_{\mathrm{fw}}(s) = \frac{\Delta\theta'}{\omega_1} = \frac{1}{s+G_{\mathrm{f}}G_{\mathrm{PI}}} \quad . \tag{5.6}$$

Due to the constant feed-forward term, $G_{\mathrm{fw}}(s)$ is not of interest in the dynamic or steady-state analysis.

The step response and steady-state characteristics of the LSRF-PLL during different faults demonstrate the accuracy range of the SSM. During a three-phase fault (type A) with $\hat{V}_{\mathrm{S},1} = 0.05$ pu, and a large phase jump of $-\pi/2$, the SSM and LSM differ significantly, as shown in Fig. 5.3. In contrast, these models show similar results for the disturbance

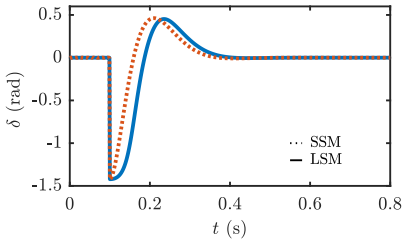


Figure 5.3: Comparison of the SSM and LSM results for the LSRF-PLL during a type A fault with $\hat{V}_{S,1} = 0.05$ pu.

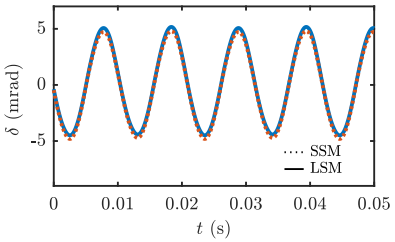


Figure 5.4: Comparison of the SSM and LSM results for the LSRF-PLL during a type E fault with maximum negative sequence component and $VUF \approx 1$.

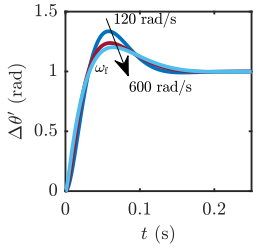


Figure 5.5: Phase jumps applied to G_{cl} with different filter cutoff frequencies ω_f.

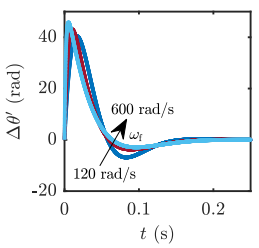


Figure 5.6: Frequency step applied to G_{cl} with different filter cutoff frequencies ω_f.

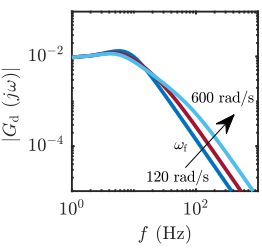


Figure 5.7: Bode plots of G_d with different filter cut-off frequencies ω_f.

rejection in steady-state during an unbalanced type E fault with $\hat{V}_{S,1} = 0.05$ pu in Fig. 5.4. For this exemplary test, the design parameters are $\omega_f = 65$ rad/s, $k_i = 279$ rad/s^2, and $k_p = 26.25$ rad/s. The corresponding design process is derived in section 5.7.

The LSRF-PLL has three design parameters. One for the low-pass filter: ω_f, and two for the PI-controller: k_p and k_i. All three affect the dynamic and steady-state characteristics. Dynamic behavior mainly includes the phase angle and frequency step responses. Fig. 5.5 and 5.6 show these responses for different filter cutoff frequencies ω_f. The results demonstrate that the rise time, settling time, and overshoot vary significantly depending on ω_f. Particularly the settling time decreases for larger ω_f.

The steady-state characteristic determine the PLL's disturbance rejection. The Bode plot of $G_d(s)$ is presented in Fig. 5.7 for different ω_f. It indicates a decrease in disturbance rejection for higher ω_f. This characteristic reveals the fundamental PLL design trade-off: An increase in control bandwidth (i.e, increasing ω_f) typically deteriorates the disturbance rejection. A suitable design process must identify an optimum design considering this trade-off.

Design processes typically require scenarios and performance indicators to evaluate fulfillment

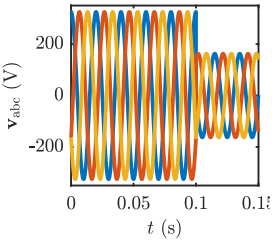


Figure 5.8: Grid voltages during a symmetrical fault (type A) with a $-90°$ phase jump.

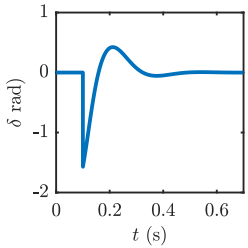


Figure 5.9: Phase angle error δ during a symmetrical fault (type A) with a $-90°$ phase jump.

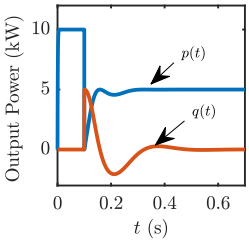


Figure 5.10: Converter active and reactive output power during a symmetrical fault (type A) with a $-90°$ phase jump.

of the design objective. Severe grid faults are suitable worst-case scenarios, and a type A fault with a phase jump of $-90°$ serves as an example for such a scenario (see Fig. 5.8). The performance indicators are commonly the step responses of the phase angle δ, as shown in Fig. 5.9. However, PLLs critically affect the power output of the converter, as indicated for the exemplary type A fault in Fig. 5.10. These characteristics highlight how important it is to consider the converter's power control to evaluate PLL designs.
The LSRF-PLL is a mature algorithm but has a low immunity to large negative sequence voltages during severe, unbalanced faults. Several approaches focus on advanced filter algorithms and different decoupling strategies to improve the immunity [119], [52], [124], [134], [122], [52], [119]. These strategies are mainly based on the algorithms presented in chapter 3.2.

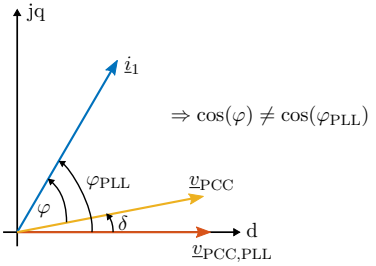
Based on the presented characteristics, three crucial questions arise that will be discussed throughout this chapter:

1. What is a realistic grid scenario to assess PLLs and which PLLs perform well in worst-case scenarios?

2. How can the PLL's impact on the converter power control be described and how can the fault response be improved during severe transients?

3. What is a suitable design framework and process to determine the optimum PLL design considering harmonics, unbalances, and frequency variations?

The investigations show critical transient instability phenomena occurring during severe faults. These are addressed with a proposed design process and an analytical approach based on Lyapunov's indirect and direct method.



$$\left.\frac{\mathrm{d}^2\ \cos(\varphi)}{\mathrm{d}\varphi^2}\right|_{\varphi_0} = -\cos(\varphi_0) \stackrel{!}{=} 0 \quad (5.7)$$

$$\varphi_0 = n\frac{\pi}{2}\ \mathrm{rad} \quad (5.8)$$

$$n := \{1, 3, 5, ...\} \quad (5.9)$$

Figure 5.11: Power factor description based on phase angle φ and its dependency on δ.

5.1 Converter Control Requirements and Worst-Case Grid Scenarios considering Severe Network Disturbances and Converter Fault Current Injection

Grid codes provide the converter requirements for FRT and normal operation [13, p.15], [67, p.18], [11]. Two requirements are particularly critical for the converter control. First, grid codes define the accuracy of active and reactive power supply defined by the active factor $\cos(\varphi)$ [12, p.57]. Second, the grid operator requires a maximum settling time for the reactive current during FRT [13, p. 15], [67, p. 18], [11].
The active factor $\cos(\varphi)$ is equivalent to the power factor λ, if the active and reactive power caused by harmonics in the voltages and currents are neglectable. Consequently, $\lambda \approx \cos(\varphi)$ is assumed in the following analysis, and λ obviously depends on the phase φ between grid voltages and injected converter currents. The error of the estimated phase angle δ changes λ since it defines the reference voltage for the converter's current control, as depicted in Fig 5.11. If δ is not zero, the phase angle of the grid φ and the phase angle of the current control φ_{PLL} will differ and lead to a difference between λ and λ_{PLL}, which is defined as maximum power factor deviation $\tilde{\lambda} = \lambda - \lambda_{\mathrm{PLL}}$. The subscript PLL denotes the orientation of the converter control based on the estimated phase angle θ'. A worst-case error estimation defines the operating point φ_0 where δ has the largest impact on $\tilde{\lambda}$. This is necessary since $\tilde{\lambda}$ has a nonlinear relation to δ and φ. The second order derivative of $\lambda = \cos(\varphi)$ defines this worst-case operating point of φ according to 5.7. For simplicity $n := 1$ is chosen to derive this critical point, which occurs at $\varphi_0 = \pi/2$.

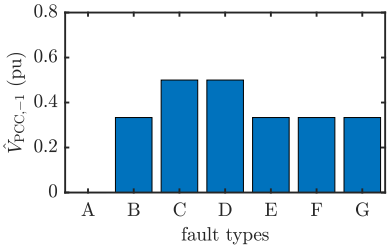


Figure 5.12: Normalized negative sequence fundamental voltage component $\hat{V}_{\mathrm{PCC},-1}$ for different fault types.

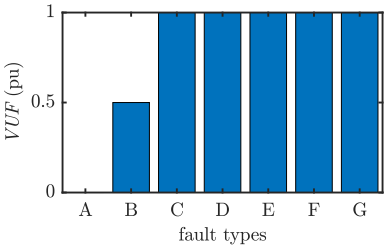


Figure 5.13: Maximum unbalance factor VUF for different fault types.

The critical operating point φ_0, the characteristics in Fig. 5.11, and the maximum power factor error $\tilde{\lambda}_{\max}$ lead to the maximum permissible phase angle error $\delta_{\max}$:

$$\pm\tilde{\lambda}_{\max} = 0.005 \text{ pu} = \lambda - \lambda_{\mathrm{PLL}} = \cos(\varphi_0) - \cos(\varphi_0 + \delta_{\max}) = \sin(\delta_{\max}) \tag{5.10}$$

$$\Rightarrow \delta_{\max} = \pm\mathrm{asin}(\tilde{\lambda}_{\max}) \approx \pm\tilde{\lambda}_{\max} \text{ rad} = \pm 0.005 \text{ rad} = \pm 0.286^\circ \tag{5.11}$$

$\tilde{\lambda}_{\max}$ is set to 0.005 pu according to [12, p.57] and serves as requirement for the maximum permissible error of the estimated phase angle of the PLL.

Harmonics in the grid voltages and large negative sequence components may distort δ, and thus affect $\tilde{\lambda}$ in steady-state (Table 3.3 [38], [52, p.35]). The PLL-SSM in Fig. 5.2 indicates that only the q-components of the Park transformed grid voltages $\tilde{v}_{\mathrm{PLL,q+}}$ influence δ. Therefore, the limits given in EN 50160 are transformed into the dq-domain. However, the negative and positive sequence of the harmonics may compensate each other in dq-domain, not representing the worst-case spectrum. Therefore, only the negative sequence harmonics are considered to determine $\tilde{v}_{\mathrm{PLL,q+}}$ because they have the largest amplitudes according to Table 3.3. Additionally, large negative sequence voltages of unbalanced grid faults have the same effect on δ as the harmonics. Analyzing the fault types shows that type C and D result in the maximum negative sequence voltage, as shown in Fig. 5.12. However, the Amplitude Normalization Scheme (ANS) normalizes the negative sequence components and harmonics with the positive sequence voltage. This normalization corresponds to the definition of the voltage unbalance factor (VUF). Fig. 5.13 shows the VUF for all fault types and indicates that type C to G yield the same normalized negative sequence component of 1 pu. This high disturbance compared to the harmonics in normal operation requires large attenuation of the negative sequence to limit the maximum distortion of the phase angle.

The worst-case grid voltage spectrum in dq-domain is shown in Fig. 5.14 and contains the voltage harmonics at different frequencies and the maximum negative sequence voltage at 100 Hz. The harmonics and negative sequence voltages will vary in their frequency due

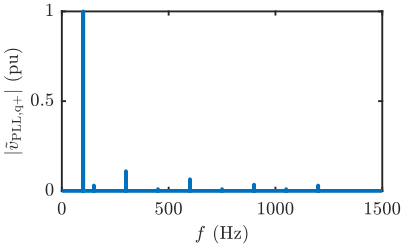


Figure 5.14: Worst-case spectrum of the grid voltage for the nominal grid frequency $f_1 = 50$ Hz, according to EN 50160 [38].

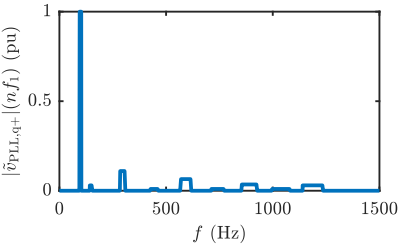


Figure 5.15: Superimposed worst-case spectrum of the grid voltage considering frequency drifts (47.5 Hz $< f_1 <$ 51.5 Hz) of the fundamental frequency voltage and the corresponding harmonics.

to variations in the fundamental grid frequency in the range of 47.5 Hz $< f_1 <$ 51.5 Hz. Therefore, they may occur in a frequency band around their nominal operating point. Combining all these possible spectra for different fundamental frequencies leads to the superimposed worst-case spectrum in Fig. 5.15, which serves as operational scenario to assess the immunity to distortions of PLLs.

In contrast to the immunity to distortions, which describes the steady-state characteristics, the dynamic requirements mainly focus on the step response of the converter current during severe grid faults. Typically, the converter has to provide reactive current depending on the positive sequence voltage $\hat{V}_{\mathrm{PCC,1}}$. Hence, two crucial operating point variables change almost simultaneously. First, the grid voltages experience large amplitude steps and phase angle jumps. The PLL must detect these changes quickly to inject active and reactive power accurately, as explained in Fig. 5.11. Second, the converter reference currents change with $\hat{V}_{\mathrm{PCC,1}}$ to support the grid voltages according to the grid codes.
The amplitude steps and phase angle jumps predominantly depend on the fault type and the fault impedance to the source impedance ratio $\underline{Z}_{\mathrm{F}}/\underline{Z}_{\mathrm{S}}$. The amplitude steps change with the magnitude of the impedance ratio, whereas the grid phase angle jump mainly depends on the impedance angles (see section 3.3.1). Fig. 5.16 shows the maximum phase jump $\Delta\hat{\theta}$ for the different fault and grid types (lv - low-voltage, mv - medium voltage, and hv - high voltage). The grid voltage level defines the $r_{\mathrm{S}} = X_{LS}/R_{\mathrm{S}}$-ratio of the source impedance $\underline{Z}_{\mathrm{S}}$ according to Table 3.1. The $r_{\mathrm{F}} = X_{LF}/R_{\mathrm{F}}$-ratio of the fault impedance $\underline{Z}_{\mathrm{F}}$ is varied between 0...10 to derive $\Delta\hat{\theta}$ for every fault type and voltage level. Type A faults show the largest phase angle jumps of approximately $\pi/2$ for $\underline{Z}_{\mathrm{F}}\approx 0$ pu and $r_{\mathrm{F}} = 10$ for the lv-grid or $r_{\mathrm{F}} = 0$ for the hv-grid, respectively. The unbalanced fault types E, F, and G produce the largest phase angle jump with $\Delta\hat{\theta} = 0.41$ rad for $\underline{Z}_{\mathrm{F}}\approx 1$ pu.
The positive sequence voltage amplitude also experiences the largest sag for the type A fault, whereas the single-phase fault (type B) shows the lowest sag depth. The unbalanced type E, F, and G faults show the largest sag depth of 0.66 pu for $\underline{Z}_{\mathrm{F}}\approx 0$ pu. The results for

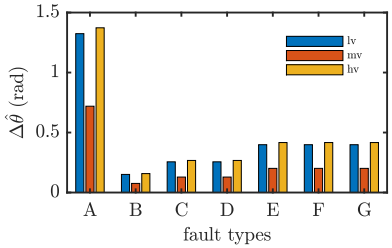


Figure 5.16: Maximum phase jump $\Delta\hat{\theta}$ for different fault types.

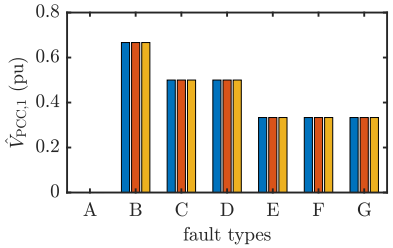


Figure 5.17: Normalized positive sequence fundamental voltage component $\hat{V}_{\mathrm{PCC,1}}$ for different fault types.

all fault types are summarized in Fig. 5.17. In summary, type A faults are the most severe disturbances for the converter control and PLLs, since they lead to the largest voltage sags, and phase angle jumps. The most severe unbalanced faults are of type E, F, and G.

The converter must provide reactive current during grid faults depending on the positive sequence voltage [11], i.e., the converter must inject q-current for an accurately locked dq-system with $\delta = 0$. In contrast to [135], new grid codes do not mention a deadband for reactive current provision [11]. Nonetheless, normal and abnormal grid conditions are not treated separately by the grid operator who sets the power factor and FRT commands. Since the reactive current steps in response to voltage drops below 10% are very small, these are out of the scope of this investigation, and the following analysis focuses on faults starting at $0.9\hat{V}_{\mathrm{S,1}}$.
Fig. 5.18 shows the active and reactive or d and q-reference current, respectively, for different positive sequence voltage magnitudes $\hat{V}_{\mathrm{PCC,1}}$, considering a converter current limitation to 1 pu. The magnitude $\hat{V}_{\mathrm{PCC,1}}$ is denoted with V^+ in the figures for better readability. The corresponding power factor characteristics in Fig. 5.19 are identical to the currents in their normalized form.
Grid codes require maximum rise and settling times for the q-currents or reactive current, respectively. The grid codes slightly differ in their requirements, and the most recent VDE-AR-N 4110 demands a maximum rise time of 20 ms and settling time of 60 ms considering a tolerance band of 10% [11]. These timing requirements are crucial for fast grid voltage support. After fault clearing, the reactive current must quickly decrease to its pre-fault value to prevent overvoltages [58].

Table 5.1 summarizes the results for the worst-case scenario and the control requirements of RES converters. The PLLs must ensure the required disturbance rejection for the power factor and quick step response of the reactive current during the worst-case scenarios of type E and type A faults. The type E fault is the worst-case for the immunity to distortions due to the high VUF. The type A fault serves as worst-case for the dynamics since it contains

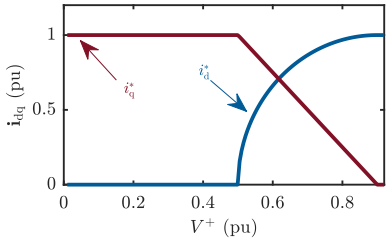


Figure 5.18: Active and reactive current references during faults according to VDE [11].

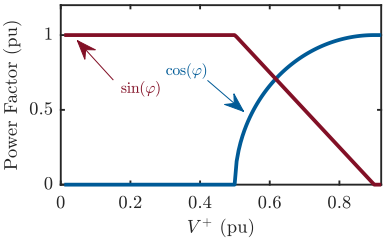


Figure 5.19: Power factor references derived with current reference requirements according to [11].

Table 5.1: Converter requirements and parameters for the worst-case grid scenarios.

Quantity	Value	Comment
$\tau_{\text{set},iq}$	60 ms	Settling time of reactive current in 10% tolerance.
$\tau_{\text{rise},iq}$	20 ms	Rise time of reactive current in high voltage grid.
$\delta_{\max}$	0.005 pu	Maximum error of the estimated phase angle.
$\hat{V}_{\text{PCC,1,min}}$	0.05 V	Minimum positive sequence voltage amplitude.
f_1	47.5 Hz $< f_1 <$ 51.5 Hz	Range of the fundamental frequency.
$\hat{V}_{\text{PCC},-1}$	1 pu	Maximum negative sequence voltage amplitude.
$\tilde{v}_{\text{PLL,q+}}$	see spectrum Fig. 5.15	q-component of the voltage harmonics.

the largest $\Delta\hat{\theta}$ jump and $\hat{V}_{\text{PCC,1}}$ sag. The minimum positive sequence voltage $\hat{V}_{\text{PCC,1,min}}$ is assumed to be 0.05 pu according to [13].
Since the LSRF-PLL cannot sufficiently deal with large unbalances, several PLLs are proposed in the literature to increase the control bandwidth while conserving the immunity to distortions. These can be divided into sequence decomposition-based PLLs and PLLs with prefilter. To assess their performance during the derived worst-case scenarios, their accurate disturbance and control transfer functions are necessary, which are derived in the following section.

5.2 Control and Disturbance Characterization of Online Symmetrical Component Decomposition

The analysis in section 3.2 identified Clarke's and Park's transformation as suitable tools for symmetrical component decomposition. The decomposition in $\alpha\beta$-frame needs a 90° phase-lag operator that is realized with a Second Order Generalized Integrator (SOGI) algorithm containing two integrators. The decomposition in the dq-frame is based on the DSRF, which decouples the positive and negative sequences by applying two different reference frames in the positive and negative sequence. These algorithms are interesting for PLLs since the

decomposition extracts the positive sequence voltage and rejects the negative sequence. This characteristic increases the filter capability of the PLLs, but may introduce additional transfer characteristics and feedback loops that affect dynamic behavior and stability.

5.2.1 Dual Synchronous Reference Frame (DSRF)

The DSRF is a decoupling method to extract symmetrical components in the dq-frame. The characteristics of Park's transformation for positive and negative sequence components were already derived in section 3.2. Rearranging 3.30 and A.12 leads to the basic idea of the decoupling strategy for the DSRF summarized in 5.12 and 5.13 and shown in Fig. 5.20.
The Park matrices with θ' and $-\theta'$ for the positive and negative sequence voltage, respectively, transform the grid voltages $\mathbf{v}_{\alpha\beta}$ into their dq-components. These components still contain harmonics and the negative or positive sequence coupling component denoted by $\mathbf{T}_{\mathrm{dq}^{-2}}\overline{\mathbf{v}}^{+}_{\mathrm{dq}}$ or $\mathbf{T}_{\mathrm{dq}^{+2}}\overline{\mathbf{v}}^{-}_{\mathrm{dq}}$, respectively. Then, a low-pass filter extracts the dc-components $\overline{\mathbf{v}}^{+}_{\mathrm{dq}}$ and $\overline{\mathbf{v}}^{-}_{\mathrm{dq}}$. These can be transformed back with $\mathbf{T}_{\mathrm{dq}^{-2}}$ and $\mathbf{T}_{\mathrm{dq}^{+2}}$ with $-2\theta'$ and $2\theta'$, respectively, to get the decoupling terms to compensate for $2\omega_1$ oscillations caused by the opposite sequence component. Finally, the positive and negative sequence voltages in dq-frame, i.e, $\mathbf{v}^{+}_{\mathrm{dq}}$ and $\mathbf{v}^{+}_{\mathrm{dq}}$, respectively, are obtained according to:

$$\overline{\mathbf{v}}^{+}_{\mathrm{dq}} = \mathbf{v}^{+}_{\mathrm{dq}} - \mathbf{T}_{\mathrm{dq}^{+2}}\overline{\mathbf{v}}^{-}_{\mathrm{dq}} - \sum_{n=-\infty}^{m} \mathbf{T}_{\mathrm{dq}^{-(n-1)}}\overline{\mathbf{v}}^{n}_{dq} \quad , \tag{5.12}$$

$$\overline{\mathbf{v}}^{-}_{\mathrm{dq}} = \mathbf{v}^{-}_{\mathrm{dq}} - \mathbf{T}_{\mathrm{dq}^{-2}}\overline{\mathbf{v}}^{+}_{\mathrm{dq}} - \sum_{n=-\infty}^{m} \mathbf{T}_{\mathrm{dq}^{-(n+1)}}\overline{\mathbf{v}}^{n}_{\mathrm{dq}} \quad . \tag{5.13}$$

$\overline{\mathbf{v}}^{+}_{\mathrm{dq}}$ can be directly used to detect the phase angle with a conventional SRF-PLL. The block diagram containing the DSRF, the 1st-order low-pass filter $G_{\mathrm{f,DSRF}}(s)$ (see 5.14), and the SRF-PLL is shown in Fig. 5.20.

$$G_{\mathrm{f,DSRF}}(s) = \frac{\omega_{\mathrm{f}}}{s + \omega_{\mathrm{f}}} \tag{5.14}$$

Compared to the SSM of the LSRF-PLL, the SSM of the DSRF-PLL uses the same assumptions for linearizing the PLL but additionally assumes an ideal phase angle tracking for the decoupling structure, i.e., $\delta = 0$ for $\mathbf{T}_{\mathrm{dq}^{-2}}$ and $\mathbf{T}_{\mathrm{dq}^{+2}}$. This is, of course, not valid for severe grid faults but leads to the LTI description and SSM in Fig. 5.21. The linear transfer functions H_{21} and H_{21} were already derived in several publications and are given in 5.15 and 5.16 [52, pp.189-192]. The SSM fidelity of the DSRF for severe grid faults is discussed in section 5.7.

$$H_{21} = \frac{2\omega_{\mathrm{f}}^2\omega_1 s}{s^4 + 4\omega_{\mathrm{f}}s^3 + 4\left(\omega_{\mathrm{f}}^2 + \omega_1^2\right)s^2 + 8\omega_{\mathrm{f}}\omega_1^2 s + 4\omega_{\mathrm{f}}^2\omega_1^2} \tag{5.15}$$

$$H_{22} = \frac{\omega_{\mathrm{f}}\left(s^3 + 2\omega_{\mathrm{f}}s^2 + 4\omega_1^2 s + 4\omega_{\mathrm{f}}^2\omega_1^2\right)}{s^4 + 4\omega_{\mathrm{f}}s^3 + 4\left(\omega_{\mathrm{f}}^2 + \omega_1^2\right)s^2 + 8\omega_{\mathrm{f}}\omega_1^2 s + 4\omega_{\mathrm{f}}^2\omega_1^2} \tag{5.16}$$

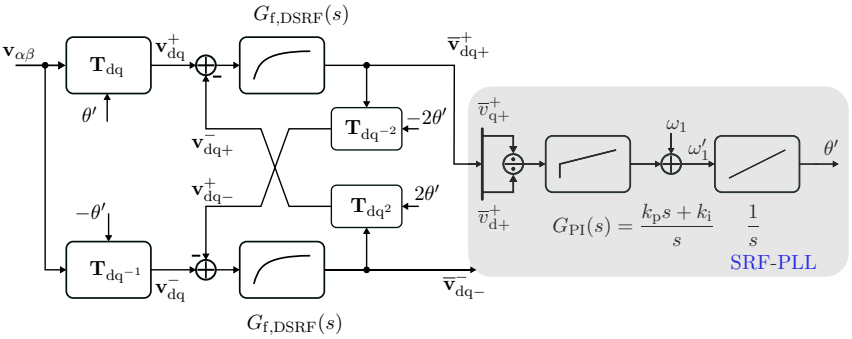


Figure 5.20: LSM of the DSRF.

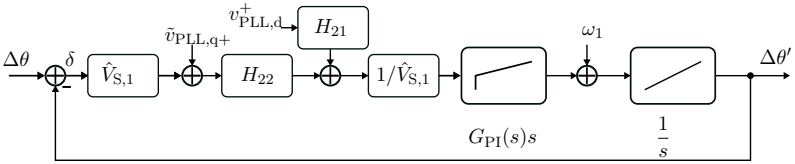


Figure 5.21: SSM of the DSRF.

Based on the SSM, the control transfer function $G_{\mathrm{cl,DSRF}}(s)$ is derived to describe the system response to phase angle jumps. According to 5.17, the transfer function is of fourth-order, and depends on the PLL design parameters and the fundamental frequency operating point ω_1.

$$G_{\mathrm{cl,DSRF}}(s) = \frac{\Delta\theta'}{\Delta\theta} = \frac{H_{22}(s)\,(k_{\mathrm{p}}s + k_{\mathrm{i}})}{s^2 + H_{22}(s)\,(k_{\mathrm{p}}s + k_{\mathrm{i}})} \tag{5.17}$$

In contrast to the LSRF-PLL, the DSRF-PLL has two significant disturbance transfer functions. Harmonics in the q-voltage component $\tilde{v}_{\mathrm{PLL,q+}}$ distort the estimated phase angle θ' according to 5.18, and the harmonics in the d-voltage component $\tilde{v}_{\mathrm{PLL,d+}}$ also affect the θ' distortions according to 5.19. However, the two disturbance inputs, i.e., $\tilde{v}_{\mathrm{PLL,q+}}$ and $\tilde{v}_{\mathrm{PLL,d+}}$, can be combined to obtain one disturbance transfer function, which is more convenient for further analysis. The transfer function H_{21} has zero gain for dc-components in $v^{+}_{\mathrm{PLL,d}}$ and thus the input can be simplified to $v^{+}_{\mathrm{PLL,d}} \approx \tilde{v}_{\mathrm{PLL,d+}}$, which only contains oscillatory components. This simplification enables a unified transfer function for both disturbance inputs assuming that $\tilde{v}_{\mathrm{PLL,q+}} e^{-\mathrm{j}\frac{\pi}{2}} \approx \tilde{v}_{\mathrm{PLL,d+}}$, i.e., the harmonics in the q-voltage are a 90° phase lead version

of the d-voltage harmonics in the steady-state. This leads to the unified complex transfer function $G_{\mathrm{d,dq,DSRF}}(s)$ given in 5.20 that can be used to calculate the harmonics in θ'.

$$G_{\mathrm{d,DSRF}}(s) = \frac{\Delta\theta'}{\tilde{v}_{\mathrm{PLL,q+}}}\bigg|_{v^{+}_{\mathrm{PLL,d}}=0} = \frac{1}{\hat{V}_{\mathrm{S,1}}} G_{\mathrm{cl,DSRF}}(s) \tag{5.18}$$

$$G_{\mathrm{d,2,DSRF}}(s) = \frac{\Delta\theta'}{v^{+}_{\mathrm{PLL,d}}}\bigg|_{\tilde{v}_{\mathrm{PLL,q+}}=0} = \frac{1}{\hat{V}_{\mathrm{S,1}}} \frac{H_{21}(s)\,(k_{\mathrm{p}}s + k_{\mathrm{i}})}{s^2 + H_{22}(s)\,(k_{\mathrm{p}}s + k_{\mathrm{i}})} \tag{5.19}$$

$$G_{\mathrm{d,dq,DSRF}}(s) = \frac{\Delta\theta'}{\tilde{v}_{\mathrm{PLL,q+}}} = G_{\mathrm{d,DSRF}}(s) + G_{\mathrm{d,2,DSRF}}(s) e^{-\mathrm{j}\frac{\pi}{2}} \tag{5.20}$$

Fig. 5.22 and 5.23 show the SSM and LSM results for a type A and type E fault with $|\underline{Z}_{\mathrm{F}}|$=0.05 pu, r_{F}=0 pu, and r_{S}=1 pu. The low fault impedance magnitude and large change in the impedance ratio lead to large phase angle jumps and amplitude step. The PLL design parameters are set to $\omega_{\mathrm{f}} = 168$ rad/s, $k_{\mathrm{i}} = 2402$ rad/s^2, and $k_{\mathrm{p}} = 74$ rad/s according to the design process presented in section 5.7. The SSM predicts a much slower response with a smaller overshoot than the LSM. This characteristic is a first indicator that an analysis based on the SSM may predict a larger stability margin, which is critical since it may lead to wrong design decisions. In contrast, the SSM shows only minor differences to the LSM for the disturbance rejection results presented in Fig. 5.23 and accurately predicts the distortions during a type E fault with large VUF. This high SSM accuracy was expected due to the small amplitudes of the harmonics.

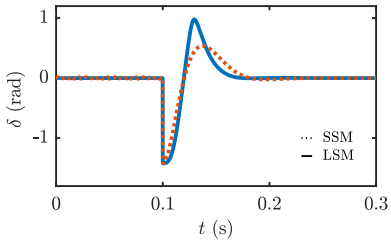


Figure 5.22: Comparison of SSM and LSM results for the phase angle step response of the DSRF-PLL during a type A fault with $\hat{V}_{\mathrm{S,1}} = 0.05$ pu.

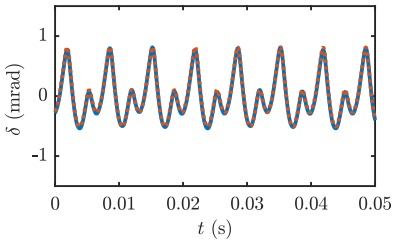


Figure 5.23: Comparison of SSM and LSM results for the distortions in θ' of the DSRF-PLL during a type E fault with maximum negative sequence component and VUF=1.

5.2.2 Dual Second Order Generalized Integrator (DSOGI)

The DSOGI is a sequence decomposition algorithm in $\alpha\beta$-frame using two Second Order Generalized Integrators (SOGIs), which are ideal integrators for sinusoidal inputs. They can

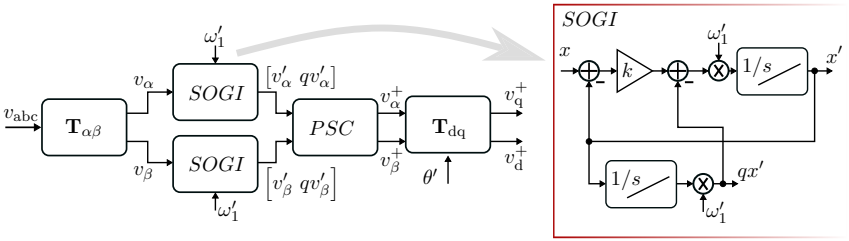


Figure 5.24: LSM of the DSOGI.

be utilized to generate a 90° phase lagged signal from a sinusoidal input, and thus to realize the q-operator according to 3.21. The SOGI algorithm contains the two integrators, the gain k, and the estimated frequency ω_1'. Fig. 5.24 shows the DSOGI with two SOGI blocks and a Positive Sequence Calculator (PSC) containing the matrix given in 3.21, which calculates the positive sequence of the input voltages. The positive sequence voltage $\mathbf{v}^+_{\alpha\beta}$ are then used as input for a standard SRF-PLL to estimate the phase angle θ' (comparable to the DSRF-PLL in Fig. 5.20). The estimated frequency of the PLL can be used for ω_1' to make the SOGI frequency adaptive. However, a constant ω_1' tuned to the fundamental grid frequency may also achieve satisfactory results for small frequency deviations.

In $\alpha\beta$-frame, the SOGI can be described by the linear transfer functions:

$$\frac{x'_\alpha}{x_\alpha} = \frac{x'_\beta}{x_\beta} = \frac{k\omega_1' s}{s^2 + k\omega_1' s + \omega_1'^2} \quad , \qquad \frac{qx'_\alpha}{x_\alpha} = \frac{qx'_\beta}{x_\beta} = \frac{k\omega_1'^2}{s^2 + k\omega_1' s + \omega_1'^2} \quad . \tag{5.21}$$

These expressions assume that the grid frequency ω_1 is equal to the estimated frequency ω_1'. In contrast to the SOGI, the DSOGI-PLL has no direct LTI representation since the SOGI does not have a constant operating point but an operating trajectory in the dq-frame, so that the linearization of the PLL-structure is not straightforward. Two possibilities exist to linearize the system: First, Linear Time-Periodic (LTP) methods can be used to linearize the system based on operating trajectories, but the analysis is rather complex. Second, the equivalence to other decomposition structures, i.e, the DSRF, can be exploited.
Fortunately, the DSRF model sufficiently describes the SSM characteristics of the DSOGI for small deviations from the frequency operating point, enabling equivalent tuning of the design parameters of DSOGI and DSRF [52], [124]. Ref. [124] and [52] prove that the SSMs of DSRF or Multiple Reference Frame (MRF) (proposed in [136]) and DSOGI are identical for $2\omega_{f,DSRF} = k\omega_1'$. Of course, frequency and phase angle transients that affect ω_1' lead to differences in the large-signal characteristics.

For verification, the models are tested using the same scenarios as the DSRF-PLL simulations achieving similar results. The PLL parameters are $k = 0.875$ rad/s, $k_i = 1484$ rad/s^2, and

$k_\mathrm{p} = 63.88$ rad/s, which are obtained from the design process presented in section 5.7. The transient response for a severe type A fault in Fig. 5.25 shows significant deviations of the SSM and LSM. The LSM predicts a larger overshoot than the SSM. The estimated phase angle distortions show only minor differences between SSM and LSM but reveal larger uncertainties compared to DSRF models (compare Fig. 5.23). These simulation results indicate that the DSRF-SSM approximates the DSOGI characteristics but does not capture all effects, and shows differences beyond simple linearization errors.

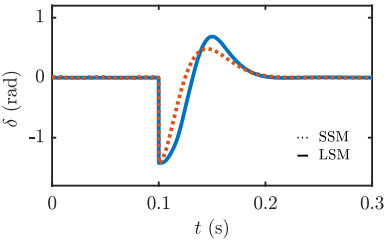


Figure 5.25: Comparison of SSM and LSM results for the phase angle step responses of the DSOGI-PLL during a type A fault with $\hat{V}_{\mathrm{S},1} = 0.05$ pu.

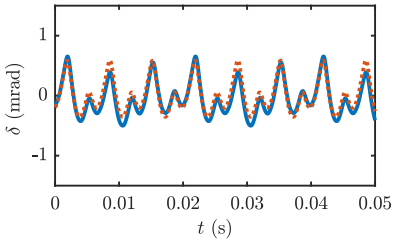


Figure 5.26: Comparison of SSM and LSM results of the distortions in θ' of the DSOGI-PLL during a type E fault with maximum negative sequence component and VUF=1.

5.3 Control and Disturbance Characterization for PLLs with Prefilters

The presented decomposition algorithms rely on the sequence calculation in dq-frame and $\alpha\beta$-frame. A second possibility exploits the characteristic that the positive and negative sequence components occur at different frequencies in the dq-frame. Several filter approaches realize the desired sequence decomposition by filtering the input signals and attenuating the negative sequence voltage or harmonics.

The sequence extraction needs a high attenuation in a narrow frequency band since positive and negative sequence components are very close to each other in the frequency domain. The Notch-filter (Nf) is the fundamental filter structure to attenuate signals in a narrow frequency band. The Bode plots of the DSRF-PLL (see Fig. 5.41) already show a Nf characteristic for the negative sequence. In general, narrowband filters reject single dominant harmonics without critically affecting the bandwidth, such as low-pass filters, but may deteriorate stability. This thesis focuses on two different filter structures: Notch-filters (Nfs) and Moving Average Filters (MAFs).

5.3.1 Notch-filter (Nf)

The Nf transfer function given in 5.22 describes its input-output characteristic. The natural frequency ω_n sets the eigenfrequency of the maximum attenuation, and the damping factor $\zeta_{\mathrm{f,Notch},n}$ determines the width of the attenuation peak. The eigenfrequency ω_n must be tuned to $2\omega_1$ to reject the negative sequence component in the dq-frame. Moreover, several dominant grid voltage harmonics can be rejected by using Nfs in a sequence tuned to different $\omega_{\mathrm{n},n}$, according to:

$$G_{\mathrm{f,Notch},n}(s) = \prod_{n=2}^{m} \frac{s^2 + \omega_{\mathrm{n},n}^2}{s^2 + 2\zeta_{\mathrm{f,Notch},n}\omega_{\mathrm{n},n}s + \omega_{\mathrm{n},n}^2} \quad . \tag{5.22}$$

The Nf can be simply integrated into the LSRF-PLL by replacing the low-pass filter. This results in the Nf-PLL that has the same block diagram as the LSRF-PLL in Fig. 5.2 except for the filter. The transfer functions of the SSM in 5.23 and 5.24 are also similar to the LSRF-PLL and rely on the same assumptions.

$$G_{\mathrm{cl,Notch}}(s) = \frac{\theta'}{\theta} = \frac{G_{\mathrm{Notch},n}(s)\,(k_\mathrm{p}s + k_\mathrm{i})}{s^2 + G_{\mathrm{Notch},n}(s)\,(k_\mathrm{p}s + k_\mathrm{i})} \tag{5.23}$$

$$G_{\mathrm{d,Notch}}(s) = \frac{\theta'}{\tilde{v}_{\mathrm{PLL,q+}}} = \frac{1}{\hat{V}_{\mathrm{S},1}} G_{\mathrm{cl,Notch}}(s) \tag{5.24}$$

Again, the models are tested and verified during a type A and type E fault with $|\underline{Z}_\mathrm{F}|$=0.05 pu, r_F=0 pu, and r_S=1 pu. The tested Nf-PLL contains three cascaded notch-filters tuned to the angular frequencies $2\omega_1$, $3\omega_1$, and $6\omega_1$. The other design parameters are $\zeta_{\mathrm{f,Notch}} = 1.03$, $k_\mathrm{i} = 2016$ rad/s^2, and $k_\mathrm{p} = 78.54$ rad/s. How these parameters are derived based on the grid requirements is shown in section 5.7. In contrast to the DSRF and DSOGI-PLL, the SSM yields similar characteristics as the LSM for the transients and steady-state distortions. The reason may be that the Nf-PLL is not frequency adaptive, which reduces the number of assumptions for deriving the SSM. However, the overshoot is slightly larger in the LSM results than predicted by the SSM.

The Nf is a potent algorithm to reject the negative sequence voltage component in PLL algorithms. It can also sufficiently reject harmonics in the grid voltages. However, the dominant harmonics must be known a priori to tune the natural frequencies of the cascaded Nf. MAFs may provide a more efficient solution to reject all harmonics with frequencies that are multiples of the fundamental grid frequency.

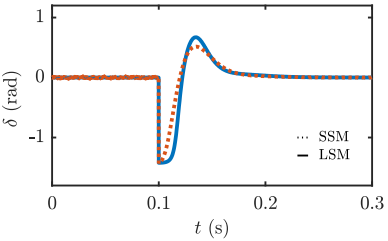


Figure 5.27: Comparison of SSM and LSM of the Nf-PLL during a type A fault with $\hat{V}_{S,1} = 0.05$ pu.

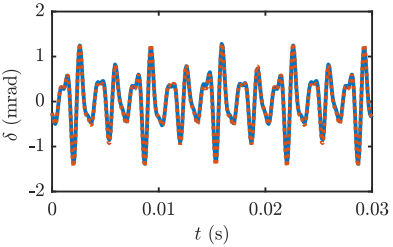


Figure 5.28: Comparison of SSM and LSM of the Nf-PLL during a type E fault with maximum negative sequence component and VUF=1.

5.3.2 Enhanced Moving Average Filter with Prefiltering Stage (EPMAF)

The Enhanced Moving Average Filter with Prefiltering Stage (EPMAF)-PLL is based on Moving Average Filters (MAFs) described by the transfer functions:

$$G_{\mathrm{MAF}}(s) = \frac{1 - e^{-sT_{\mathrm{MAF}}}}{sT_{\mathrm{MAF}}} \Rightarrow \qquad G_{\mathrm{MAF}}(z) = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}} \quad . \tag{5.25}$$

They contain a deadtime term and an integrator tuned with the averaging time constant T_{MAF}. This filter shows a Nf characteristic for all frequencies that are integer multiples of $1/T_{\mathrm{MAF}}$, and thus rejects all harmonics with these frequencies. This function is not linear, but the deadtime has an accurate representation in the z-domain, and its discrete transfer function with $NT_{\mathrm{s}} = T_{\mathrm{MAF}}$ is given in 5.25 [137],[120].
The MAF serves as a prefilter for the SRF-PLL to reject the negative sequence voltages and voltage harmonics. It is applied to the dq-transformed voltages using an angle $\overline{\theta}$ generated with a constant frequency and arbitrarily chosen starting angle. The filtered voltages are processed in the SRF-PLL structure, as shown in Fig. 5.29. As a drawback, the algorithm suffers from steady-state error in the amplitude and frequency detection as presented in [120]. Therefore, the EPMAF-PLL consists of an additional amplitude and phase error correction, which were proposed by Golestan in [120]. Details on the mathematical background are provided in [120] and not repeated here. The additional parameters k_v and k_φ of the EPMAF-PLL result directly from the MAF design parameters as follows:

$$k_\varphi = \frac{1}{2}\left(T_{\mathrm{MAF}} - T_{\mathrm{s}}\right) \quad , \qquad k_v = T_{\mathrm{MAF}}^2/24 \quad . \tag{5.26}$$

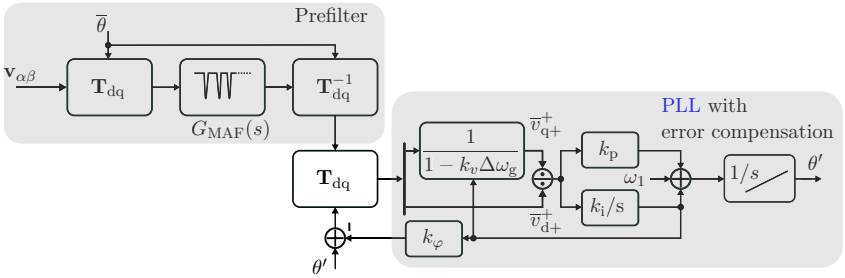


Figure 5.29: LSM of the EPMAF-PLL.

The control transfer function was already derived in [120] and is given in 5.27 for the sake of completeness. The disturbance transfer function in 5.28 is derived based on this control transfer function. These two functions describe the SSM of the EPMAF-PLL.

$$G_{\mathrm{cl,MAF}}(s) = \frac{\theta'}{\theta} = \frac{k_{\mathrm{p}}s + k_{\mathrm{i}}}{s^2 + (k_{\mathrm{p}} - k_{\mathrm{i}}k_\varphi)\, s + k_{\mathrm{i}}} G_{\mathrm{MAF}}(s) \tag{5.27}$$

$$G_{\mathrm{d,MAF}}(s) = \frac{\theta'}{\tilde{v}_{\mathrm{PLL,q+}}} = \frac{1}{\left(\hat{V}_{\mathrm{S},1} + \hat{V}_{\mathrm{S},-1}\right)} G_{\mathrm{cl,MAF}}(s) \tag{5.28}$$

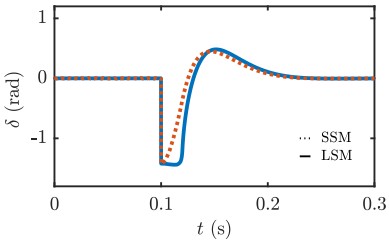


Figure 5.30: Comparison of SSM and LSM results for the phase angle step response of the EPMAF-PLL during a type A fault with $\hat{V}_{\mathrm{S},1} = 0.05$ pu.

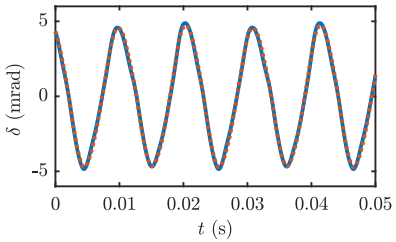


Figure 5.31: Comparison of SSM and LSM results for the distortions in θ' of the EPMAF-PLL during a type E fault with maximum negative sequence component and VUF=1.

A first test of the SSM for the transient and steady-state characteristics in the same scenario as the Nf-PLL shows just minor differences compared to the LSM. The results for the phase angle step response and disturbance rejection are shown in Fig. 5.30, and Fig. 5.31, respectively. The design parameters are $T_{\mathrm{MAF}} = 20$ ms, $k_\varphi = 0.01$ s, $k_v = 16.7\ \mu\mathrm{s}^2$, $k_{\mathrm{i}} = 2500\ \mathrm{rad/s}^2$, and $k_{\mathrm{p}} = 108.4$ rad/s. For the detailed design process, refer to section 5.7.

The derived PLL-SSMs accurately describe the disturbance rejection but show significant differences during severe transients compared to the LSMs. However, these characteristics sensitively depend on the scenarios and the chosen design parameters. The worst-case scenarios were already derived in section 5.1, and thus the next section discusses the PLL design based on the derived models, Symmetrical Optimum (SO), and required immunity to distortions as the first design approach.

5.4 PLL Control Bandwidth Design based on the Required Distortion Attenuation utilizing SSMs

The PLL parameter design crucially affects the PLL performance in the steady-state and during transients. The LSRF-PLL is a standard type 2 control plant that can be described by the generic open-loop transfer function:

$$G_{\mathrm{ol}}(s) = \frac{k\,(s+\omega_{\mathrm{z}})}{s^2\,(s+\omega_{\mathrm{p}})} = \frac{k_{\mathrm{p}}\omega_f\left(s+\frac{k_{\mathrm{i}}}{k_{\mathrm{p}}}\right)}{s^2\,(s+\omega_f)} \quad , \tag{5.29}$$

where k is the open-loop gain, and ω_{z} and ω_{p} are angular frequencies. The symmetric optimum is an approach to design these control structures [138], [139]. The basic idea is to maximize the phase margin PM of the system to achieve a desired stability margin [131], [124]. This approach exploits the symmetry of the open-loop Bode plots regarding the crossover frequency ω_{c} with the corner frequencies ω_{z} and ω_{p}, as shown in Fig. 5.32 and 5.33.
Fig. 5.32 further includes an approximation of the transfer function in 5.29, assuming two corner frequencies ω_{z} and ω_{p} that have both the same distance to ω_{c}. Below or above ω_{z} and ω_{p}, respectively, the magnitude decreases with -40 dB/dec, and in between with -20 dB/dec. The phase plot in Fig. 5.33 illustrates the phase of the open-loop transfer function G_{ol} and indicates symmetry around ω_{c}. Notable is the fact that the phase margin PM reaches its maximum at the crossover frequency ω_{c}. But how can this be achieved?

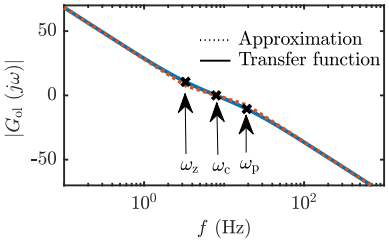


Figure 5.32: Magnitude Bode plot of the open-loop transfer function of the LSRF-PLL presenting the parameters of a generic type 2 control structure.

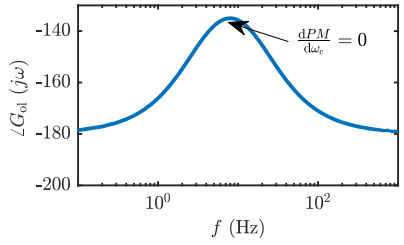


Figure 5.33: Phase angle Bode plot of the open-loop transfer function of the LSRF-PLL presenting the parameters of a generic type 2 control structure.

Golestan already presents in [124] how the symmetric optimum can be applied to LSRF-PLLs. The derivation is repeated here for the sake of completeness. PM depends on the three frequencies ω_z, ω_c, and ω_p. The phase of the transfer function in 5.29 can be calculated and results in PM according to 5.30, which depends on ω_z, ω_c, and ω_p.

$$PM = -\left(-\pi - \angle G_{ol}(j\omega_c)\right) = \pi + \left(-\pi + \underbrace{\tan^{-1}\left(\omega_c/\omega_z\right)}_{\phi_z} - \underbrace{\tan^{-1}\left(\omega_c/\omega_p\right)}_{\phi_p} \right) \tag{5.30}$$

Then, the general definition of the cross-over frequency leads to the first design rule:

$$|G_{ol}(j\omega_c)| = 1 \Rightarrow \qquad \omega_c = k_p \frac{\cos\left(\phi_p\right)}{\sin\left(\phi_z\right)} \Rightarrow \qquad \omega_c = k_p \quad . \tag{5.31}$$

Since the SO basically maximizes PM to guarantee a large stability margin, ω_c can be calculated as follows:

$$\partial PM/\partial\omega_c = 0 \Rightarrow \qquad \omega_c = \sqrt{\omega_z \omega_p} \quad . \tag{5.32}$$

Rearranging the expressions by introducing an arbitrary constant $a^2 = \frac{\omega_p}{\omega_z}$ results in 5.33 and leads to the design rule for k_i and ω_f, so that the LSRF-PLL design parameters are entirely described by choosing ω_c and a according to:

$$a^2 = \frac{\omega_p}{\omega_z} \Rightarrow \qquad PM = \tan^{-1}\frac{a^2-1}{2a} \tag{5.33}$$

$$\Rightarrow \qquad \omega_f = a\omega_c \tag{5.34}$$

$$\Rightarrow \qquad k_i = \frac{k_p \omega_c}{(2\zeta+1)} \quad . \tag{5.35}$$

The detailed derivation of equations 5.30-5.33 is given in Appendix A.3. This description simplifies the open-loop and closed-loop transfer functions and indicates that a corresponds to the damping ratio ζ of the closed-loop poles, as described by:

$$G_{ol}(s) = \frac{a\omega_c^2\left(s + \frac{\omega_c}{a}\right)}{s^2\left(s + a\omega_c\right)} \Rightarrow \qquad G_{cl}(s) = \frac{\theta'}{\theta} = \frac{(2\zeta+1)\omega_c^2\left(s + \frac{\omega_c}{(2\zeta+1)}\right)}{\left(s+\omega_c\right)\left(s^2 + 2\zeta\omega_c s + \omega_c^2\right)} \quad . \tag{5.36}$$

Hence, introducing $a = 2\zeta + 1$ yields the closed-loop transfer function G_{cl} with one real pole at $-\omega_c$ and one pole-pair at $-\omega_c$ with ζ as damping factor. The desired control bandwidth ω_c and damping factor a determine the three design parameters of the LSRF-PLL. For most applications, the optimum trade-off between overshoot and settling time is achieved by $\zeta = 1/\sqrt{2}$, which corresponds to $a = 2.41$ [124]. This leaves the control bandwidth as degree of freedom for PLL design. It should be designed to comply with the necessary immunity to distortions. With the resulting design parameters, the PLL dynamics can be evaluated.

The necessary attenuation of the PLL results from the grid voltage harmonics and the maximum distortions of the estimated phase angle. The maximum control bandwidth ω_c can be calculated to achieve the necessary attenuation atten_{ω_d} of $|G_{ol}|$ at an angular frequency ω_d, according to [140]:

$$\text{atten}_{\omega_d} \approx |G_{ol}\,(j\omega_d)| \approx -20\log\frac{\omega_d}{\omega_c} - 20\log\frac{\omega_d}{\omega_p} = -20\log\frac{\omega_d^2}{\omega_p\omega_c} \quad , \tag{5.37}$$

$$\text{atten}_{\omega_d} = -40\log\left(\frac{\omega_d}{\omega_c\sqrt{a}}\right) \Leftrightarrow \omega_c = \frac{\omega_d}{\sqrt{a}}10^{\left(\frac{\text{atten}_{\omega_d}}{40}\right)} \quad . \tag{5.38}$$

This approach is suitable for a single dominant harmonic in the grid voltage but may fail for complex spectra. The disturbance transfer function G_d given in 5.5 leads to a more accurate description of the distortions of the estimated phase angle. The attenuation for every single voltage harmonic $|G_d\,(n\omega_1)|$ is calculated and multiplied with the amplitude $|\tilde{v}_{\text{PLL,q+}}\,(n\omega_1)|$. The voltage harmonics $\tilde{v}_{\text{PLL,q+}}$ occur at frequencies $2\omega_1$ and $3n\omega_1$ due to the frequency shift of $+\omega_1$ of Park's transformation and the varying sequences of the harmonics according Table 3.3. The resulting amplitudes of the phase angles can be summed up for a worst-case approximation of the harmonic amplitude of $\Delta\delta$. The worst-case estimate neglects the phase shift between different harmonics to yield an accurate upper boundary of the distortions of $\Delta\delta$ as follows:

$$\Delta\delta = |G_d\,(2\omega_1)|\,|\tilde{v}_{\text{PLL,q+}}\,(2\omega_1)| + \sum_{n=1}^{8}|G_d\,(3n\omega_1)|\,|\tilde{v}_{\text{PLL,q+}}\,(3n\omega_1)| \quad . \tag{5.39}$$

The SO is a potent method to reduce the design parameter count of the LSRF-PLL, and guarantees the defined stability margin. It can be applied to sophisticated PLLs, but may not achieve the same accuracy in the control bandwidth, immunity to distortions, and stability margin due to the different transfer characteristics. Therefore, the impact of the SO on the presented PLLs is discussed in the following section.

5.4.1 Is the Symmetrical Optimum Applicable for Prefiltered SRF-PLLs?

Most PLLs with advanced prefilters contain an additional Nf characteristic compared to the LSRF-PLL. Originally, the SO is not applicable for these characteristics since the derived expressions, particularly for the PM in 5.30, are not valid anymore. But how do the Nf characteristic affects the SO design rules in detail?

The SO maximizes the phase margin of the open-loop transfer function of the LSRF-PLL. Typical phase margins for a robust characteristic are in the range of $PM > 30°$ [124]. This requirement guarantees stability since the LSRF-PLL has an infinite gain margin. However, PLLs with prefilter or decomposition algorithms have a finite gain margin due to the 180 degree phase cross-over caused by the notch characteristic. The gain margin mainly

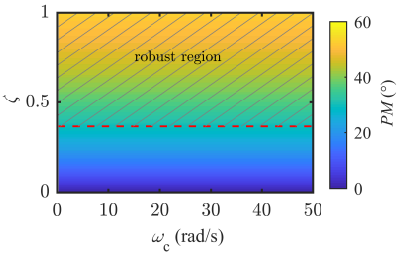


Figure 5.34: Phase margin of LSRF-PLL for different design parameters ζ and ω_c with the hashed robust region of $PM > 30°$.

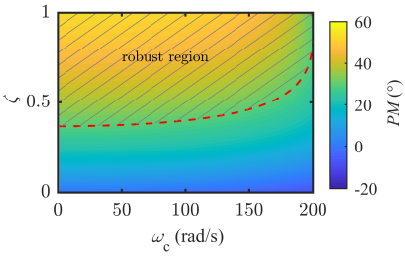


Figure 5.35: Phase margin of DSRF-PLL for different design parameters ζ and ω_c with the hashed robust region of $PM > 30°$.

depends on the open-loop gain, which is critically affected by the voltage amplitude of the fundamental frequency component $\hat{V}_{S,1}$, as shown in Fig. 5.2. Hence, a deviation in $\hat{V}_{S,1}$ will directly change the PLL open-loop gain. The ANS suppresses this effect since it normalizes the PLL input to the instantaneous grid voltage amplitude $\hat{V}_{S,1}$. Consequently, the gain margin is not directly affected by grid voltage steps anymore, and the PM also serves as primary robustness criteria for PLLs with prefilter or sequence decomposition.

The design parameters of the DSRF and DSOGI-PLL are equivalent to the LSRF-PLL. They all contain the low-pass filter and the PI-controller parameters that can be simplified to a damping ratio ζ and the control bandwidth ω_c. However, the impact of the design parameters ζ and ω_c on the phase margin differs significantly. Fig. 5.34 shows the phase margin of the LSRF-PLL for different design parameters and indicates the robust design parameter range with $PM > 30°$. As expected, the phase margin only depends on ζ for the full parameter range. In contrast, the phase margin of the DSRF-SSM (see Fig. 5.35) also depends on ω_c, but the difference between the designed and real PM is neglectable for control bandwidths below $\omega_c < 80$ rad/s. This control bandwidth boundary indicates the range where the SO can be applied without checking the PM separately. The results are also valid for the DSOGI-PLL due to the equivalence to the SSM of the DSRF-PLL.

The Nf and EPMAF-PLL have a much more apparent notch characteristic in their control behavior and do not contain an explicit low-pass filter. Nevertheless, their design can also be simplified to two parameters, i.e., the PI-controller parameters are fixed by choosing the desired damping ratio ζ and control bandwidth ω_c. In contrast to the other PLLs, the filter frequency of Nf and EPMAF is set to the dominant harmonics. For the Nf-PLLs, the PI parameter design is equivalent to the LSRF-PLL. The Nf is tuned to reject the first three dominant harmonics: $2\omega_1$, $3\omega_1$, and $6\omega_1$, and the corresponding damping ratios are equal $\zeta_{Notch} = \zeta_{f,Notch,2\omega_1} = \zeta_{f,Notch,3\omega_1} = \zeta_{f,Notch,6\omega_1}$.

The phase margin of the Nf-PLL presented in Fig. 5.36 critically depends on the damping ratio and control bandwidth. The damping ratio alters the bandwidth of the notch attenuation peak. A higher damping ratio leads to a larger bandwidth of the attenuation peak, which thus affects the control characteristics in a wider frequency range. This effect is verified for small damping ratios of $\zeta < 0.1$, where the PM does not depend on ω_c anymore, as shown in Fig. 5.36. However, low damping ratios with a narrow frequency band of the notch attenuation cause the immunity to distortions to deteriorate during frequency variations, which will be discussed in detail in the next section.
EPMAF-PLLs significantly differ in their transfer characteristic to the other PLLs and thus show different dependencies of the PI design parameters. Equ. 5.40 and 5.41 give the design rules derived in [120] and indicate that k_i and k_p only depend on the natural frequency $\omega_{n,EPMAF}$, and the damping ζ according to:

$$k_i = \omega_{n,EPMAF}^2 \quad , \tag{5.40}$$

$$k_p = 2\zeta_{EPMAF}\omega_{n,EPMAF} + k_\varphi k_i \quad . \tag{5.41}$$

For a more convenient presentation, the natural frequency $\omega_{n,EPMAF}$ will be denoted with $\omega_{c,EPMAF}$, even though it does not represent the cross-over frequency. The EPMAF filter design is already presented in section 5.3.2 and does not offer a degree of freedom.
Fig. 5.37 presents the phase margin analysis for the EPMAF-PLL. Surprisingly, two robust design regions appear since it does not matter if the gain margin is positive or negative. A large damping ratio is desirable in the lower frequency range to achieve a robust design. Contrarily, the damping ratio does not critically affect PM for higher frequencies.

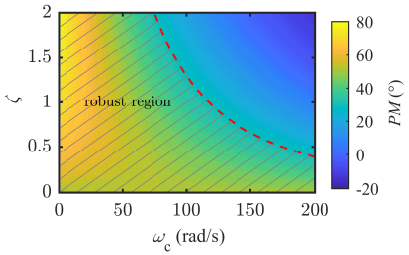


Figure 5.36: Phase margin of Nf-PLL for different design parameters ζ and ω_c with the hashed robust region of $PM > 30°$.

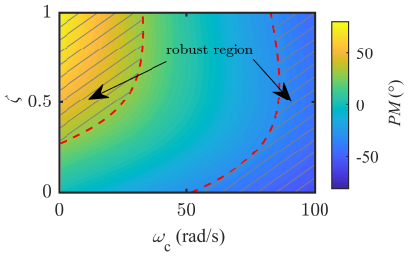


Figure 5.37: Phase margin of EPMAF-PLL for different design parameters ζ and ω_c with the hashed robust region of $PM > 30°$ or $PM < -30°$.

In summary, the SO can be applied to PLLs with prefilters or sequence decomposition and provides a suitable design scheme to reduce the design parameters. It is evident that the prefilter or decomposition alter the phase margin and additionally introduce a gain margin

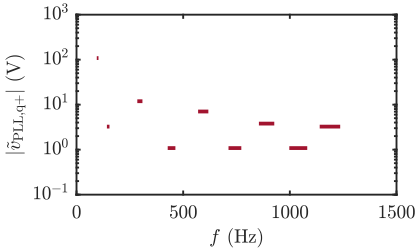


Figure 5.38: Harmonic spectrum of $\tilde{v}_{\mathrm{PLL,q+}}$ considering fundamental frequency variations in the range of 47.5 Hz to 51.5 Hz.

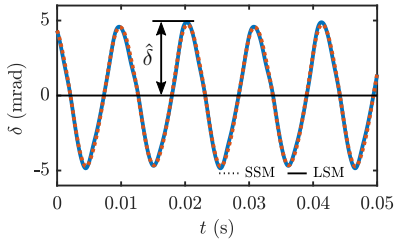


Figure 5.39: Estimated phase angle distortions of the EPMAF-PLL, and the definition of the maximum distortion of the estimated phase angle $\hat{\delta}$ is introduced.

to the control system. The gain margin is not critical due to the ANS, whereas the phase margin must be analyzed thoroughly for any PLL. According to [124], the bandwidth ω_c of PLLs with prefilters have to be one/fifth of the notch frequency. However, this is not valid in general, as shown in the previous analysis. Hence, the PM must be checked for every design parameter set for advanced PLLs to ensure robust control behavior.

5.4.2 SSM-based Design of PLLs utilizing the SO

The presented PM analysis is crucial to guarantee PLL stability that is the mandatory requirement for the design. Moreover, the immunity to distortions is another crucial performance indicator in steady-state and critical concerning grid standards. Once the necessary immunity to distortions reduced the number of feasible design parameters, the evaluation of the step responses must be only applied to the left design parameter space.

The grid voltage harmonics presented in Fig. 5.15 distort the error of the estimated phase angle δ and the converter's power factor λ. These distortions can be predicted with the disturbance transfer function G_d applying the harmonic spectrum $\tilde{v}_{\mathrm{PLL,q+}}$ as input. For the analysis, the harmonic spectrum is first transformed into the dq-frame since the PLL disturbance input is defined by $\tilde{v}_{\mathrm{PLL,q+}}$. Possible deviations in the fundamental frequency also change the frequencies of the harmonics leading to a frequency-shift of the voltage spectrum. The superimposed spectra of $\tilde{v}_{\mathrm{PLL,q+}}$ for all fundamental frequencies is shown in Fig. 5.38 and serve as input for the disturbance transfer functions of the PLLs to determine the immunity to voltage distortions.

The maximum deviation in the error of the phase angle is described by $\hat{\delta}$, see Fig. 5.39. The distortion magnitude $\hat{\delta}$ is a superposition of the voltage harmonics attenuated by G_d. Fig. 5.40 and Fig. 5.41 show the disturbance spectrum at the LSRF and DSRF-PLL output denoted with $\hat{\delta}_n$ resulting from $|G_d||\tilde{v}_{\mathrm{PLL,q+}}|$ for all fundamental frequencies. The spectrum $\hat{\delta}_n$ is a superposition of the spectra of $\hat{\delta}$ for each fundamental frequency, and the spectrum

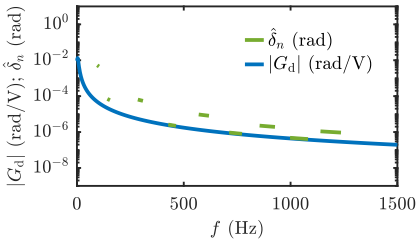


Figure 5.40: Disturbance transfer function G_d and output distortions $\hat{\delta}_n$ of the LSRF-PLL considering fundamental frequency variations.

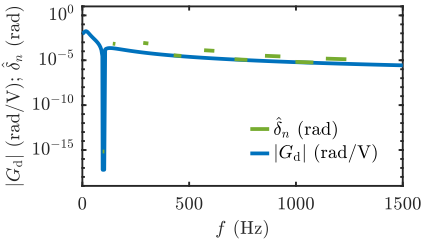


Figure 5.41: Disturbance transfer function G_d for $f_1 = 50$ Hz and output distortions $\hat{\delta}_n$ of the DSRF-PLL considering fundamental frequency variations.

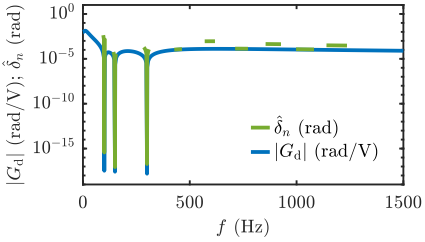


Figure 5.42: Disturbance transfer function G_d and output distortions $\hat{\delta}_n$ of the Nf-PLL considering fundamental frequency variations.

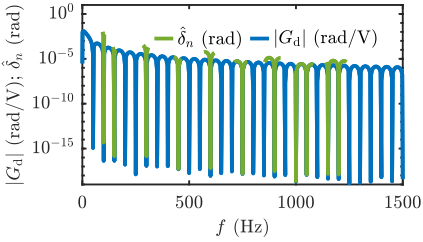


Figure 5.43: Disturbance transfer function G_d and output distortions $\hat{\delta}_n$ of the EPMAF-PLL considering fundamental frequency variations.

for one fundamental frequency can be extracted by choosing the respective ω_1 and taking all components of $\hat{\delta}_n$ with $n\omega_1$. Note that G_d for the DSRF-PLL must be calculated separately for each fundamental frequency since the algorithm is frequency adaptive, and the transfer function changes with the fundamental frequency.

The superimposed spectrum $\hat{\delta}_n$ for the Nf-PLL and EPMAF-PLL are presented in Fig. 5.42 and 5.43, respectively. The results for $\hat{\delta}_n$ indicate that the varying fundamental frequency critically affects the immunity to distortions, particularly at higher frequencies. Higher-order harmonics experience a larger frequency shift than low-order harmonics due to the relation $n\omega_1 = n\omega_{1,\mathrm{n}} \pm n\Delta\omega_1$. These results demonstrate that the notch bandwidth is crucial for the disturbance rejection since frequency deviations may lead to loss of its attenuation, as shown in Fig. 5.42 for the Nf and Fig. 5.43 for the EPMAF.

Due to the frequency variations, it is complicated to evaluate the maximum estimated phase angle distortion $\hat{\delta}$ based on these spectra. However, an estimate of the worst-case for $\hat{\delta}$ can

be achieved by summing up all harmonic amplitudes for one fundamental frequency value ω_1 according to:

$$\hat{\delta}_m = \left| G_\mathrm{d}\left(2\omega_{1,m}\right) \left\| \tilde{v}_\mathrm{PLL,q+}\left(2\omega_{1,m}\right) \right| + \sum_{n=1}^{8} \left| G_\mathrm{d}\left(3n\omega_{1,m}\right) \right\| \tilde{v}_\mathrm{PLL,q+}\left(3n\omega_{1,m}\right) \right| \quad . \tag{5.42}$$

Then, the range of ω_1 can be sampled with a sufficiently low step $\Delta\omega_1$ to capture a subset of all possible ω_1. The interval 47.5 Hz $< \omega_1/(2\pi) <$ 51.5 Hz is sampled with M equidistant steps m with $\Delta\omega_1$, which leads to $\hat{\boldsymbol{\delta}}$:

$$\hat{\boldsymbol{\delta}} = \begin{bmatrix} \hat{\delta}_1 & \dots & \hat{\delta}_m & \dots & \hat{\delta}_M \end{bmatrix} \quad . \tag{5.43}$$

Finally, the maximum expectable distortion magnitude $\hat{\delta}_\mathrm{wc}$ for one design parameter combination ω_c and ζ can be derived as follows:

$$\hat{\delta}_\mathrm{wc} = \max \hat{\boldsymbol{\delta}}\left(\omega_\mathrm{c}, \zeta\right) \quad . \tag{5.44}$$

This estimate neglects the phase of the harmonics, which is difficult to approximate for every single operating condition. However, the chosen assumptions always guarantee the condition $\hat{\delta} \leq \hat{\delta}_\mathrm{wc}$.

The design parameter space is finally reduced, respecting the stability and immunity to distortions. Now, the settling time can be extracted to achieve optimum design parameters. In the range of $\zeta = 0 - 1$, the difference between the settling times of frequency response and phase angle response is neglectable (Fig. 13 in [124]). Hence, the settling time of the estimated phase angle error for a phase angle jump serves as an indicator for the dynamic performance. The settling time is defined as the time interval from fault initiation until the error of the estimated phase angle enters a defined tolerance band and stays within its boundaries. The tolerance band is chosen to 5 mrad according to the maximum distortions of the power factor presented in section 5.1. This definition is presented in Fig. 5.44. Note that the tolerance band is larger in the figure for visualization purpose.
The type A fault is the most critical disturbance for PLLs, considering the phase angle jump and voltage magnitude steps. This fault can be simplified to $-\pi/2$ phase angle jump since the voltage amplitude step does not affect the SSM step response. The optimum design can then be extracted by finding the minimum settling time $\min t_{\mathrm{set},\delta}$ respecting mandatory immunity to distortions $\hat{\delta}_\mathrm{wc} < 5$ mrad. The overall optimization is defined as follows:

$$\min_{\omega_\mathrm{c},\zeta} \quad t_{\mathrm{set},\delta}\left(\omega_\mathrm{c}, \zeta\right) \qquad \text{s.t.} \qquad \hat{\delta}_\mathrm{wc} < \delta_\mathrm{max} \quad . \tag{5.45}$$

The overall design process can be summarized as presented in Fig. 5.45. First, the design parameter space ω_c, ζ is chosen and sampled with a predefined resolution that leads to a design parameter matrix with y x z entries containing all sampled combinations of ω_c and ζ.

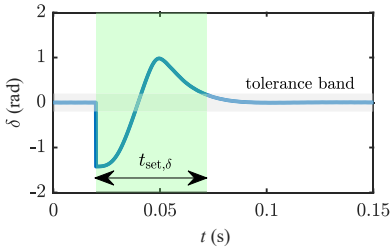


Figure 5.44: Definition of the settling time $t_{\text{set},\delta}$ for the step response of the phase angle error by using a tolerance band to define the steady-state.

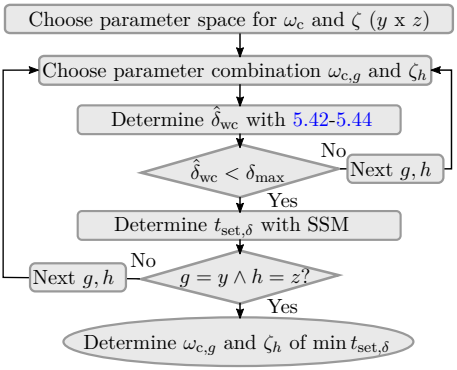


Figure 5.45: Design process for PLLs considering the necessary immunity to distortions $\hat{\delta}_{wc} < \delta_{max}$ and optimizing the settling time $t_{\text{set},\delta}$.

For every design parameter set $\omega_{c,g}$ and ζ_h, the maximum estimated phase angle distortion $\hat{\delta}_{wc}$ is calculated with G_d during a type E fault with $|\underline{Z}_F|$=0 pu, $|\underline{Z}_S|$=1 pu, r_F=0 pu, and r_S=1 pu. Then, the algorithm checks if $\hat{\delta}_{wc} < \delta_{max}$ is achieved for these design parameters. If not, the next parameter set is calculated since this parameter combination does not comply with the necessary constraint. If the requirement is fulfilled, the settling time of the estimated phase angle $t_{\text{set},\delta}$ is calculated based on the control transfer function G_{cl}. A type A fault serves as a worst-case scenario assuming the grid parameters $|\underline{Z}_F|$=0.05 pu, $|\underline{Z}_S|$=1 pu, r_F=0 pu, and r_S=1 pu and $f_1 = 50$ Hz. Since the magnitude step does not affect the SSM, the scenario is replaced by an -90 degree phase jump. These steps are repeated for all sampled parameter combinations. Finally, the parameter set $\omega_{c,g}$ and ζ_h with the minimum settling time min $t_{\text{set},\delta}$ is the outcome of this optimization. The final parameters ensure the necessary immunity to distortions while achieving the fastest settling for the designed PLL.

The settling times for the analyzed design parameter space [$\boldsymbol{\omega}_c$ $\boldsymbol{\zeta}$] are shown in the following figures. The parameters of the hashed surface $\hat{\delta}_{wc} > 5$ mrad violate the immunity to distortions

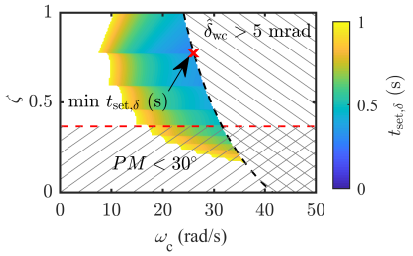


Figure 5.46: Settling time of the phase angle error $t_{\mathrm{set},\delta}$ of the LSRF-PLL for different design parameter sets ω_c and ζ, and identification of the set for minimum settling time considering the maximum distortion criteria and indicating the robustness.

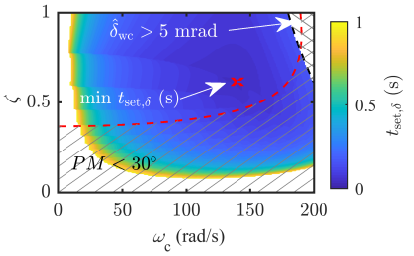


Figure 5.47: Settling time of the phase angle error $t_{\mathrm{set},\delta}$ of the DSRF-PLL for different design parameter sets ω_c and ζ, and identification of the set for minimum settling time considering the maximum distortion criteria and indicating the robustness.

criterion, whereas the robustness region $PM < 30° \ \wedge \ PM > -30°$ is only a performance indicator for the design. The LSRF-PLL only achieves low ω_c due to the low disturbance rejection capability of the low-pass filter, as shown in Fig. 5.46. The damping ratio directly adjusts the control robustness and does not depend on ω_c. Surprisingly, the conventional damping ratio of $1/\sqrt{2}$ does not achieve the minimum settling time, but should be increased to 0.78. Note that the PT2 behavior in combination with an absolute settling tolerance leads to steps in the settling times from one design parameter set to the other.

The DSRF-PLL enables much larger control bandwidth ω_c due to the enhanced filter capability of the sequence decomposition. This characteristic is highlighted in the settling time results in Fig. 5.47, where the mandatory immunity to distortions does not critically limit the allowed design parameter space. For the DSRF-PLL, the maximum ω_c is predominantly limited by the stability. However, the minimum settling time is achieved for $[\omega_\mathrm{c} \ \zeta]$ with enough distance to both boundaries, i.e., to the disturbance rejection and robustness limits. Since these results rely on the SSM, they are also valid for the DSOGI-PLL.

Even though the Nf has a high distortion attenuation, the Nf-PLL bandwidth is strictly limited by the immunity to distortions, as presented in Fig. 5.48. This significant difference to the DSRF results from the missing frequency adaptivity of the Nf. The robustness region is not of interest since the required immunity to distortions already covers it. The settling times of the EPMAF-PLL are presented in Fig. 5.49 and demonstrate that the maximum control bandwidth is also strictly limited by the immunity to distortions. Moreover, the resulting design parameter set for the minimum settling time has a $PM \leq 30$, indicating a small stability margin.

The proposed design, which considers the optimization of ζ by finding ζ_opt and $\omega_\mathrm{c,opt}$, is compared to the conventional approach with $\zeta_{0.7} = 0.7$ and $\omega_{\mathrm{c},0.7}$. Table 5.2 summarizes the results of the PLL designs. The control bandwidths do not show significant differences except for the Nf-PLL, whereas the damping ratios significantly differ from $\zeta_{0.7}$. Three of four PLLs

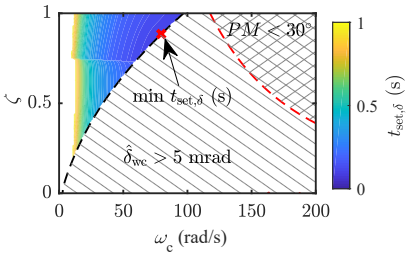


Figure 5.48: Settling time of the phase angle error $t_{\text{set},\delta}$ of the Nf-PLL for different design parameter sets ω_c and ζ, and identification of the set for minimum settling time considering the maximum distortion criteria and indicating the robustness.

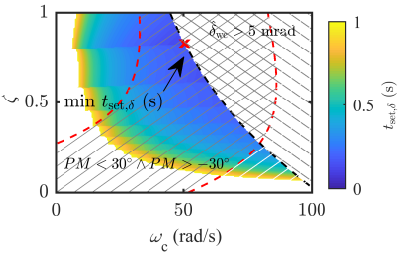


Figure 5.49: Settling time of the phase angle error $t_{\text{set},\delta}$ of the EPMAF-PLL for different design parameter sets ω_c, and ζ and identification of the set for minimum settling time considering the maximum distortion criteria and indicating the robustness.

Table 5.2: Design parameter results for the presented optimization process considering the phase angle settling time and the immunity to distortions.

PLLs	$\omega_{c,\text{opt}}$ (rad/s)	ζ_{opt}	$\omega_{c,0.7}$ (rad/s)	$\zeta_{0.7}$
LSRF	25.13	0.78	25.13	0.7
DSRF/DSOGI	138.23	0.62	138.23	0.7
Nf	78.54	0.88	50.27	0.7
EPMAF	50.27	0.83	53.41	0.7

achieve a larger ζ indicating better damping compared to the conventional design. However, the design parameters do not explicitly indicate the steady-state and dynamic PLL performance. Therefore, $\hat{\delta}_{\text{wc}}$, $t_{\text{set},\delta}$, and PM are shown for the proposed and conventional design as indicators for the immunity to distortions, dynamic performance, and robustness. The settling time decreases significantly for each analyzed PLL, and the most significant decrease of 50% is achieved for the Nf-PLL. The maximum output distortion slightly increases for the optimum design but never exceeds the limit of 5 mrad. Moreover, in three of four cases, the PM is increased. Only for the Nf the PM decreases but does not enter a critical region. These results highlight the effectiveness of the proposed design procedure and show that the damping ratio $\zeta_{0.7} = 0.7$ is not the optimum case for the minimum settling time considering an absolute tolerance band of 5 mrad.

The presented design process relies on the model fidelity of the SSMs. Moreover, the settling time is only determined for a single worst-case scenario. Two validation steps are presented in the next section to confirm the models and worst-case design results. First, the SSM results are compared to the LSM results for type E and type A faults with various sag depths to capture more operating points and proof model fidelity. Second, an experiment is designed to validate the SSMs and LSMs under realistic operating conditions. The experiment also consists of various fault scenarios, not only focusing on the worst-case.

Table 5.3: Performance parameters for the conventional and optimized design considering $\hat{\delta}_{\text{wc}}$, $t_{\text{set},\delta}$, and PM.

PLLs	design	$\hat{\delta}_{\text{wc}}$ (rad)	$t_{\text{set},\delta}$ (s)	PM (°)
LSRF	$\zeta_{0.7}$	0.0044	0.38	45
	ζ_{opt}	0.0046 ↑	0.29 ↓	47 ↑
DSRF/DSOGI	$\zeta_{0.7}$	0.0029	0.06	40
	ζ_{opt}	0.0027 ↓	0.04 ↓	37 ↓
Nf	$\zeta_{0.7}$	0.0045	0.22	55
	ζ_{opt}	0.005 ↑	0.11 ↓	44 ↓
EPMAF	$\zeta_{0.7}$	0.0048	0.17	4
	ζ_{opt}	0.005 ↑	0.13 ↓	7 ↑

5.5 PLL Model Validation with RCP-System and SiC Converter Prototype

A realistic test environment for PLLs consists of an adjustable three-phase voltage source, voltage measurements, and the controller hardware that processes the PLL-algorithms. The voltage source must meet three essential requirements: First, it must be adjustable in a wide range to enable fault voltage emulation with arbitrary voltage magnitudes and angles in the three phases in the range of 0-1.2$\hat{V}_{\text{S},1}$. Second, the voltage source bandwidth must be high enough to enable accurate emulation of harmonics and fast magnitude steps and angle jumps. As a third point, the instantaneous phase angle θ, and the positive and negative sequence voltage magnitudes must be known to compare them to the PLL output. All these requirements are met by the realized SiC-converter prototype that provides the adjustable grid voltage $\mathbf{v}_C$ at its filter capacitor output.
Three LEM LV-25P voltage sensors measure $\mathbf{v}_C$, and transform them into analog signals that are captured by the ADCs of the RCP-system. The algorithms in the RCP-system are processed in the FPGA and the CPU. In the following tests, the CPU calculates the voltage reference $\mathbf{v}^*_{\text{abc}}$ and executes the PLL algorithms. The FPGA generates the switching signals for the converter applying SPWM and transmits the measured voltages $\mathbf{v}_C$ to the CPU. Finally, the PLL output signals are compared to the reference values to calculate the error of the estimated phase angle δ. The overall setup is presented in Fig. 5.50, and the parameters are summarized in Table 5.4.

The voltage waveform comparison of the reference voltages $\mathbf{v}^*_{\text{abc}}$ generated by the RCP-system and the instantaneous output voltages of the converter $\mathbf{v}_C$ show just minor differences, as shown in Fig. 5.51. However, two problems are identified in the measured error of the estimated phase angle δ. The first problem is that the measured phase angle error contains a dc-offset due to the phase shift between the voltages $\mathbf{v}^*_{\text{abc}}$ and $\mathbf{v}_C$ caused by the LC-filter. The offset is almost identical for all PLLs and does not depend on the operational scenario. The

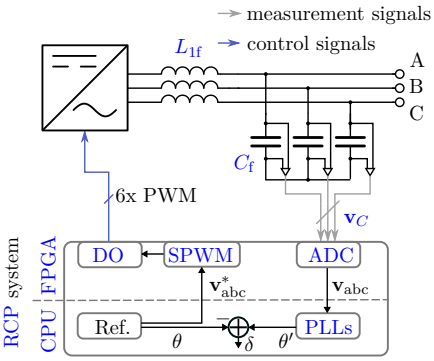


Figure 5.50: Test bench consisting of an RCP-system and SiC-converter prototype to validate PLL models with emulated grid voltages considering the ADCs, measurements, and control unit execution time.

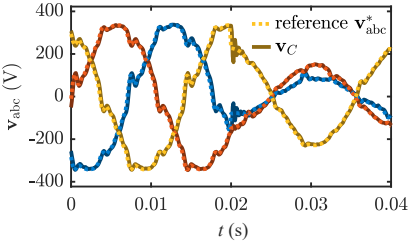


Figure 5.51: Comparison of reference voltages v^*_{abc} given to the SPWM and output voltage of the converter v_C during a type E fault (without zero-sequence voltage) with $|Z_F|$=0.1 pu, r_F=0 pu, and r_S=10 pu, and voltage harmonics according to EN 50160 [38].

Table 5.4: Parameters of the test bench for PLL model validation.

Parameter	Value	Part	Value
V_{dc}	720 V	L_{1f}	0.5 mH
f_{sw}	80 kHz	C_f	6.8 μF
T_{CPU}	100 µs		
T_{FPGA}	10 ns		

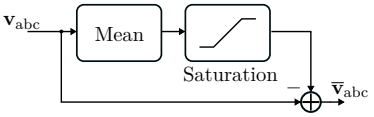


Figure 5.52: Filter for dc-components in the measured grid voltages consisting of a moving average filter and a saturation to limit the impact on the PLL dynamics.

offset is shown in the raw data of the DSRF-PLL steady-state in Fig. 5.54 and is compensated in the following analysis. The second problem is based on a dc-offset in the measured grid voltages and is more complicated to solve.

The measured estimated phase angle error demonstrates that PLLs in the SRF are vulnerable to dc-offsets in the input voltages. These dc-components lead to 50 Hz oscillations in the dq-components that are difficult to filter due to their low frequency. Several approaches are proposed in the literature to overcome this problem [134], [141], [142]. Here, a simple structure containing a low-pass filter with a saturated output is used, see Fig. 5.52. The mean operator is tuned to 50 Hz and the lower and upper limit of the saturation to -0.5 V and 3 V, respectively. The saturation prevents that the compensation deteriorates the PLL dynamics. The tuning was the same for every PLL and not changed during all analyzed scenarios, which shows the low sensitivity of the dc-offset on the operating point.

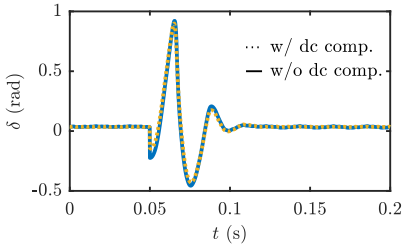


Figure 5.53: Step response results for the DSRF-PLL with and without mean compensation during a type E fault with $|Z_{\mathrm{F,typeE}}| = 0.01$. The minor impact of the dc-component rejection on the dynamics is visible.

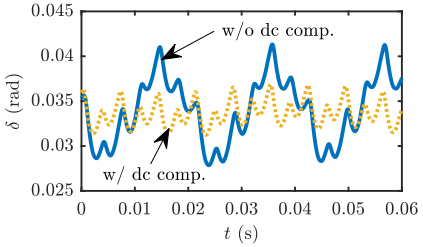


Figure 5.54: 50 Hz oscillation in the error of the estimated phase angle during a type E fault with $|Z_{\mathrm{F,typeE}}| = 0.01$ due to dc-components in the measured grid voltages that mainly result from sensor offsets, and their successful rejection by the proposed mean filter. The constant error of 30 mrad results from the phase-shift caused by the *LC*-filter.

For validation, the dc-filter is tested for the DSRF-PLL. The 50 Hz component is successfully rejected and the dynamics are not significantly affected, as shown in Fig. 5.53 and Fig. 5.54. From the author's point of view, it is not helpful to derive a general design rule, since the dc-component critically depends on the system under investigation, and the dc-filter should be directly designed for the individual hardware setup.

The presented setup enables validation of the PLL-models under realistic operating conditions. The following sections show the results for the PLL performance indicators, i.e., settling time and distortion of the estimated phase angle, in comparison to the offline-simulation results for different grid scenarios.

5.5.1 Steady-State Distortion Rejection during Type E Faults

The PLL's immunity to distortions is tested during type E faults with different positive sequence voltages or $|Z_{\mathrm{F,typeE}}|$, respectively. The fundamental frequency operating point is 47.5 Hz representing the worst-case for most of the PLLs. The maximum distortion $\hat{\delta}$ is measured according to Fig. 5.39. Since the distortions are limited to small values below 5 mrad, the SSM, LSM, and Experiment (EXP) should achieve similar results.

Fig. 5.55 and 5.56 confirm these expectations and show only minor differences. However, the relative error is comparably large for some PLLs and fault cases, e.g., the DSRF has the most significant error with approximately 50%. Nevertheless, absolute tolerance is below 1 mrad, which is a very accurate result for phase angle measurements. These results verify the accuracy of the SSMs regarding the phase angle distortions over a wide range of operating points. The results further show that $\hat{\delta}$ increases with decreasing $|Z_{\mathrm{F,typeE}}|$ since the negative sequence voltage increases, which leads to larger distortions. Only the DSRF shows an almost

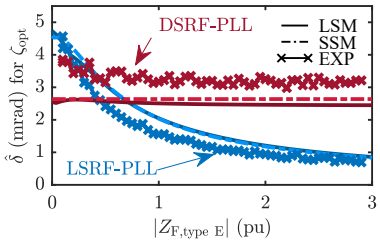


Figure 5.55: Comparison of SSM, LSM, and experimental results (EXP) for the maximum distortion magnitude $\hat{\delta}$ of the LSRF-PLL and DSRF-PLL during a type E fault with different sag depths or $|Z_{F,typeE}|$, respectively.

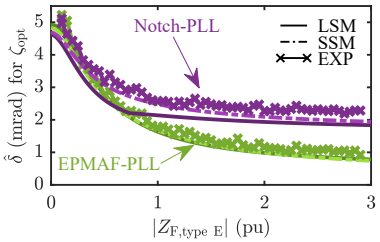


Figure 5.56: Comparison of SSM, LSM, and experimental results (EXP) for the maximum distortion magnitude $\hat{\delta}$ of the Nf-PLL and DSOGI-PLL during a type E fault with different sag depths or $|Z_{F,typeE}|$, respectively.

constant $\hat{\delta}$ due to the frequency adaptive filter capability, and thus full attenuation of the negative sequence even for shifts in the fundamental frequency.

5.5.2 Dynamic Response on Type A Faults

The dynamic characteristics of the PLL models are validated during a type A fault with different fault impedance magnitudes $|Z_{F,typeA}|$ and a constant fault impedance ratio r_F=0 pu. These parameters, in combination with a source impedance ratio of r_S=10 pu, lead to large phase angle jumps. $|Z_{F,typeA}|$ is varied between 0.1 and 3 that yields a positive sequence magnitude range of 0.1 pu $< \hat{V}_{S,1} <$ 0.88 pu normalized to the rated voltage of 230 V.

Fig. 5.57 shows the comparison of the experiment and LSM results for the PLL design parameters with optimized bandwidth ω_c and fixed damping ratio $\zeta_{0.7}$. The results indicate sufficient model accuracy for most operational scenarios. However, the settling times of the simulation and experiment differ significantly in the range of 20% for some operating points caused by the PT2 behavior of the step responses. Only minor differences in the oscillation magnitudes between the simulation and experiment may lead to large deviations in the settling time. For example, the oscillation magnitude of the simulation results is slightly below the limit of the tolerance band, whereas the oscillation magnitude determined by the experiment is slightly larger than the tolerance band. In this case, the settling time determined in the experiment will be shifted by at least 1/2 of the oscillation period in comparison to the simulation results until it may stay within the tolerance band. These characteristics lead to the steps in the settling time results that are shifted with $|Z_{F,typeA}|$ in the LSM compared to the experiment.
The settling time results for the optimized design are shown in Fig. 5.58 and show less differences between experiment and LSM than the conventional design. Here, the maximum deviation is approximately 3% (except for the DSRF) that highlights the high fidelity of

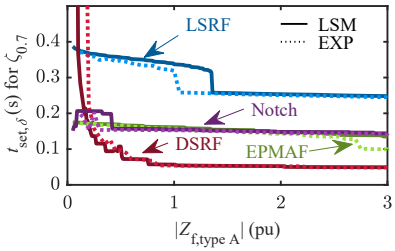


Figure 5.57: Comparison of the LSM and experiment results (EXP) for the settling time $t_{\mathrm{set},\delta}$ of the estimated phase angle of the PLLs during type A faults with different sag depths considering the PLL bandwidth optimization with fixed $\zeta = 0.7$.

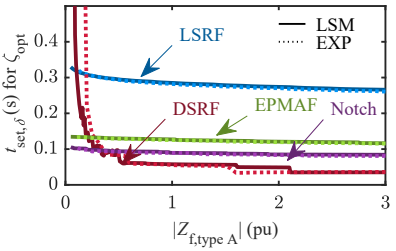


Figure 5.58: Comparison of the LSM and experiment results (EXP) for the settling time $t_{\mathrm{set},\delta}$ of the estimated phase angle of the PLLs during type A faults with different sag depths considering the PLL bandwidth and damping factor optimization.

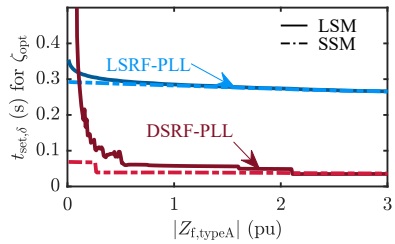


Figure 5.59: Comparison of the SSM and LSM results for the estimated phase angle settling time $t_{\mathrm{set},\delta}$ of the LSRF-PLL and DSRF-PLL during type A faults with different sag depths.

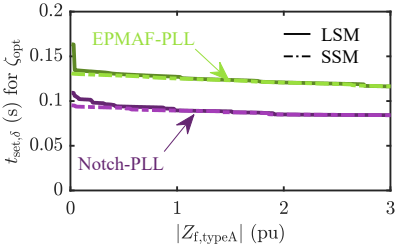


Figure 5.60: Comparison of the SSM and LSM results for the estimated phase angle settling time $t_{\mathrm{set},\delta}$ of the Nf-PLL and EPMAF-PLL during type A faults with different sag depths.

the LSMs. As already observed in the conventional design, the DSRF is unstable for small $|Z_{\mathrm{F,typeA}}|$ ($t_{\mathrm{set},\delta} \to \infty$), which is accurately predicted by the LSM.

The SSMs yield accurate results for most PLLs even for severe fault scenarios with small $|Z_{\mathrm{F,typeA}}|$, as shown in Fig. 5.59 and Fig. 5.60. The relative error is smaller than 20% except for the DSRF-PLL, which is a sufficient accuracy considering that the fault scenarios contain large magnitude and phase angle jumps that are typically out of range of SSMs. However, the LSM and experiment reveal an instability mechanism of the DSRF-PLL that the SSM cannot capture. Therefore, the assumptions for deriving the SSM are reviewed in section 5.7 and lead to the proposed multi-fidelity model-based design.

Based on the validated models, both design optimizations can be compared. Fig. 5.61 and 5.62 show a shorter settling time for ζ_{opt} for most of the PLLs and operating scenarios. The LSRF-PLL yields a smaller settling time, particularly for larger sag depths and smaller $\hat{V}_{\mathrm{S},1}$, respectively. In contrast, the DSRF settling times do not differ significantly between both designs. The most significant improvement in the settling times is achieved for the PLLs

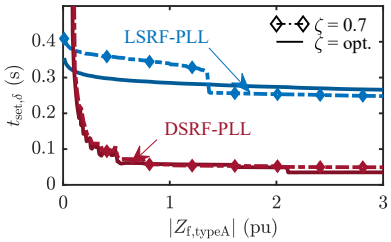


Figure 5.61: LSM results of the settling time of the estimated phase angle $t_{\mathrm{set},\delta}$ of the LSRF-PLL and DSRF-PLL for the two design approaches ζ_{opt} and $\zeta_{0.7}$ during type A faults with different sag depths.

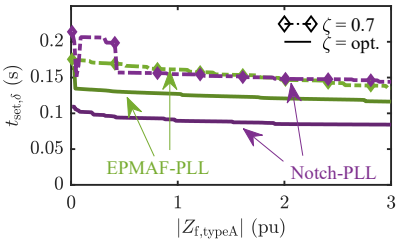


Figure 5.62: LSM results of the settling time of the estimated phase angle $t_{\mathrm{set},\delta}$ of the Nf-PLL and EPMAF-PLL for the two design approaches ζ_{opt} and $\zeta_{0.7}$ during type A faults with different sag depths.

with prefilter, as demonstrated in Fig. 5.62. The settling time of the Nf-PLL can be reduced by 50%-100% and the settling time of the EPMAF by 20%.
These results confirm the effectiveness of the damping factor optimization, particularly, for PLLs with prefilter. Moreover, the individually optimized designs enable a fair comparative study between the PLLs since they all must meet the same disturbance rejection constraint under the same worst-case scenarios. The comparison confirms that the settling times of the PLLs can be significantly decreased with higher filter efforts. The Nf and EPMAF-PLL lead to much shorter settling times than the LSRF-PLL. These results can only be improved by a filter that is frequency adaptive such as the DSRF-PLL. Unfortunately, this structure shows other instability mechanisms that cannot be captured by its SSM, so that design efforts are significantly increased.

The validated models accurately predict the error of the estimated phase angle during different grid scenarios. However, the phase angle error is only an auxiliary quantity and not of direct interest for the converter performance since the grid codes provide requirements for the converter's power factor accuracy and output current settling time. Therefore, the models must be extended to describe the impact of the PLL on the power factor and output current of the converter. These model extensions are presented in the next section.

5.6 Impact of the PLL on the Voltage Oriented Control Considering Power Factor and Converter Current

The PLLs affect the converter's power factor and output current, which is critical due to grid code requirements. Conventional PLL designs do not consider these relations and rely on the

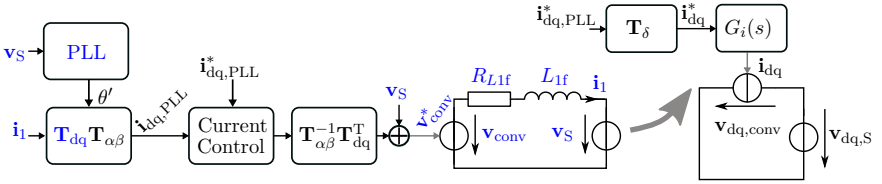


Figure 5.63: Norton's equivalent circuit of VOC with PLL considering an averaged converter model with filter inductance.

evaluation of the estimated phase angle error δ [124], [140]. However, this is typically only an auxiliary quantity for the converter control. Therefore, this section presents the influence of δ on the converter's power factor λ and output current $\mathbf{i}_{dq}$, and analyses the impact on the PLL design.

Fig. 5.63 shows the VOC structure including the PLL and the averaged converter model with the converter-side filter inductance L_{1f}. This structure can be simplified to a Norton equivalent circuit in dq-frame that accurately describes the system dynamics. The Norton equivalent circuit relies on the assumption that the current control closed-loop transfer function can be approximated by a First Order Lag Element (PT1) transfer function G_i with the time constant τ_i according to 5.46. This assumption holds for the current control design based on pole-zero cancellation.

$$G_i(s) = \frac{1}{1 + s\tau_i} \tag{5.46}$$

The VOC structure in Fig. 5.63 consists of two dq-frames. One corresponds to the real phase angle θ, and leads to the converter currents $\mathbf{i}_{dq}$. The other dq-frame locks on the estimated phase angle θ' of the PLL, which results in the converter currents $\mathbf{i}_{dq,PLL}$. Both currents should be identical in steady-state $\delta = 0$. However, these currents differ significantly during grid voltage transients leading to differing active and reactive power injection compared to the references.

Eq. 5.47 gives the relation between $\mathbf{i}_{dq}$ and $\mathbf{i}^*_{dq,PLL}$, which contains the matrix $\mathbf{T}_\delta$ to transform the currents from the PLL dq-frame into the grid dq-frame. This relation reveals that both components of $\mathbf{i}^*_{dq,PLL}$ affect reactive and active grid currents during phase angle transients ($\delta \neq 0$). These coupling mechanisms are nonlinear due to the multiplication of $\mathbf{T}_\delta(\delta)$ with the reference currents, even if the trigonometric terms of $\mathbf{T}_\delta$ are linearized.

$$\mathbf{i}_{dq} = \begin{bmatrix} i_d & i_q \end{bmatrix}^T = \underbrace{\begin{bmatrix} \cos(\delta) & \sin(\delta) \\ -\sin(\delta) & \cos(\delta) \end{bmatrix}}_{\mathbf{T}_\delta} \mathbf{i}_{dq,PLL} = \mathbf{T}_\delta G_i(s) \mathbf{i}^*_{dq,PLL} \tag{5.47}$$

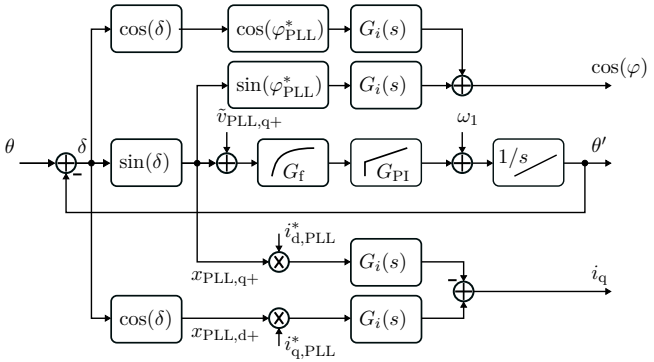


Figure 5.64: Extended PLL-LSM with current control and power factor.

The power factor is based on similar relations like the grid currents and can be described as follows:

$$[\cos(\varphi) \quad \sin(\varphi)]^{\mathrm{T}} = \frac{\mathbf{i}_{\mathrm{dq}}}{\sqrt{i_{\mathrm{d}}^2+i_{\mathrm{q}}^2}} = \mathbf{T}_{\delta} G_i(s) \frac{\mathbf{i}^*_{\mathrm{dq,PLL}}}{\sqrt{i^{*2}_{\mathrm{d,PLL}}+i^{*2}_{\mathrm{q,PLL}}}} = \mathbf{T}_{\delta} G_i(s) \left[\cos\left(\varphi^*_{\mathrm{PLL}}\right) \ \sin\left(\varphi^*_{\mathrm{PLL}}\right)\right]^{\mathrm{T}} . \tag{5.48}$$

Typically the active and apparent power define the power factor, but the d and q-current component in the grid frame directly represent the active and reactive current, respectively. Hence, the power factor can be calculated with $\mathbf{i}_{\mathrm{dq}}$ according to 5.48, which shows that both components of $\mathbf{i}^*_{\mathrm{dq,PLL}}$ affect the $\cos(\varphi)$ during phase angle transients. Moreover, the current references $\mathbf{i}^*_{\mathrm{dq,PLL}}$ can be substituted with the power factor references $[\cos\left(\varphi^*_{\mathrm{PLL}}\right) \ \sin\left(\varphi^*_{\mathrm{PLL}}\right)]^{\mathrm{T}}$ to obtain an identical transfer characteristic like the currents (see 5.47).
The equivalent circuit in Fig. 5.63 is combined with the PLL-LSM according to 5.47 and 5.48, and leads to the block diagram in Fig. 5.64. This model describes the large-signal behavior of the VOC, considering the dynamics of the grid synchronization. Only the ANS is neglected, i.e., the grid voltage magnitude $\hat{V}_{\mathrm{S,1}}$ is accurately tracked and normalizes the PLL input.

The model is verified with time-domain simulations based on the averaged converter model considering the PLL, VOC, and physical circuit components, as shown in Fig. 5.63. A type A fault with $\hat{V}_{S,1} = 0.68$ pu and a 90° phase angle jump is applied to the converter terminals at $t = 0.1$ s. The LSRF-PLL parameters are $\omega_{\mathrm{f}} = 120$ rad/s, $k_{\mathrm{i}} = 1035$ rad/s^2, and $k_{\mathrm{p}} = 50$ rad/s. A time constant τ_i =1 ms is assumed for the current control [117]. The grid currents in the PLL-frame ($\mathbf{i}_{\mathrm{dq,PLL}}$) in Fig. 5.65 do not show any response to the type A fault, since they do not depend on δ. In contrast, the grid currents $\mathbf{i}_{\mathrm{dq}}$ in Fig. 5.66 show a disturbance response due to the phase angle jump. These characteristics confirm the model equation given in 5.47, which achieves the same results like the numerical model as presented

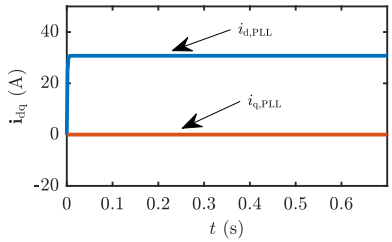


Figure 5.65: Converter currents in dq-components transformed with the PLL phase angle θ' during a symmetrical fault (type A) with a 90° phase jump.

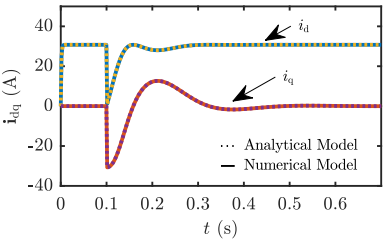


Figure 5.66: Converter current in dq-components transformed with the grid phase angle θ during a symmetrical fault (type A) with a 90° phase jump simulated with the numerical and analytical model.

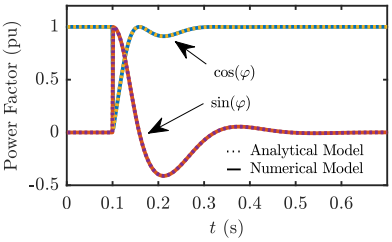


Figure 5.67: Power factors during a symmetrical fault (type A) with a 90° phase jump simulated with the numerical and analytical model.

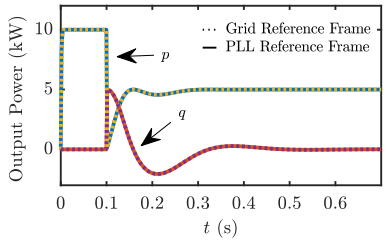


Figure 5.68: Converter output power in different angle reference frames during a symmetrical fault (type A) with a 90° phase jump.

in Fig. 5.66. The power factor shows similar transients like the currents $\mathbf{i}_{dq}$ as depicted in Fig. 5.67, which confirms the relation given in 5.48.

The test scenario shows differing transient processes for the currents $\mathbf{i}_{dq}$ and $\mathbf{i}_{dq,PLL}$ in response to the fault. However, the active and reactive power, i.e., p and q, are identical in both reference frames as shown in Fig. 5.68. This behavior indicates that the voltages in the PLL-frame $\mathbf{v}_{dq,PLL,S}$ change in response to the phase angle jump, whereas the currents $\mathbf{i}_{dq,PLL}$ are constant (compare Fig. 5.65). In contrast, the currents in the grid-frame show a disturbance response, whereas the voltages $\mathbf{v}_{dq,S}$ are constant (compare Fig. 5.66). Regardless of these differences, the PLL dynamics predominantly affect the injected active and reactive power in both reference frames during faults with large phase jumps.

The presented model accurately describes how the phase angle estimation of PLLs affect the power factor and converter currents. Transient processes in the phase angle change the injected converter power, which is particularly critical during faults since the reactive power must be quickly provided to sufficiently support the grid voltages. The next two sections

present the detailed analysis of how δ affects the power factor distortions and the settling time of the reactive current for different fault scenarios.

5.6.1 PLL Impact on the Converter Power Factor

The PLL's immunity to voltage distortions mainly affects the power factor distortions. SSMs can sufficiently describe these characteristics since harmonics occur typically as small perturbations around an operating point. Eq. 5.48 is linearized to derive the SSM to determine the dynamics of the power factor λ during phase jumps. Therefore, G_i is neglected and $\sin(\varphi^*_{\mathrm{PLL}})$ is substituted by $\sqrt{1-\lambda^{*2}}$ in 5.48 according to:

$$\lambda = \cos(\varphi^*_{\mathrm{PLL}})\cos(\delta) + \sin(\varphi^*_{\mathrm{PLL}})\sin(\delta) = \lambda^*\cos(\delta) + \sqrt{1-\lambda^{*2}}\sin(\delta) \quad . \tag{5.49}$$

Then, λ^*_0 is defined as operating point of the power factor reference, whereas $\delta_0 = 0$ rad is the constant operating point of the phase angle, which leads to:

$$\Delta\lambda = \Delta\lambda^* + \sqrt{1-\lambda^{*2}_0}\Delta\delta = \Delta\lambda^* + \sin(\varphi^*_{\mathrm{PLL},0})\Delta\delta \quad . \tag{5.50}$$

Accordingly, $\sin(\varphi^*_{\mathrm{PLL},0})$ is the operating point of $\sin(\varphi^*_{\mathrm{PLL}})$. The linear equation for the power factor indicates that the estimated phase angle $\Delta\delta$ only affects the power factor if $\lambda^*_0 \neq 1$ or $\sin(\varphi^*_{\mathrm{PLL}}) \neq 0$, respectively. In contrast, the largest impact of $\Delta\delta$ on λ occurs for $\lambda^*_0 = 0$ or $\sin(\varphi^*_{\mathrm{PLL}}) = 1$, respectively. Based on 5.50 and assuming $\Delta\lambda^* = 0$ (constant power factor reference), the disturbance transfer function of the power factor with the voltage harmonics $\tilde{v}_{\mathrm{PLL,q+}}$ as input can be expressed as:

$$G_{\mathrm{d,pf}}(s) = \frac{\Delta\lambda}{\tilde{v}_{\mathrm{PLL,q+}}} = \sin\left(\varphi^*_{\mathrm{PLL},0}\right)\frac{\theta'}{\tilde{v}_{\mathrm{PLL,q+}}} = \sin\left(\varphi^*_{\mathrm{PLL},0}\right)G_{\mathrm{d}}(s) \quad . \tag{5.51}$$

Substituting $\Delta\lambda$ in equation 5.51 by 5.50 and assuming $\Delta\delta|_{\theta=0} = \theta'$ reveals the equivalence between $G_{\mathrm{d,pf}}(s)$ and the disturbance transfer function of the PLL G_{d}, which is only scaled by $\sin\left(\varphi^*_{\mathrm{PLL},0}\right)$.

The derived power factor model is tested with type E faults. The current references $\mathbf{i}^*_{\mathrm{dq}}$ are selected according to the FRT requirements shown in Fig. 5.18. The results for the distortions of the estimated phase angle $\hat{\delta}$ and the respective distortions of the power factor $\hat{\lambda}$ are shown in Fig. 5.69 and 5.70. They confirm the theoretical expectations for all four PLLs. For the power factor operating point $\lambda^*_0 = 1$ ($\sin(\varphi^*_{\mathrm{PLL},0}) = 0$) and $V^+ > 0.9$ pu, $\hat{\delta}$ does not affect $\hat{\lambda}$. For decreasing voltage sags in the range of 0.5 pu $< V^+ <$ 0.9 pu, $\hat{\lambda}$ increases since λ^*_0 is decreasing ($\sin(\varphi^*_{\mathrm{PLL},0})$ is increasing) due to the FRT requirements. Finally, $\lambda^*_0 = 0$ ($\sin(\varphi^*_{\mathrm{PLL},0}) = 1$) for $V^+ < 0.5$ pu, and thus $\hat{\lambda}$=$\hat{\delta}$. These characteristics are valid for all four analyzed PLLs, which verifies the extracted disturbance model in 5.51 and its general applicability to SRF-based PLLs.

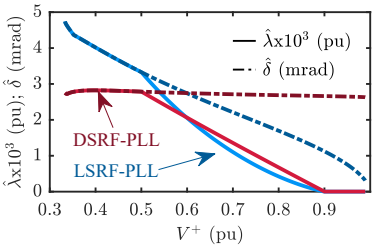


Figure 5.69: Power factor distortion amplitude $\hat{\lambda}$ and estimated phase angle distortions $\hat{\delta}$ of LSRF- and DSRF-PLL during type E faults with different sag depths.

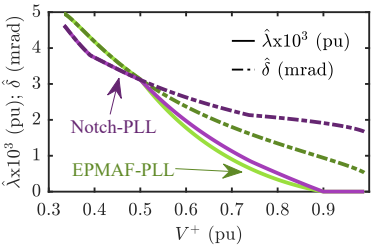


Figure 5.70: Power factor distortion amplitude $\hat{\lambda}$ and estimated phase angle distortions $\hat{\delta}$ of Nf- and EPMAF-PLL during type E faults with different sag depths.

The power factor distortions depend on the distortions in the estimated phase angle extracted by the PLL. However, the influence significantly changes with the power factor or current references, respectively. In normal operation, the power factor reference of the converter is typically in the range of 0.85-1, where the phase angle distortions do not affect the power factor. In contrast, the power factor reference decreases to zero for severe grid faults, where the estimated phase angle distortions directly distort the power factor. Since $\hat{\lambda}$=$\hat{\delta}$ is the worst-case scenario, the power factor requirement in the grid codes can be directly applied to the distortions of the estimated grid angle as already assumed for the design process in section 5.4.

5.6.2 PLL Impact on the Converter Current Control

The model presented in Fig. 5.64 sufficiently describes the effect of the error of the estimated phase angle on the grid currents. Fig. 5.66 shows simulation results that emphasize the massive impact of the PLL phase angle on the current control dynamics during grid voltage transients. But how can these relations be interpreted and which current settling times can be expected for different fault scenarios depending on the PLL and its design? These questions are answered using the model derived in 5.47:

$$\mathbf{i}_{\mathrm{dq}} = \mathbf{T}_{\delta}\mathrm{G}_i(s)\mathbf{i}^*_{\mathrm{dq,PLL}} \quad , \tag{5.52}$$

which is linearized to identify critical relations and scenarios.
The transfer characteristics $\mathbf{x}_{\mathrm{PLL,dq+}} = [x_{\mathrm{PLL,d+}}\ x_{\mathrm{PLL,q+}}]^{\mathrm{T}}$ to θ are derived from the block diagram in Fig. 5.64 by defining $x_{\mathrm{PLL,d+}} = \cos(\delta)$ and $x_{\mathrm{PLL,q+}} = \sin(\delta)$. The resulting transfer

functions are linearized around the steady-state operating point $\theta_0 - x_{\mathrm{PLL,q+},0} G_{\mathrm{ol}} = \delta \approx 0$, which yields the linear dependency of $\Delta\mathbf{x}_{\mathrm{PLL,dq+}}$ on the linearized phase angle $\Delta\theta$:

$$\begin{bmatrix} x_{\mathrm{PLL,d+}} \\ x_{\mathrm{PLL,q+}} \end{bmatrix} = \begin{bmatrix} \cos\left(\theta - x_{\mathrm{PLL,q+}} G_{\mathrm{ol}}\right) \\ \sin\left(\theta - x_{\mathrm{PLL,q+}} G_{\mathrm{ol}}\right) \end{bmatrix} \Rightarrow \begin{bmatrix} \Delta x_{\mathrm{PLL,d+}} \\ \Delta x_{\mathrm{PLL,q+}} \end{bmatrix} = \begin{bmatrix} 1 \\ \frac{1}{1+G_{\mathrm{ol}}} \Delta\theta \end{bmatrix} . \tag{5.53}$$

Then, the definition of $\mathbf{x}_{\mathrm{PLL,dq+}}$ is applied to $\mathbf{T}_\delta$, and the current transfer characteristic according to 5.47 is linearized around the generic operating point defined by $\mathbf{i}_{\mathrm{dq,PLL},0}$ and $\mathbf{x}_{\mathrm{dq,PLL},0}$:

$$\mathbf{i}_{\mathrm{dq}} = \begin{bmatrix} x_{\mathrm{PLL,d+}} & x_{\mathrm{PLL,q+}} \\ -x_{\mathrm{PLL,q+}} & x_{\mathrm{PLL,d+}} \end{bmatrix} G_{\mathrm{i}} \mathbf{i}^*_{\mathrm{dq,PLL}} \tag{5.54}$$

$$\Rightarrow \Delta\mathbf{i}_{\mathrm{dq}} = \begin{bmatrix} x_{\mathrm{PLL,d+},0} & x_{\mathrm{PLL,q+},0} & i^*_{\mathrm{d,PLL},0} & i^*_{\mathrm{q,PLL},0} \\ -x_{\mathrm{PLL,q+},0} & x_{\mathrm{PLL,d+},0} & i^*_{\mathrm{q,PLL},0} & -i^*_{\mathrm{d,PLL},0} \end{bmatrix} G_{\mathrm{i}} \begin{bmatrix} \Delta\mathbf{i}^*_{\mathrm{dq,PLL}} \\ \Delta\mathbf{x}_{\mathrm{PLL,dq+}} \end{bmatrix} . \tag{5.55}$$

Substituting $[\Delta x_{\mathrm{PLL,d+}} \ \Delta x_{\mathrm{PLL,q+}}]^{\mathrm{T}}$ in 5.55 and assuming that $x_{\mathrm{PLL,d+},0} = 1$ pu and $x_{\mathrm{PLL,q+},0} = 0$ pu, which is valid for the PLLs in the steady-state, leads to the converter current transfer functions:

$$\Delta\mathbf{i}_{\mathrm{dq}} = \begin{bmatrix} 1 & 0 & \frac{i^*_{\mathrm{q,PLL},0}}{1+G_{\mathrm{ol}}} \\ 0 & 1 & -\frac{i^*_{\mathrm{d,PLL},0}}{1+G_{\mathrm{ol}}} \end{bmatrix} G_{\mathrm{i}} \begin{bmatrix} \Delta\mathbf{i}^*_{\mathrm{dq,PLL}} \\ \Delta\theta \end{bmatrix} + G_{\mathrm{i}} \mathbf{i}^*_{\mathrm{dq,PLL},0} . \tag{5.56}$$

These linear transfer characteristics include the typical current response to reference steps $G_{\mathrm{i}}\mathbf{i}^*_{\mathrm{dq,PLL},0}$ and additionally describe the step response to phase angle jumps. Eq. 5.56 indicates that the current response to grid voltage disturbances strongly depends on the phase angle, current references, and the PLL open-loop transfer function. This means, that the converter current dynamics may behave like the dynamics of the estimated phase angle error depending on the current references. Considering the definition of the error transfer function of the PLLs $\delta/\Delta\theta$ and substituting $\Delta\theta$ in 5.56, leads to:

$$\frac{\delta}{\Delta\theta} = \frac{1}{1+G_{\mathrm{ol}}} \Rightarrow \qquad \Delta\mathbf{i}_{\mathrm{dq}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} G_{\mathrm{i}} \Delta\mathbf{i}^*_{\mathrm{dq,PLL}} + G_{\mathrm{i}} \mathbf{i}^*_{\mathrm{dq,PLL},0} + \begin{bmatrix} i^*_{\mathrm{q,PLL},0} \\ -i^*_{\mathrm{d,PLL},0} \end{bmatrix} G_{\mathrm{i}} \delta \tag{5.57}$$

This expression describes the coupling between i_{d} and $i^*_{\mathrm{q,PLL}}$ or i_{q} and $i^*_{\mathrm{d,PLL}}$ depending on δ during grid voltage transients. In the worst-case, i.e., $\mathbf{i}^*_{\mathrm{dq}} = [1\ 1]$ pu, the converter current to phase angle transfer function is identical to the error transfer function $\delta/\Delta\theta$ of the PLL. Consequently, the step response of the estimated phase angle error is identical to the current step response during grid voltage disturbances (see 5.57). This equivalence is critical since the PLL time constant is typically much larger than the current control time constant.

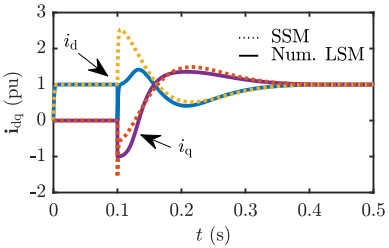


Figure 5.71: Grid currents $\mathbf{i}_{dq}$ during a phase angle jump of $-\pi/2$ at 0.1 s with current references step to $\mathbf{i}^*_{dq,PLL} = [1\ 1]^T$ pu derived with the SSM and numerical model (Num. LSM).

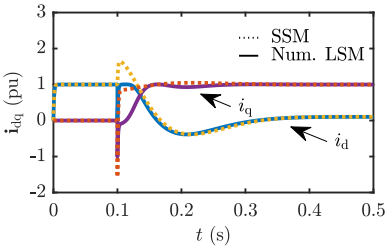


Figure 5.72: Grid currents $\mathbf{i}_{dq}$ during a phase angle jump of $-\pi/2$ at 0.1 s with current references step to $\mathbf{i}^*_{dq,PLL} = [0\ 1]^T$ pu derived with the SSM and numerical model (Num. LSM).

The SSM is validated with the numerical model during a large phase angle jump of $-\pi/2$ and different current reference steps using the LSRF-PLL with the ζ_{opt} design parameters. Fig. 5.71 shows the results with the initial references of $\mathbf{i}^*_{dq,PLL} = [1\ 0]^T$ pu. At $t = 0.1$ s the phase angle jump is applied that triggers a reference step to $\mathbf{i}^*_{dq,PLL} = [1\ 1]^T$ pu, instantaneously. The SSM yields similar results as the LSM, but the first 40 ms after the step differ significantly since the assumption $\delta \approx 0$ is critically violated there. However, this does not critically affect the error of the current settling time predicted by the SSM, which is in the small range of 2-3%. The models are compared again with the same initial conditions and phase angle jump but using $\mathbf{i}^*_{dq,PLL} = [0\ 1]^T$ pu for the current reference step. The comparison of the LSM and SSM shows significant differences in the first 40 ms due to the large δ. These differences lead to large variations in the predicted settling time of the q-component in this scenario, i.e., $t_{set,i_{q,SSM}} = 27$ ms to $t_{set,i_q} = 44$ ms. Contrarily, the slow response of i_d is accurately captured by the SSM.

Both test scenarios are also analyzed regarding the critical coupling mechanism between the dq-components of the current references. In the first test, the d and q-current, show an oscillation with a large time constant in the range of the PLL time constant that leads to a settling time $t_{set,\mathbf{i}_{dq}}$ of 220 ms using a tolerance band of 0.1 pu. The results of the second test indicate that i_d has similar dynamics as in the previous test with $t_{set,i_d} = 185$ ms but i_q shows a much quicker response with $t_{set,i_q} = 44$ ms. This finding confirms the predicted relation that the coupling of the dq-current references highly deteriorates the converter current settling time during phase angle jumps. These results confirm the predicted, critical coupling mechanism between i_d and $i^*_{q,PLL}$ or i_q and $i^*_{d,PLL}$ triggered by δ.

The type A fault was already defined as the worst-case for transient processes in the grid. Now, the impact of the settling time of δ on the settling of converter's reactive current during different type A faults is analyzed. Fig. 5.73 and Fig. 5.75 present the δ settling time for the LSRF- and Nf-PLL, and DSRF- and EPMAF-PLL, respectively. A constant settling tolerance band of $0.1 \cdot \pi/2$ is assumed. The settling time typically increases with smaller V^+

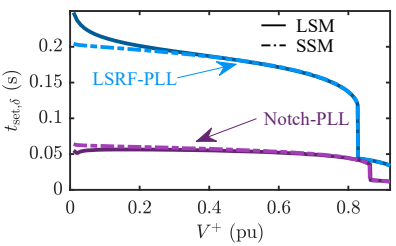


Figure 5.73: Settling time of the estimated phase angle for the LSRF- and Nf-PLL during type A faults considering a tolerance band of 0.1 $\pi/2$.

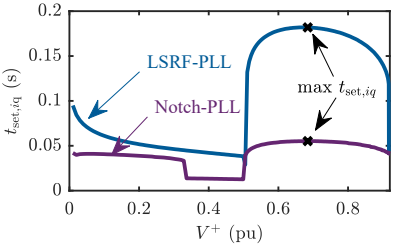


Figure 5.74: Settling time of the reactive current for the LSRF- and Nf-PLL during type A faults considering a tolerance band of 0.1 pu.

since the phase angle jumps are getting larger, indicating the worst-case for the settling at $V^+ = 0.05$ pu. The short settling times for $V^+ > 0.8$ pu are due to the small phase angle jumps compared to the absolute tolerance band. The LSMs and SSMs show similar results except for the DSRF PLL, which is getting unstable as indicated by the large settling times for small V^+ (see Fig. 5.75).

The comparison of these findings with the settling times of i_q in Fig. 5.74 and 5.76 show that the worst-case for the δ settling time not necessarily coincides with the i_q settling time. The changing current references cause this effect. The active current reference is zero for $V^+ < 0.5$ pu leading to a significant decrease of the reactive current settling times since the current control and PLL dynamics are almost decoupled. Contrarily, the settling time $t_{\mathrm{set},iq}$ and $t_{\mathrm{set},\delta}$ are almost identical for 0.5 pu $< V^+ <$ 0.8 pu.

The largest settling time max $t_{\mathrm{set},iq}$ occurs for all analyzed PLLs for the same fault scenario with $V^+ = 0.68$ pu. According to 5.56, the product of $i^*_{\mathrm{d,PLL}}$ and $\Delta\theta$ serves as input for the current transfer function and thus affects the settling time of the converter current. Deriving the fault scenario that leads to $\max(i^*_{\mathrm{d,PLL}} \cdot \Delta\theta)$ results in $V^+ = 0.68$ pu, which is identical to the numerical results. Accordingly, the worst-case for the fault dynamics occurs not at the most severe type A fault with $V^+ = 0.05$ pu but at the maximum coupling of the current control with the PLL dynamics at $V^+ = 0.68$ pu.

The fault clearing can be more critical for the reactive current dynamics than the fault initiation since the current references are typically $\mathbf{i}^*_{\mathrm{dq,PLL}} = [1\ 0]^\mathrm{T}$ pu after fault clearing, and do not depend on the fault scenario. Hence, the current response is dominated by $\delta(t) \propto i_\mathrm{q}(t)$ for all fault clearing processes, as exemplarily shown in Fig. 5.77. This relation is critical since the slow response of the reactive current leads to over-voltages at the PCC that may trip the converter system.

In contrast to the fault initiation, where the reactive current must meet strict rise and settling time requirements, the grid codes do not provide strict requirements for the active current increase after fault clearing. The VDE code in [11] demands a maximum rise time of one

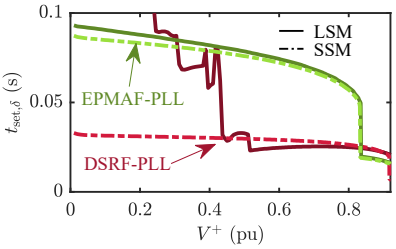


Figure 5.75: Settling time of the estimated phase angle for the DSRF- and EPMAF-PLL during type A faults considering a tolerance band of 0.1 $\pi/2$.

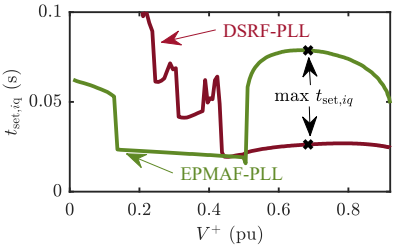


Figure 5.76: Settling time of the reactive current for the DSRF- and EPMAF-PLL during type A faults considering a tolerance band of 0.1 pu.

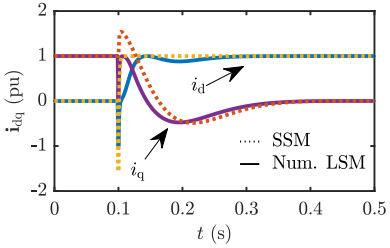


Figure 5.77: Grid currents $\mathbf{i}_{\mathrm{dq}}$ of the VOC with LSRF-PLL during fault clearing at 0.1 s with current references step to $\mathbf{i}^*_{\mathrm{dq,PLL}} = [1\ 0]^{\mathrm{T}}$ derived with the SSM and numerical model (Num. LSM).

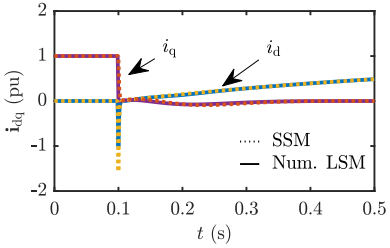


Figure 5.78: Grid currents $\mathbf{i}_{\mathrm{dq}}$ of the VOC with LSRF-PLL during fault clearing at 0.1 s with current references step to $\mathbf{i}^*_{\mathrm{dq,PLL}} = [1\ 0]^{\mathrm{T}}$ and delayed active current provision derived with the SSM and numerical model (Num. LSM).

second for the active current. This fact can be used to speed up the reactive current response by introducing a delay in the active current increase. In the presented test, the settling time of the reactive current using an LSRF-PLL is reduced from 106 ms without active current delay to 2.4 ms with an active current delay using a low-pass filter with $\tau = 0.6$ s. This solution highly decreases the probability of overvoltage and converter tripping during fault clearing.

With the proposed solution, the dynamics of the fault clearing are no longer critical for the transient behavior of the converter current, and the PLL design and evaluation can focus on the settling time constraints introduced by the reactive current response during fault initiation. This constraint contains a maximum settling time of 60 ms in accordance with [11] and becomes critical due to the coupling mechanism of the PLL.

The dynamic performance of the analyzed PLLs for both derived design parameter sets ($\zeta_{0.7}$ and ζ_{opt}) can be compared regarding their settling times of the reactive current. The settling times of both PLL designs presented in Fig. 5.79 and 5.80 are derived with the LSMs and show the expected dependency on the fault scenario. All PLLs achieve shorter settling times

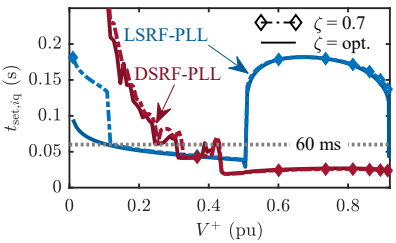


Figure 5.79: Settling time of the estimated phase angle of the LSRF- and Nf-PLL during type A faults considering a tolerance band of 0.1 pu and the two design parameter sets based on the $\zeta_{0.7}$ and ζ_{opt} optimization.

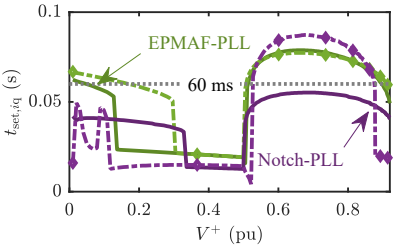


Figure 5.80: Settling time of the estimated phase angle of the DSRF- and EPMAF-PLL during type A faults considering a tolerance band of 0.1 pu and the two design parameter sets based on the $\zeta_{0.7}$ and ζ_{opt} optimization.

for ζ_{opt} in comparison to $\zeta_{0.7}$, particularly, for smaller V^+. Only the Nf-PLL has significantly shorter settling times for $\zeta_{0.7}$ during faults with small V^+. However, in the critical range of $0.5\ \mathrm{pu} < V^+ < 0.8\ \mathrm{pu}$, the settling is significantly decreased with the optimum design. Using this design, the Nf-PLL based current control achieves conformity with the grid codes, since $t_{\mathrm{set},iq} < 60$ ms for all fault scenarios. The other three analyzed PLLs are not able to meet this requirement.

This section presents the detailed description and modeling of the coupling mechanism between the converter current control and the PLL during severe faults. Moreover, the impact of the chosen scenarios on the PLL design is analyzed. The results confirm that the maximum power factor distortions can be directly designed by the immunity to voltage distortions of PLLs. However, to evaluate the current dynamics based on the estimated phase angle error is not straightforward since they are dominated by the coupling of dq-components during phase angle jumps. A delay in the active current reference after fault clearing may solve this problem. This solution does not work for the fault initiation, though, due to grid code requirements. Hence, the PLLs must be designed to meet the dynamic requirements on the settling time of the reactive current. In the presented tests, only the Nf-PLL is able to meet the settling time requirement in all fault scenarios. This is achieved by optimizing both design parameters, i.e., ω_{c} and ζ, since the design with $\zeta_{0.7}$ also fails.
The presented PLL evaluation is comparable since all PLLs are designed with the same optimization objective and application scenarios. However, in the case of the DSRF-PLL, the SSM does not predict its instability, so that the DSRF performance based on this design cannot be directly compared. This problem is solved by a multi-fidelity model-based design process for PLLs proposed and presented in the next section.

5.7 Multi-Fidelity Model-based Design for PLLs under Severe Grid Disturbances

The proposed SSM-based PLL design is applicable for most of the analyzed PLLs. However, mainly the SSM of the DSRF-PLL fails to predict the estimated phase angle settling time accurately, and even worse cannot capture the transient stability boundary of the design parameter space. A similar problem can be expected with the DSOGI-PLL since it is described with the same SSM, and thus relies on the same assumptions. In order to overcome this problem, other design processes from the literature propose to limit the bandwidth of the PLLs to one/fifth of the notch-characteristic [124]. This rule is only a general guideline and may be too conservative to achieve a fast settling time.

The SSM-based design process was presented in section 5.4 and an overview of the process steps is shown in Fig. 5.45. The immunity to distortions evaluation utilizes the SSMs that show sufficient accuracy for the harmonics in the investigated range. Contrarily, the estimated phase angle settling times show significant differences between the SSM and LSM. These differences are not surprising since the investigated transient scenarios contain substantial voltage sags and phase angle jumps. The SSM completely neglects the ANS, and in the case of the DSRF and DSOGI, the phase angle and frequency feedback to the filters, respectively. So, the LSM should be used for more accurate settling time evaluations. Moreover, the LSM is able to predict transient stability phenomena such as the instability of the DSRF-PLL or DSOGI-PLL.

The presented design process in section 5.4 is modified, so that the settling time of the estimated phase angle is extracted with the LSM during a type A fault with $|\underline{Z}_\mathrm{F}|$=0.05 pu, $|\underline{Z}_\mathrm{S}|$=1 pu, r_F=0 pu, and r_S=1 pu, and $f_1 = 50$ Hz. The LSM-based design typically increases the computational burden of the optimization. Consequently, a multi-fidelity approach is chosen to limit this burden. First, the design parameter combinations are reduced to the valid parameter sets that comply with the necessary immunity to distortions. Second, the settling times of δ are simulated with the LSM only for the valid parameter sets.

The resulting settling time of phase angle error $t_{\mathrm{set},\delta}$ is presented in Fig. 5.82 for the DSRF-PLL and shows significant differences to the SSM results in Fig. 5.81. A large subset of the design parameter space leads to an unstable step response of the DSRF-PLL. This transient instability region, which cannot be predicted by the SSM, limits the maximum bandwidth. This is critical since the SSM-based design leads to design parameters that are located in the unstable region of the design parameter space. Hence, in the case of the DSRF-PLL, an SSM-based design is prone to instability.

The LSM-based design also enables the design process to optimize the DSOGI-PLL without relying on the equivalence to the DSRF. Although, the optimum design parameters extracted with the SSM lead to an unstable PLL comparable to the DSRF, the results also show significant differences. The stable design parameter space reaches significantly higher control

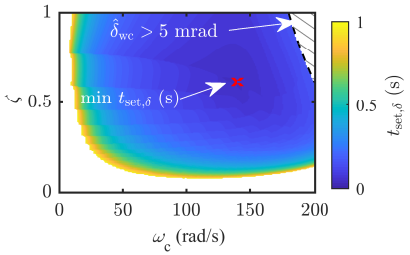


Figure 5.81: Angle error settling time $t_{set,\delta}$ of the DSRF-PLL for different design parameter sets ω_c and ζ extracted with the SSM and identification of the set for minimum settling time considering the maximum distortion criteria.

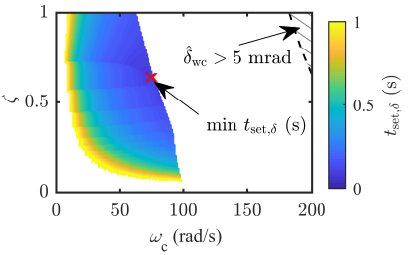


Figure 5.82: Angle error settling time $t_{set,\delta}$ of the DSRF-PLL for different design parameter sets ω_c and ζ extracted with the LSM and identification of the set for minimum settling time considering the maximum distortion criteria.

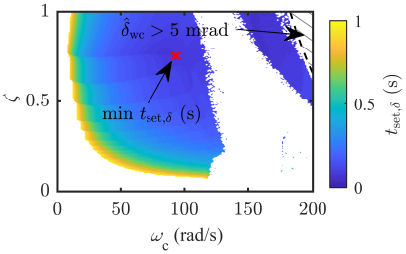


Figure 5.83: Angle error settling time $t_{set,\delta}$ of the DSOGI-PLL for different design parameter sets ω_c and ζ extracted with the LSM and identification of the set for minimum settling time considering the maximum distortion criteria.

bandwidth for the DSOGI, and thus enables faster dynamics. Unfortunately, the stable parameter combinations next to the maximum distortion boundary, which is indicated by $\hat{\delta}_{wc}$, show a small stability margin and high sensitivity to fault parameters. Therefore, control bandwidths of $\omega_c > 130$ rad/s are not considered in the optimization.

The multi-fidelity optimization is applied to all analyzed PLLs and the results are summarized in Table 5.5. The LSRF and EPMAF show only minor differences between the SSM-based and LSM-based designs. The design parameters of the other PLLs change significantly. The control bandwidths of the DSRF is almost halved, and the DSRF bandwidth is decreased by 33%. The Nf-PLL bandwidth increases by 31%, but this change is mainly caused by an extension of the damping ratio range to $0 < \zeta < 2$.

The LSM-based design achieves much faster settling times of the converter current for the DSOGI, DSRF, and Nf-PLL, as shown in Fig. 5.84 and 5.85. The DSOGI and DSRF are

Table 5.5: Design parameter results for the LSM-based optimization process. The values in brackets indicate the change in comparison to the SSM-based design.

PLLs	$\omega_{c,opt,LSM}$ (rad/s)	$\zeta_{opt,LSM}$
LSRF	26.25 (+1.12)	0.74 (-0.04)
DSRF	74.00 (-64.23)	0.64 (+0.02)
DSOGI	93.20 (-45.03)	0.76 (+0.14)
Nf	101.60 (+23.06)	1.03 (+0.15)
EPMAF	50.00 (-0.27)	0.84 (+0.01)

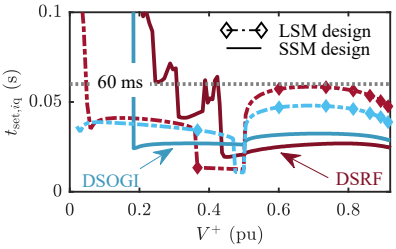


Figure 5.84: Settling time of the estimated phase angle of the DSRF- and DSOGI-PLL during type A faults considering a tolerance band of 0.1 pu.

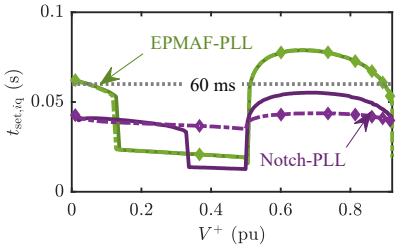


Figure 5.85: Settling time of the estimated phase angle of the Nf- and EPMAF-PLL during type A faults considering a tolerance band of 0.1 pu.

stable until $V^+ < 0.05$, which is sufficient for most grid codes. Moreover, they do not exceed the maximum settling time of 60 ms anymore, and the DSOGI achieves a slightly lower settling time in most scenarios. The Nf-PLL could further improve its settling time and is still below the limit of 60 ms for all scenarios. With the multi-fidelity model-based design, the design parameter optimization can be improved due to its more accurate settling time data. But particularly for the DSRF and DSOGI, the LSM-based design is crucial since the instability finally affects the suitable design parameter space. It identifies the transient stability boundary in the design space and reveals the differences between DSRF and DSOGI. Accordingly, the DSOGI-PLL achieves shorter settling times than the DSRF in a broader grid fault operating range.

The presented optimization consists of a robust design framework and process to conduct comparative studies of PLLs with optimized design to comply with grid codes considering the power factor distortion and reactive current settling time. The model-based design identifies PLL properties and possible improvements such as optimization of control bandwidth and damping, identification of critical coupling mechanism of the PLLs with the current control, rejection of overvoltages after fault clearing by active current delay, and identification of the transient stability boundary for the design parameters of the DSRF- and DSOGI-PLL.

The LSM-based design framework can capture the transient stability phenomena of PLLs during faults, because it can accurately describe the input-output characteristics. However,

it is not suitable for deriving analytical stability criteria. Therefore, the next section presents the analytical assessment of transient stability for PLLs with prefilter.

5.8 Transient Stability Phenomena caused by the PLL

The PLLs may show instability phenomena that cannot be explained with Linear Time-Invariant (LTI)-models. These phenomena are closely related to the Loss of Synchronization (LOS) as one of the most critical scenarios for converter-based generation units [143], [8], [144]. The instability mechanism is complex since it is caused by the interaction of the current control with the PLL in weak grids and the trigonometric function $\sin(\delta)$ introduced by Park's transformation. Hence, it is influenced by the interaction of different equilibria that cannot be captured by LTI-models.

The transient stability of PLLs has attracted much attention, particularly, the interaction with the current control for weak grid conditions [145] [143], [146], [147]. These contributions mainly focus on the SRF-PLL without any prefilter, however, as shown, this PLL is typically not able to meet the required immunity to distortions and bandwidth. With this simplified PLL structure, the phase-portrait technique and the Equal Area Criterion (EAC) can be directly applied since the systems are typically of second-order. Sophisticated PLL structures for unbalanced and distorted grids, e.g., LSRF, DSRF, are often higher-order systems that cannot be directly analyzed with these techniques but with Lyapunov's direct method [98], [148]. An overview of the application of Lyapunov's direct method for higher order PLLs is given in [149]. Recently, Guangyu presented the transient stability analysis for a nonlinear PLL with the same method [150]. However, the evaluation of the transient stability of the LSRF-PLL based on Lyapunov's direct method and the relation to its design based on the Symmetrical Optimum (SO) is still an open point, which will be presented in this section.

The large-signal structure of the LSRF-PLL is shown in Fig. 5.86 indicating the states of the system x_1, x_2, and x_3. The nonlinear dynamic matrix $\mathbf{A}(\mathbf{x})$ and its linear equivalent can be obtained from this block diagram and leads to:

$$\dot{\mathbf{X}} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} x_2 + x_3 k_\mathrm{p} \\ x_3 k_\mathrm{i} \\ -\omega_\mathrm{f}\left(\hat{V}_{\mathrm{S},1}\sin\left(x_1\right) + x_3\right) \end{bmatrix} \qquad \dot{\mathbf{X}}_\mathrm{lin}\big|_{\delta_0=0} = \begin{bmatrix} 0 & 1 & k_\mathrm{p} \\ 0 & 0 & k_\mathrm{i} \\ -\omega_\mathrm{f}\hat{V}_{\mathrm{S},1} & 0 & -\omega_\mathrm{f} \end{bmatrix} \Delta\mathbf{x} \quad . \tag{5.58}$$

This equation describes the large-signal system dynamics and due to the term $\sin(\delta)$, this system has an infinite count of equilibria on the x_1-axis or δ-axis, respectively.

The derived system equations can be directly verified with the numerical large-signal model since they rely on the same model assumptions, and thus, should yield the same results. The trajectories $x_1(t)$, $x_2(t)$, and $x_3(t)$ of both models for a severe transient process, i.e., a phase angle jump of $\pi/2$, are shown in Fig. 5.87 and Fig. 5.88, and describe precisley the same

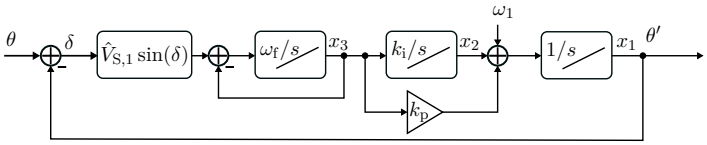


Figure 5.86: Block diagram of the nonlinear state-space model of LSRF-PLL.

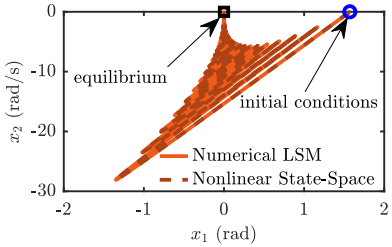


Figure 5.87: Trajectory of the states $\dot{\delta}$ and δ of the LSRF-PLL for a phase angle jump of $\pi/2$ calculated with the numerical LSM and the nonlinear state-space model.

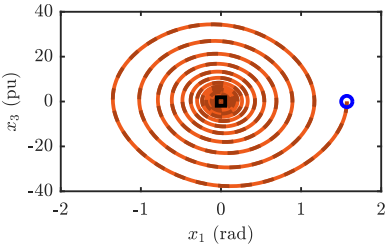


Figure 5.88: Trajectory of the states $\ddot{\delta}$ and δ of the LSRF-PLL for a phase angle jump of $\pi/2$ calculated with the numerical LSM and the nonlinear state-space model.

transient process. This finding confirms the expected accuracy of the model according to 5.58. Now, the analysis techniques for nonlinear systems can be applied to this model.

The phase-portrait is a suitable technique to visualize the state-space characteristics of nonlinear systems up to the second-order. The LSRF-PLL is of order three, and thus its phase portrait consist of three dimensions, which cannot be sufficiently visualized. Therefore, only the phase-portrait and velocity plot of the SRF-PLL is presented in Fig. 5.89. The velocity vector $\dot{\mathbf{X}}$ can be directly drawn based on 5.58 for any point in the state-space and shows the direction and velocity of the trajectory in the state-space moving forward in time. Hence, deriving the equilibria and analyzing the vector field in the neighborhood of them reveals their stability properties. The equilibria of the system can be divided into Stable Equilibrium Points (SEPs) and Unstable Equilibrium Points (UEPs). For the SEPs, the trajectory converges to these points if the initial condition is in its neighborhood, which indicates asymptotic stability. Contrarily, the trajectories next to the UEPs will move away from these points. These conclusions can be drawn by analyzing the velocity vector $\dot{\mathbf{X}}$ in the neighborhood of these equilibria. Exemplary, three initial condition are chosen, and their trajectories are plotted. Two of them are unstable, whereas the third one converges into the origin.

Unfortunately, the phase-portrait, which is often used in recent publications ([143], [146]), is not a suitable technique for analyzing the stability of higher-order PLLs since the interpretation is too complex. So, Lyapunov's method should be applied to achieve analytical stability

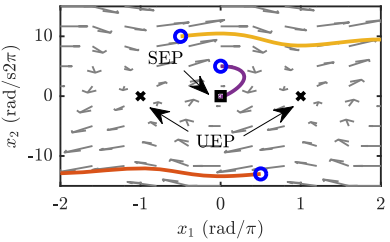


Figure 5.89: Velocity plot with phase portrait of the SRF-PLL highlighting the SEP and UEPs in the plotted range of δ and $\dot{\delta}$.

criteria. It is divided into the indirect method and direct method. The indirect method is still based on the linearized state equations given in 5.58. The direct method is more complex but directly derives the stability properties from the nonlinear system equations [148].
Based on Lyapunov's indirect method, the stability of an equilibrium of a nonlinear system can be proved with the stability of the linear representation, if the system has no eigenvalues λ_{ev} on the imaginary axis. The characteristic polynomial can be derived from 5.58 and results in:

$$\lambda_{\mathrm{ev}}^3 + \underbrace{\omega_{\mathrm{f}}}_{a_2}\lambda_{\mathrm{ev}}^2 + \underbrace{\omega_{\mathrm{f}}\hat{V}_{\mathrm{S},1}k_{\mathrm{p}}}_{a_1}\lambda_{\mathrm{ev}} + \underbrace{\omega_{\mathrm{f}}\hat{V}_{\mathrm{S},1}k_{\mathrm{i}}}_{a_0} = 0 \quad . \tag{5.59}$$

Using the Routh-Hurwitz criterium $a_2 a_1 > a_0$ leads to the criterium for asymptotic stability of the LSRF-PLL design parameters:

$$\frac{k_{\mathrm{i}}}{\omega_{\mathrm{f}}} - k_{\mathrm{p}} < 0 \quad . \tag{5.60}$$

However, this result does not provide sufficient information in which region of the state-space this property is valid. Therefore, Lyapunov's direct method must be applied: First, the positive definite energy function V in 5.61 is defined as Lyapunov candidate that fits for a system with trigonometric terms according to [98], [149]. This function should be positive in the whole state-space except for the analyzed equilibrium $\mathbf{x}_0$, and thus $V(\mathbf{x}_0) = 0$. The integral is positive in the range of $-\pi < x_1 < \pi$ since $\int_0^{x_1} \sin(\sigma)\mathrm{d}\sigma = 1 - \cos(x_1)$. The second term is positive if $p_{11}p_{22} > p_{12}^2$ according to Sylvester's criterion.

$$V = \int_0^{x_1} \sin(\sigma)\mathrm{d}\sigma + \mathbf{x}^{\mathrm{T}} P \mathbf{x} = \int_0^{x_1} \sin(\sigma)\mathrm{d}\sigma + \frac{1}{2}\begin{bmatrix} x_2 & x_3 \end{bmatrix} \begin{bmatrix} p_{11} & p_{12} \\ p_{12} & p_{22} \end{bmatrix} \begin{bmatrix} x_2 \\ x_3 \end{bmatrix} \tag{5.61}$$

Then, $\dot{V}$ according to 5.62 must be negative definite to conclude that V is a Lyapunov function, and thus the equilibrium is locally asymptotically stable. Since the parameters of $\mathbf{P}$ can be chosen to meet this requirement, 5.62 is rearranged to obtain 5.63, and all terms

that do not contain quadratic state dependencies are set to zero (see 5.64). These operations lead to the definition of $\mathbf{P}$ in 5.64 that only depends on system parameters.

$$\dot{V} = \sin(x_1)\,\dot{x}_1 + p_{11}x_2\dot{x}_2 + p_{22}x_3\dot{x}_3 + p_{12}x_3\dot{x}_2 + p_{12}x_2\dot{x}_3 \tag{5.62}$$

$$\begin{aligned}\dot{V} = &\left(1 - p_{12}\omega_\mathrm{f}\hat{V}_{S,1}\right)\sin(x_1)\,x_2 + \left(k_\mathrm{p} - p_{22}\omega_\mathrm{f}\hat{V}_{S,1}\right)\sin(x_1)\,x_3 \\ &+ (p_{11}k_\mathrm{i} - p_{12}\omega_\mathrm{f})\,x_3x_2 + (p_{12}k_\mathrm{i} - p_{22}\omega_\mathrm{f})\,x_3^2\end{aligned} \tag{5.63}$$

$$\begin{aligned}&\left(1 - p_{12}\omega_\mathrm{f}\hat{V}_{S,1}\right) = 0 \\ &\left(k_\mathrm{p} - p_{22}\omega_\mathrm{f}\hat{V}_{S,1}\right) = 0 \;\Rightarrow \\ &(p_{11}k_\mathrm{i} - p_{12}\omega_\mathrm{f}) = 0\end{aligned} \qquad \mathbf{P} = \begin{bmatrix} \frac{1}{k_\mathrm{i}\hat{V}_{S,1}} & \frac{1}{\omega_\mathrm{i}\hat{V}_{S,1}} \\ \frac{1}{\omega_\mathrm{f}\hat{V}_{S,1}} & \frac{k_\mathrm{p}}{\omega_\mathrm{f}\hat{V}_{S,1}} \end{bmatrix} \tag{5.64}$$

This matrix must be positive definite to comply with the requirement that $V > 0$ except for $V(\mathbf{x}_0) = 0$. This can be checked with Sylvester's criterion $p_{11}p_{22} > p_{12}^2$ and leads to the same conclusion as the Routh-Hurwitz criterion that $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} < 0$. Substituting these relations in 5.63 yields

$$\dot{V} = (p_{12}k_\mathrm{i} - p_{22}\omega_\mathrm{f})\,x_3^2 = \left(\frac{k_\mathrm{i}}{\omega_\mathrm{f}\hat{V}_{S,1}} - \frac{k_\mathrm{p}}{\hat{V}_{S,1}}\right)x_3^2 \quad , \tag{5.65}$$

and

$$\dot{V} \leq 0 \Leftrightarrow \frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} \leq 0 \quad . \tag{5.66}$$

Unfortunately, $\dot{V}$ is only semi-positive definite since x_1 and x_2 are not included in $\dot{V}$ anymore and thus, the equilibrium is only locally stable and not necessarily locally, asymptotically stable. Lasalle's Invariance Principle must be applied to prove that the system is asymptotically stable. The set $M = \{\mathbf{x}|\dot{V} = 0\}$ should only contain the trajectory of $\mathbf{x}_0$, which is in this case the vector [0 0 0]. Checking this criterion leads to the conclusion that the equilibrium $\mathbf{x}_0$ of the LSRF-PLL is locally asymptotically stable for $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} > 0$ in the interval $-\pi < x_1 < \pi$.

This analysis is validated in simulation for two design parameter sets next to the stability boundary, i.e., $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = -0.0015$ and 0.0166. Fig. 5.90 and 5.91 show the trajectory for a phase angle jump of $\pi/2$ for a design parameter set with $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = -0.0015$. According to the stability criterion, the system should be asymptotically stable. The simulation confirms the stability and the constraints of Lyapunov's method that $V > 0\ \forall t$ and $\dot{V} \leq 0\ \forall t$. The other case with $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = 0.0166$ also confirms the criterion with $V > 0\ \forall t$ and $\dot{V} \geq 0\ \forall t$, as shown in Fig. 5.92 and 5.93.

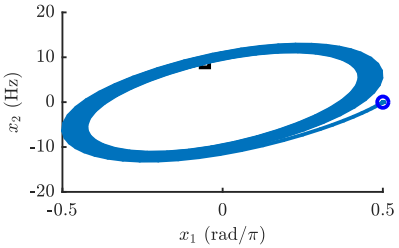


Figure 5.90: Trajectory of the states $\dot{\delta}$ and δ of the LSRF-PLL with $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = -0.0015$ for a phase angle jump of $\pi/2$ calculated with the nonlinear state-space model.

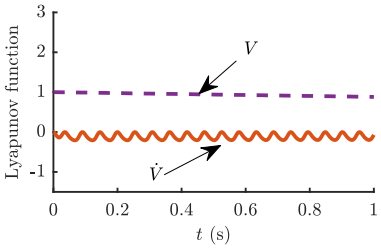


Figure 5.91: Lyapunov function V and its derivative $\dot{V}$ for the LSRF-PLL with $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = -0.0015$ for a phase angle jump of $\pi/2$ calculated with the nonlinear state-space model.

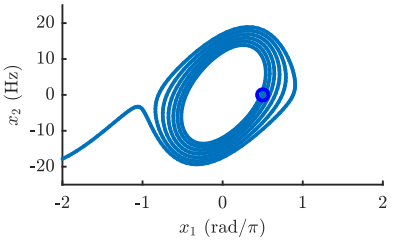


Figure 5.92: Trajectory of the states $\dot{\delta}$ and δ of the LSRF-PLL with $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = 0.0166$ for a phase angle jump of $\pi/2$ calculated with the nonlinear state-space model.

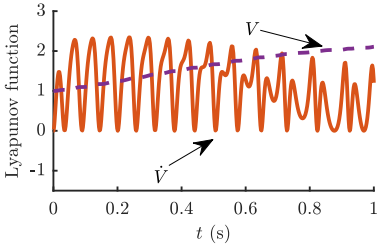


Figure 5.93: Lyapunov function V and its derivative $\dot{V}$ for the LSRF-PLL with $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} = 0.0166$ for a phase angle jump of $\pi/2$ calculated with the nonlinear state-space model.

The SO design process can be analyzed with the new insights into the stability behavior and the analytical stability criterion. Including the design rules of the SO according to 5.31-5.33 into the stability criterion $\frac{k_\mathrm{i}}{\omega_\mathrm{f}} - k_\mathrm{p} < 0$ leads to:

$$\frac{\frac{k_\mathrm{p}\omega_\mathrm{c}}{(2\zeta+1)}}{(2\zeta+1)} - \omega_\mathrm{c} = \frac{\omega_\mathrm{c}^2}{(2\zeta+1)^2\omega_\mathrm{c}} - \omega_\mathrm{c} < 0 \Rightarrow \qquad \zeta > 0 \quad . \tag{5.67}$$

Consequently, if the LSRF-PLL is designed with the SO, it is locally asymptotically stable for all ω_c and $\zeta > 0$ in the interval $-\pi < x_1 < \pi$.

The presented transient stability framework is a potent tool to derive parameter constraints for local asymptotic stability of PLLs. This was proved exemplary for the LSRF as the most simple structure of a PLL with prefilter. However, the application to more complex PLLs is not straightforward because deriving of the criteria gets increasingly complicated with larger system-order. Consequently, the use of Lyapunov's direct method for PLLs with advanced

prefilters is still an open research point for a better understanding of the presented instability mechanism.

In summary, this chapter comprises the following results:

- the most critical scenarios for grid converters to test the dynamics of the converter control,
- the dominant coupling mechanism of PLLs with the current control in stiff grids,
- a design framework and process to identify suitable PLL schemes and their optimum control parameters, and
- a method to assess the transient stability analytically based on Lyapunov's direct method.

Based on these findings, the DSOGI-PLL is identified as PLL with the shortest settling time considering stability and distortion immunity constraints. Consequently, the DSOGI-PLL is used for grid synchronization and sequence decomposition in the following analyses of the grid-following and grid-forming controls.

6 Grid-following Converter Control for Unbalanced Fault Ride-Through Operation Considering Grid Strength

Grid-following control comprises control schemes that rely on a grid synchronization unit. VOC is a mature and widely used control structure of the grid-following controls. It basically consists of a PLL and current control. The previous chapter presents the basic scheme of the VOC (see Fig. 5.63) but mainly focuses on the impact of the PLL on the converter control. Consequently, the previous analysis relies on the following simplifications:

- The current control is simplified to a PT1-transfer function without considering the converter's voltage limitation.
- Only positive sequence currents are considered but grid converters must deal with unbalanced systems during FRT. These unbalanced operating conditions require dual sequence current controllers that guarantee zero steady-state error for the positive and negative sequence current.
- The current reference calculation is not analyzed in detail. Particularly, prioritizing between positive and negative sequence currents during unbalanced grid faults may affect the grid voltage support or converter utilization.
- VOC has been analyzed in a stiff grid and typically achieves a sufficient control characteristic if the converter is connected to a stiff grid. However, a weak grid connection may lead to instability of the converter control.

This chapter aims to fill these gaps by deriving a complete control structure considering the dual sequence current control with voltage limitation and current reference generators with current limitation. This structure utilizes the tuned DSOGI-PLL developed in the previous chapter. The control performance is evaluated using the previously derived worst-case grid scenarios, which are modified to cover weak grid conditions.

Two types of basic dual sequence controllers are the PI-based or PR-based controls. Four PI-controllers operating in two reference frames, i.e., positive sequence dq-frame and negative sequence dq-frame, are necessary to control both sequence currents [76], [52]. In contrast, both

sequences can be directly controlled in the $\alpha\beta$-frame using two PR-controllers [77], [52]. The equivalence between PI-controllers and PR-controllers, in theory, is derived in [151] and [52, pp.151-156], but does not consider the sequence decomposition necessary for realizing a dual sequence control in the dq-frame. Therefore, this chapter presents a thorough comparison between both structures considering the sequence extraction algorithm and explaining the critical controller part by utilizing an SSM.
Besides the control structure, the dynamic performance of current controllers mainly depends on their control parameter design and the voltage limitation of the converter. Consequently, the design process for current controllers is summarized, and different limitation algorithms are compared throughout this section. Finally, a combination of Peak Voltage Limitation (PVL) and Vector Voltage Limitation (VVL) is proposed that guarantees the best trade-off between both limitation concepts, i.e., fast dynamic performance and low Total Harmonic Distortion (THD). The control performance is evaluated for reference steps and grid voltage disturbances. Therefore, the power model presented in chapter 5 is extended to the negative sequence, and the LSM and SSM are experimentally validated using the test bench introduced in chapter 4.2.1.

Once the converter accurately controls the positive and negative sequence current during FRT, it may provide unbalanced currents during unbalanced faults. These unbalanced currents might lead to an unbalanced power injection by the converter. The unbalanced power injection causes double-fundamental frequency oscillations in the power that may propagate to the dc-link of the converter yielding voltage oscillations. An accurate model of these oscillations is derived, and a basic design criterion for the dc-link of grid converters is discussed based on the model assumptions. In the following evaluation of current reference generators, the dc-link oscillations serve as a critical indicator for converter utilization.
The converter may accomplish different control objectives during FRT by adjusting the amount of positive and negative sequence currents. Current reference generators calculate the converter current references based on the measured PCC voltages to achieve control objectives like balancing the voltages or mitigating dc-link oscillations. Several current reference generators and grid support schemes are already presented in the literature [52], [16], [26]. However, the voltage support schemes using VOC show critical implementation problems, and the typical current reference generators are not analyzed regarding their voltage support behavior. To fill this gap, the voltage support of the current reference generators is evaluated considering different grid impedance ratios and SCRs. This evaluation reveals a trade-off between limitation of dc-link voltage oscillations, limitation of the maximum phase voltage, and increasing the minimum phase voltage.
The current reference generators significantly change the stability margin depending on the impedance ratio of the lines and SCR of the grid connection. This stability phenomenon is one of three stability related problems of the VOC. The current control causes the second

instability phenomenon, which is analyzed by assessing the stability of the VOC based on PR-controllers under different grid impedance ratios and SCRs. The interaction between current control and PLL dominates the third mechanism, an emerging topic that urgently demands analysis methods to capture the nonlinear dynamics. To fill this gap, a stability analysis framework based on a Lyapunov function is proposed that accurately predicts the Region of Attraction (ROA) of the VOC for generic weak grid scenarios.

6.1 Dual Sequence Current Control for Severe Unbalanced Grid Faults and Weak Grid Conditions

VOC may be implemented with PI-controllers or PR-controllers, but which controller achieves a better control performance? Both control structures are presented in Fig. 6.1. They contain a DSOGI-PLL, frame transformations, the controllers, and a voltage feed-forward. Details on the current controller blocks are shown in section 3.4. For evaluating the controllers, the converter is modeled with a PT1-delay τ_d, representing the sampling delay and SPWM, and a controlled voltage source neglecting switching patterns.

The main difference between the PI and PR based structure is how they use the estimated phase angle of the PLL θ'. For the PI control, the measured phase currents $\mathbf{i}_1$ must be transformed into the dq-frame. In contrast, the reference currents $\mathbf{i}^*_{\mathrm{dq,PLL}}$ for the PR-controller need to be transformed from the dq-frame into the $\alpha\beta$-frame. The PI-controller block or PR-controller block's detailed structures are shown in Fig. 3.12 and 3.13, respectively.

In a first approach, only the positive sequence is considered, and the PLL dynamics are neglected to derive the design parameters and compare both controllers. Both control structures may achieve the same control characteristics, which is proven in theory in [151]. However, this equivalence is only valid for PR-controllers with the coupling terms between the $\alpha\beta$-components as described by:

$$\mathbf{v}^*_{\mathrm{conv},\alpha\beta} = \begin{bmatrix} k_\mathrm{p} + k_\mathrm{r}\frac{s}{s^2+\omega_\mathrm{r}^2} & -k_\mathrm{r}\frac{\omega_\mathrm{r}}{s^2+\omega_\mathrm{r}^2} \\ k_\mathrm{r}\frac{\omega_\mathrm{r}}{s^2+\omega_\mathrm{r}^2} & k_\mathrm{p} + k_\mathrm{r}\frac{s}{s^2+\omega_\mathrm{r}^2} \end{bmatrix} \mathbf{e}_{\alpha\beta} \quad , \tag{6.1}$$

where $\mathbf{v}^*_{\mathrm{conv},\alpha\beta}$ denotes the reference voltage of the converter and $\mathbf{e}_{\alpha\beta}$ is the control error of the current control. Throughout the following analysis, this controller is denoted as decoupled PR-controller. In contrast to this controller definition, the PR-controller is typically implemented without the cross-coupling terms between the α and β-channel. This implementation is

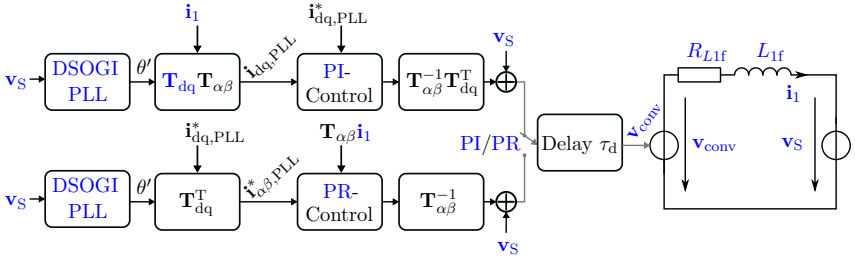


Figure 6.1: VOC using a PI or PR-controller with an averaged converter model and output filter.

equivalent to operate two PR-controllers in parallel, each for the positive and negative sequence, i.e., $\omega_\mathrm{r} = \omega_1$ and $\omega_\mathrm{r} = -\omega_1$, respectively, according to:

$$\mathbf{v}^*_{\mathrm{conv},\alpha\beta} = \frac{1}{2}\left(\begin{bmatrix} k_\mathrm{p} + \frac{k_\mathrm{r} s}{s^2+\omega_1^2} & \frac{-k_\mathrm{r}\omega_1}{s^2+\omega_1^2} \\ \frac{k_\mathrm{r}\omega_1}{s^2+\omega_1^2} & k_\mathrm{p} + \frac{k_\mathrm{r} s}{s^2+\omega_1^2} \end{bmatrix} + \begin{bmatrix} k_\mathrm{p} + \frac{k_\mathrm{r} s}{s^2+\omega_1^2} & \frac{-k_\mathrm{r}(-\omega_1)}{s^2+\omega_1^2} \\ \frac{k_\mathrm{r}(-\omega_1)}{s^2+\omega_1^2} & k_\mathrm{p} + \frac{k_\mathrm{r} s}{s^2+\omega_1^2} \end{bmatrix}\right)\mathbf{e}_{\alpha\beta} \quad (6.2)$$

$$= \begin{bmatrix} k_\mathrm{p} + k_\mathrm{r}\frac{s}{s^2+\omega_\mathrm{r}^2} & 0 \\ 0 & k_\mathrm{p} + k_\mathrm{r}\frac{s}{s^2+\omega_\mathrm{r}^2} \end{bmatrix}\mathbf{e}_{\alpha\beta} \quad . \quad (6.3)$$

Fig. 6.2 and 6.3 show the comparison between the PI-controller, decoupled PR-controller, and standard PR-controller for different control bandwidths or time constants τ_i, respectively. A simulation model according to Fig. 6.1 is used assuming $R_{L1\mathrm{f}}$=0.2 mΩ, $L_{1\mathrm{f}}$=1.2 mH, and $\hat{V}_\mathrm{S}$=325 V. The PI and decoupled PR-controller show identical results in the step response. In contrast, the PR-controller without the cross-coupling experiences a comparably large oscillation related to the missing coupling terms. However, this oscillation is not critical for the dynamics since its magnitude is smaller than 10%. Moreover, a larger control bandwidth can reduce this oscillation significantly, as shown in Fig. 6.3.

There are several design methods for current controls of grid converters. The technical and

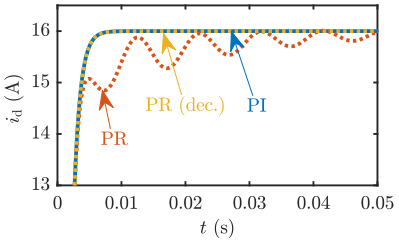


Figure 6.2: Reference step response of i_d to 16 A for the PI, PR, and decoupled PR-controller designed to a time constant of $\tau_\mathrm{i} = 1$ ms.

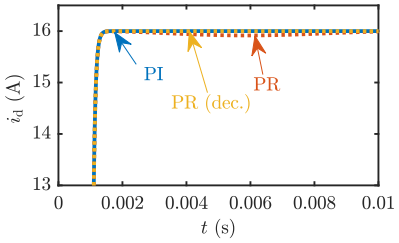


Figure 6.3: Reference step response of i_d to 16 A for the PI, PR, and decoupled PR-controller designed to a time constant of $\tau_\mathrm{i} = 62.5$ μs.

symmetrical optimum are mature methods for the design [130]. The technical optimum relies on pole-zero cancellation with an "optimum" damping factor of $1/\sqrt{2}$. The symmetrical optimum interprets the RL-load as ideal integrator $1/sL$ in the time range of the current control. More sophisticated approaches consider the sampling delay of the converter [152]. For the control modeling, it can be desirable to achieve a PT1 behavior of the closed-loop current control for reference steps, as presented in chapter 5. The control bandwidth of PI-controllers and PR-controllers can be designed with pole-zero cancellation to achieve this behavior [153]. This design procedure relies on the open-loop transfer function assuming an ideal voltage feed-forward according to:

$$G_{\mathrm{ol,PI},i1}(s) = \underbrace{\left(k_\mathrm{p} + k_\mathrm{i}\frac{1}{s}\right)}_{G_\mathrm{PI}} \cdot \underbrace{\frac{1}{R_{L1\mathrm{f}} + \mathrm{s}L_{1\mathrm{f}}}}_{G_{RL}(s)} \cdot \underbrace{\frac{1}{\tau_\mathrm{d}s+1}}_{G_{\mathrm{d,conv}}(s)} = \frac{k_\mathrm{p}}{L_{1\mathrm{f}}\, s} \cdot \frac{\frac{k_\mathrm{i}}{k_\mathrm{p}} + s}{\frac{R_{L1\mathrm{f}}}{L_{1\mathrm{f}}} + s} \cdot \frac{1}{\tau_\mathrm{d}s+1} \quad . \tag{6.4}$$

The converter sampling and modulation delay τ_d must be considered if it has the same order of magnitude as the desired bandwidth. The line impedance components $R_{L1\mathrm{f}}$ and $L_{1\mathrm{f}}$ introduce a PT1 transfer characteristic that should be canceled by the PI-controller by adjusting the parameters k_p and k_i as follows:

$$\frac{k_\mathrm{i}}{k_\mathrm{p}} = \frac{R_{1\mathrm{f}}}{L_{1\mathrm{f}}} \quad , \qquad \tau_i = \frac{L_{1\mathrm{f}}}{k_\mathrm{p}} = \frac{R_{1\mathrm{f}}}{k_\mathrm{i}} \quad . \tag{6.5}$$

The resulting time constant τ_i serves as a design parameter for the control bandwidth. The converter sampling delay and SPWM delay are modeled as a PT1-element with τ_d and lead to the closed-loop transfer function:

$$G_{\mathrm{o,PI},i1}(s) = \frac{1}{\tau_i\, s} \cdot \frac{1}{\tau_\mathrm{d}s+1} \Rightarrow \qquad G_{\mathrm{c,PI},i1}(s) = \frac{1}{\tau_\mathrm{d}\tau_i} \cdot \frac{1}{s^2 + \frac{1}{\tau_\mathrm{d}}\, s + \frac{1}{\tau_\mathrm{d}\tau_i}} \quad . \tag{6.6}$$

This transfer function is a second-order system that only depends on τ_d and τ_i. Hence, the natural frequency $\omega_{\mathrm{c},i1}$ and corresponding damping ratio $\zeta_{\mathrm{c},i1}$ can be designed with τ_i for a given τ_d according to:

$$\omega_{\mathrm{c},i1} = \frac{1}{\sqrt{\tau_\mathrm{d}\tau_i}} \Rightarrow \qquad \zeta_{\mathrm{c},i1} = \frac{1}{2}\sqrt{\frac{\tau_i}{\tau_\mathrm{d}}} \quad . \tag{6.7}$$

The design is tested for different damping ratios $\zeta_{\mathrm{c},i1}$ using a simulation model according to Fig. 6.1 with the parameters $R_{L1\mathrm{f}}$=0.2 mΩ, $L_{1\mathrm{f}}$=1.2 mH, and $\hat{V}_\mathrm{S}$=325 V. The sampling delay is defined to $\tau_\mathrm{d} = 1/f_\mathrm{sw} = 62.5\ \mu$s. The current reference of i_d is changed from 0 A to 16 A to derive the step response. The pole-zero cancellation sufficiently cancels the $R_{1\mathrm{f}}/L_{1\mathrm{f}}$-pole and achieves very similar results for the PI-controller and PR-controller, as shown in Fig. 6.4 and 6.5. Moreover, the step responses indicate that a first-order transfer

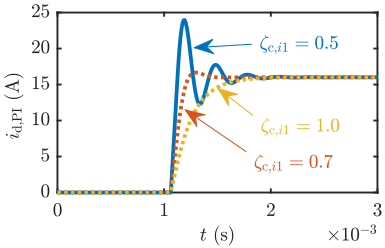


Figure 6.4: Reference step response of i_d to 16 A for the PI-controller designed to different damping factors $\zeta_{\mathrm{c},i1}$ assuming a converter and sampling delay of $\tau_\mathrm{d} = 62.5\ \mu$s.

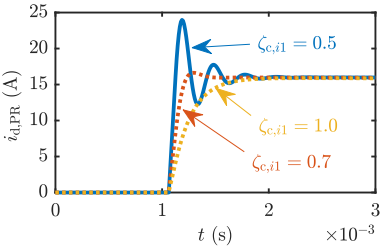


Figure 6.5: Reference step response of i_d to 16 A for the PR-controller designed to different damping factors $\zeta_{\mathrm{c},i1}$ assuming a converter and sampling delay of $\tau_\mathrm{d} = 62.5\ \mu$s.

function G_i could sufficiently approximate the closed-loop current control for damping ratios $\zeta_{\mathrm{c},i1} > 0.7$ according to:

$$G_{\mathrm{c,PI},i1}(s)|_{\zeta_{\mathrm{c},i1}>0.7} \approx G_i(s) = \frac{1}{\tau_i s + 1} \quad . \tag{6.8}$$

The presented controller comparison only considers the positive sequence component. However, converters need a dual sequence controller for the FRT. The PR-controller intrinsically handles the negative sequence. Contrarily, the PI-controller needs a sequence decomposition to control the positive or negative sequence component with zero steady-state error. The structure is presented in Fig. 6.6, where the current $\mathbf{i}_1$ is fed back to the controller using a DSOGI to extract the positive sequence current $\mathbf{i}^+_{1,\alpha\beta}$. This DSOGI introduces a filter in the feedback that must be considered during the control design and can be approximated by the transfer function H_{22} given in 5.16. The transfer function of the converter current $G_{\mathrm{cl,PI},i1}$ can be derived by assuming $\mathbf{i}_{1,\mathrm{dq}} \approx \mathbf{i}^*_{1,\mathrm{dq}}$ and $i_{1,\mathrm{q}} \approx 0$ and is defined as follows:

$$G_{\mathrm{cl,PI},i1}(s) = \frac{i_\mathrm{d}}{i^*_\mathrm{d}} = \frac{G_{\mathrm{ol,PI},i1}(s)}{1 + H_{22}(s) G_{\mathrm{ol,PI},i1}(s)} \quad . \tag{6.9}$$

The DSOGI transfer function H_{22} can be replaced by a PT1 element G_DSOGI with the time-constant $\tau_\mathrm{DSOGI} = 1/4f_1 = 5$ ms, which yields the simplified closed-loop transfer function:

$$G_{\mathrm{cl,PI},i1}(s) \approx \frac{G_{\mathrm{ol,PI},i1}(s)}{1 + G_\mathrm{DSOGI}(s) G_{\mathrm{ol,PI},i1}(s)} \qquad \text{with} \quad G_\mathrm{DSOGI}(s) = \frac{1}{\tau_\mathrm{DSOGI} s + 1} \quad . \tag{6.10}$$

The design of the PI-parameters must be adjusted considering the delay τ_DSOGI. The comparison of the step responses presented in Fig. 6.7 confirms that the PR-controller is much faster than the PI-controller. The PR achieves a rise time of 200 μs, whereas the PI needs 17 ms to reach the reference value. This comparison proves that the sequence

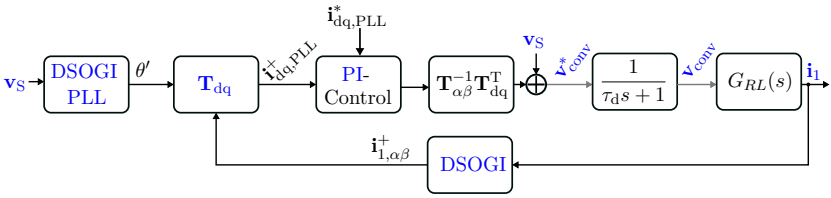


Figure 6.6: Structure of the positive-sequence PI-controller with DSOGI.

decomposition slows down the dual sequence PI-control, whereas the PR-controller is much faster. The same step responses are simulated with the SSM given in 6.10 and compared to the time-domain simulation. Fig. 6.8 shows that the SSM cannot describe the slow oscillations but accurately captures the slope of the current step response.

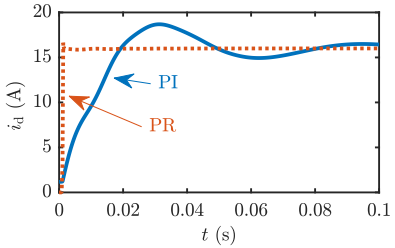


Figure 6.7: Reference step response of i_d to 16 A for the dual-sequence PI and PR-controller assuming a converter and sampling delay of $\tau_\mathrm{d} = 5$ ms and $\tau_\mathrm{d} = 62.5$ μs, respectively.

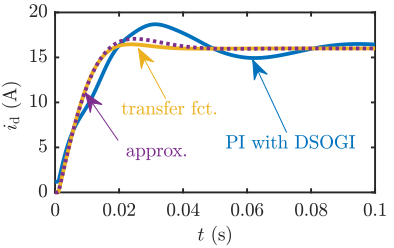


Figure 6.8: Reference step response of i_d to 16 A for the dual-sequence PI-controller simulated with the numerical model, transfer function, and PT1-approximation.

The PR-controller is a fast dual-sequence controller without suffering from the delay of sequence decomposition like the PI-controller. The presented analysis has confirmed this characteristic. Consequently, the PR-controller is identified as a suitable controller and is considered for further analysis.

6.1.1 Voltage Limitation Schemes

The derived current control must be combined with a voltage limitation to achieve a suitable control performance. The voltage limitation typically deteriorates the current control dynamics since it limits the output voltage of the converter, and thus the maximum converter

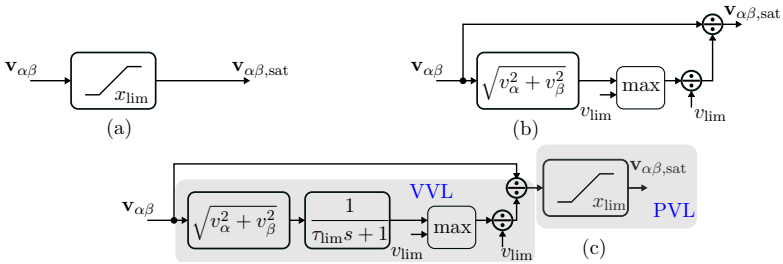


Figure 6.9: Voltage limitation schemes: (a) PVL; (b) VVL; (c) PDVVL.

current slope in the filter inductance $L_{1\mathrm{f}}$. Hence, this section aims to describe a proposed voltage limitation with minimum impact on the controller dynamics.

There are two typical approaches for limiting the voltages: the Peak Voltage Limitation (PVL) and Vector Voltage Limitation (VVL), which are already introduced in section 3.4.3. Moreover, recent approaches propose a limitation of the current reference to guarantee the voltage limits [85], [86]. However, all these structures suffer from the following drawbacks: The PVL leads to harmonics if the limitation is active in steady-state operation. The VVL suffers from poor dynamics since a filter algorithm must extract the fundamental sequence component. These slow dynamics are also a drawback of the current reference limitation, which additionally relies on the measured grid voltages to calculate the maximum current reference to respect the limits of the converter voltage. The main goal of this section is to derive a limitation algorithm that does not suffer from the drawbacks mentioned above.

The structures of the PVL and VVL are presented in Fig. 6.9a and 6.9b, respectively. The PVL simply limits the output voltages of the control to $V_{\mathrm{dc}}/2$. The VVL calculates the magnitudes of the controller output voltages and determines a scaling factor to keep the converter voltage amplitudes within the limit of $V_{\mathrm{dc}}/2$. This VVL conserves the sinusoidal waveform in the steady-state. Both limitation schemes suffer from the previously mentioned drawbacks. Therefore, the Peak and Delayed Vector Voltage Limitation (PDVVL) is proposed, which combines both strategies to achieve the fast dynamic response of the PVL without suffering from the harmonics in steady-state. It limits the output voltage with a saturation block like the PVL and scales the output voltages to the maximum $V_{\mathrm{dc}}/2$ with a delayed magnitude calculation. This limitation guarantees that the VVL is not active during transients, where the maximum output voltage is desirable. In contrast, the PVL is no longer active in the steady-state since the delayed VVL properly limits the fundamental frequency voltages before reaching the saturation block.

The algorithms are tested with a large-signal model of the converter with VOC based on PR-controllers, as presented in Fig. 6.1. The model considers the same parameters as in the previous section and a dc-link voltage of 700 V. A current reference step of 16 A is applied to the controller that triggers the voltage limitation during its transient process. The results are

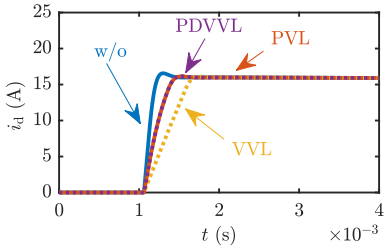


Figure 6.10: Reference step response of i_d for the PR controller with different limitation algorithms. The controller and limitation are designed to $\tau_i = 62.5\ \mu s$, $\tau_{lim} = 6.3$ ms, and to $v_{lim} = 350$ V.

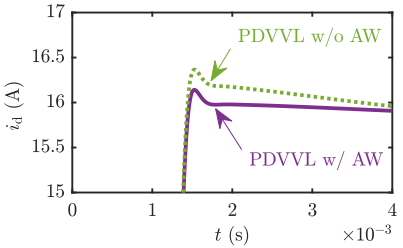


Figure 6.11: Reference step response of i_d for the PR controller highlighting the impact of the anti-windup. The controllers and limitation are designed to $\tau_i = 62.5\ \mu s$, $\tau_{lim} = 6.3$ ms, and $v_{lim} = 350$ V.

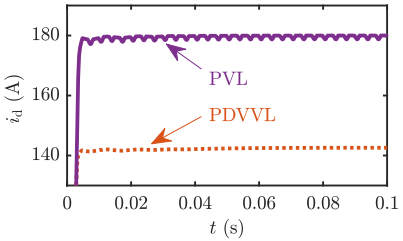


Figure 6.12: Reference step response of i_d with $i_d^* = 180$ A using the PR controller with PVL and PDVVL. The controllers and limitation are adjusted to $\tau_i = 62.5\ \mu s$, $\tau_{lim} = 6.3$ ms, and $v_{lim} = 350$ V.

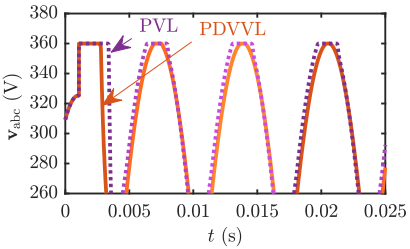


Figure 6.13: Zoomed reference step response of i_d for the PR controller using PVL and PDVVL. The controllers and limitation are adjusted to $\tau_i = 62.5\ \mu s$, $\tau_{lim} = 6.3$ ms, and to $v_{lim} = 350$ V.

shown in Fig. 6.10. The current response without voltage limitation is used as a reference and denoted with w/o. The low-pass filter of the PDVVL is tuned to $\tau_{lim} = 6.3$ ms in this test. The chosen time constant guarantees a settling time of the vector limitation within $T_1 = 20$ ms considering a tolerance band of 3%. All analyzed limitations increase the rise time of the current control. However, the PVL and PDVVL achieve the same rise time, whereas the VVL is much slower. The anti-windup presented in chapter 3 only slightly changes the response characteristics, as shown in Fig. 6.11, and is not analyzed further.

In the steady-state test, a very large current reference of $i_d^* = 180$ A is chosen to operate the converter in steady-state voltage limitation. The results in Fig. 6.12 and 6.13 expose that the PVL causes low-frequency harmonics in the output current by clipping the output voltage peaks but achieves larger currents due to overmodulation. The PDVVL accurately limits the magnitude of the fundamental frequency voltage component without clipping the voltages. Hence, the proposed PDVVL combines the advantages of the PVL and VVL without suffering from their drawbacks. This voltage limitation is used throughout the following analyses.

The overall current control structure with the proposed voltage limitation (PDVVL) is shown

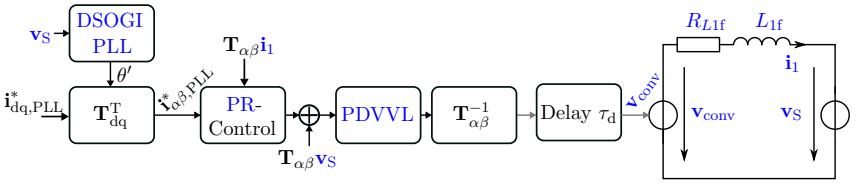


Figure 6.14: Dual sequence current control containing PR-controllers, a DSOGI-PLL and PDVVL.

in Fig 6.14. It tracks the positive and negative sequence current references with short settling times and minor steady-state error. The control performance during severe grid faults is analyzed in the following section.

6.1.2 Evaluation and Modeling of the Dual Sequence Current Control during Severe Voltage Sags and Phase Jumps

The derived dual sequence control (see Fig 6.14) is tested in the worst-case scenarios identified in chapter 5. This previous analysis has identified type A faults as the most critical scenarios. However, the type A fault does not contain negative sequence voltages and thus cannot be a suitable test scenario for the dual sequence control. For the positive and negative sequence, the type E fault with maximum phase jump $\Delta\hat{\theta}$ serves as the most critical scenario. This fault characteristic is achieved by choosing the fault parameter $\underline{Z}_F$=1 pu, which leads to $\Delta\hat{\theta} \approx 0.41$ rad.

The main focus of this section is to test the dual sequence control and analyze how it affects the current step response during unbalanced faults. Therefor, the analytical model in section 5.6 is extended to the negative sequence to describe the fault dynamics of the dual sequence control. In order to obtain the analytical model for the negative sequence, the model of the VOC introduced in section 5.6 is adapted by simply replacing δ with $-\delta$ for the negative sequence, as exemplarily shown in Fig. 6.15 for the reactive currents i_q^+ and i_q^-. Note that δ describes the deviation between the grid phase angle θ and the estimated phase angle of the PLL θ'.

At first, only positive or negative sequence reference currents according to the VDE-AR-N 4110 are applied in response to the type E fault to test the current control and verify the analytical model. The fault voltages are depicted in Fig. 6.16. The numerical model according to Fig 6.14 and the analytical model achieve similar results for the current step responses, as shown in Fig. 6.17 and Fig. 6.18. Note that the current i_{dq+} describes the simulated grid current $\mathbf{i}_1$ transformed with Park's transformation using θ, whereas the current i_{dq-} corresponds to the grid current transformed with $-\theta$. The overall findings are threefold: The results of the numerical model verify the accurate reference tracking of the proposed dual sequence control. Second, approximating the current control with G_i given in 6.8 causes

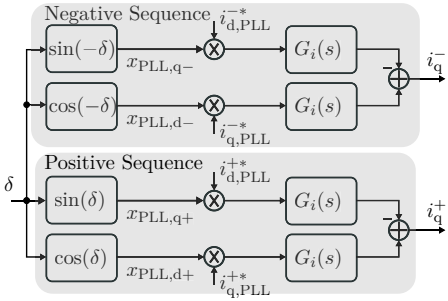


Figure 6.15: Analytical model of the dual sequence current control considering PLL dynamics.

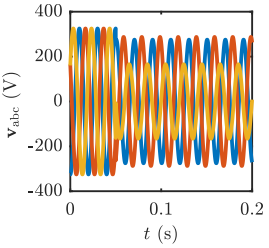


Figure 6.16: Grid voltages during a type E fault with $\underline{Z}_F$=1 pu and $\Delta\hat{\theta} \approx 0.41$ rad.

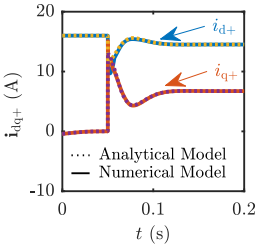


Figure 6.17: Positive sequence current injection during a type E fault with $\underline{Z}_F$=1 pu and $\Delta\hat{\theta} \approx 0.41$ rad.

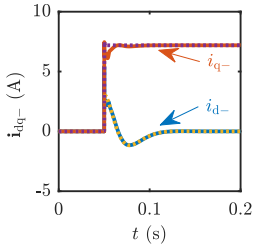


Figure 6.18: Negative sequence current injection during a type E fault with $\underline{Z}_F$=1 pu and $\Delta\hat{\theta} \approx 0.41$ rad.

only minor deviations in the step responses since the PLL dominates the control dynamics. Third, the comparison between the numerical model and analytical model verify the fidelity of the derived analytical model, which accurately describes the behavior of the dual sequence control for grid faults with phase jumps. This proves that the coupling of the PLL with the current control explained in section 5.6 is also valid for the dual sequence control. However, the negative sequence current response to faults is not critically changed by this coupling effect since the operating points typically do not contain an active current component in the negative sequence.

In contrast to the previous analysis, VDE-AR-N 4110 (see Fig. 3.10) typically requires that the converter injects positive and negative sequence currents simultaneously during unbalanced grid faults (see Fig. 3.10) [11]. The step response of current references with positive and negative sequence are difficult to analyze since the coupling of positive and negative sequence currents leads to double fundamental frequency oscillations in the dq-frame. These oscillations make it difficult to determine the settling time of active and reactive currents without decomposing the sequences of the simulated grid currents. The described

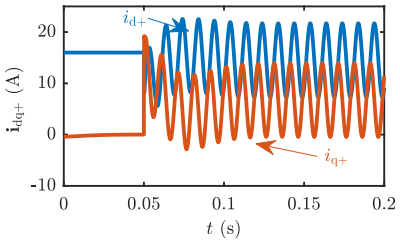


Figure 6.19: Grid currents $\mathbf{i}_{dq+}$ during positive and negative sequence current injection during a type E fault with $\underline{Z}_F$=1 pu and $\Delta\hat{\theta} \approx 0.41$ rad.

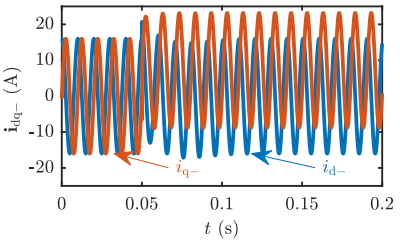


Figure 6.20: Grid currents $\mathbf{i}_{dq-}$ during positive and negative sequence current injection during a type E fault with $\underline{Z}_F$=1 pu and $\Delta\hat{\theta} \approx 0.41$ rad.

characteristic is shown in Fig. 6.19 and Fig. 6.20 for the transformed grid currents i_{dq+} and i_{dq-}, respectively. A sequence decomposition such as the DSOGI may calculate the sequence components of the simulated grid currents $\mathbf{i}_1$ to derive the positive and negative sequence of the grid currents (i^+_{dq} and i^-_{dq}), which can then be used to extract the settling times. However, the sequence decomposition introduces a delay due to the necessary sequence decomposition. Especially for short settling times, this delay dominates the dynamics and leads to significant errors in the settling time compared to the real settling time.

Another way to extract the instantaneous sequence components i^+_{dq} and i^-_{dq} is based on the derived analytical model of the dual-sequence control (see Fig. 6.15) since it only needs the current references and the estimated phase angle error δ to calculate the sequence components of the grid currents.

The step responses of i_{dq+} and i_{dq-} presented in Fig. 6.19 and Fig. 6.20 are analyzed again using either the decoupling of the positive and negative sequence based on the DSOGI or the calculation of the analytical model. The comparison of the step responses of the calculated positive and negative sequence currents is shown in Fig. 6.21. The results indicate that the step responses derived with the analytical model accurately track the positive and negative sequence currents. In contrast, the calculation based on the DSOGI significantly alters the original step responses due to the delay of the DSOGI. The analytical model achieves much more accurate results for the settling time, particularly for the negative sequence current response. Here, the post-processing delay of the sequence decomposition changes the extracted settling time from $t_{set,iq^-} = 0.2$ ms to $t_{set,iq^-} = 10$ ms. Consequently, the proposed analytical model is a potent tool to derive the settling times of the positive and negative sequence currents in simulation.

The presented simulation results prove the low settling time and minor steady-state error of the dual sequence control for grid fault events. However, the control must be tested in a realistic test bench to validate its control characteristics and simulation models finally.

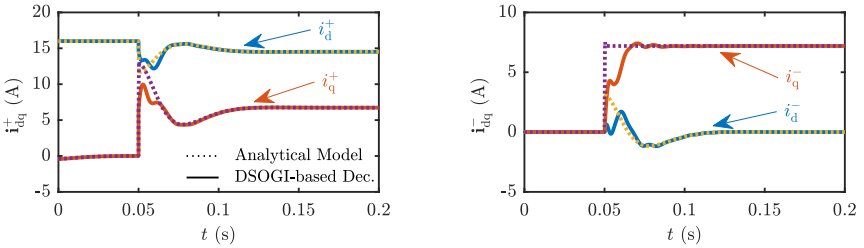


Figure 6.21: Positive and negative sequence grid currents $\mathbf{i}^+_{dq}$ (left) and $\mathbf{i}^-_{dq}$ (right) extracted with DSOGI and analytical model during dual sequence current injection during a type E fault with $\underline{Z}_F$=1 pu and $\Delta\hat{\theta} \approx 0.41$ rad.

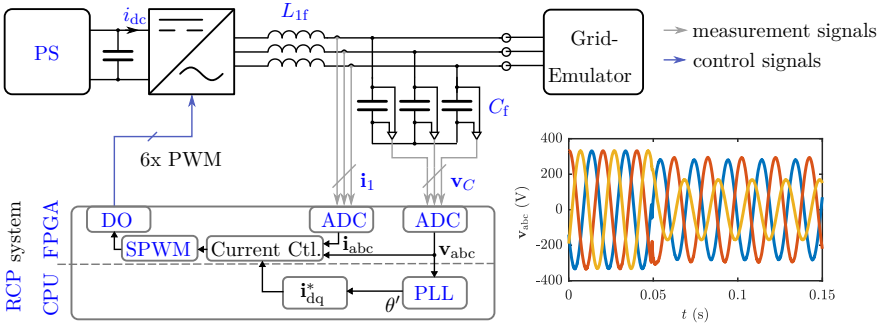


Figure 6.22: Test bench for the VOC with PS, IGBT4 prototype, and grid emulator.

6.1.3 Experimental Validation of Dual Sequence PR-controllers with Voltage Limitation and Anti-Windup

The control performance of the dual sequence control and the simulation models are validated with the IGBT4 test bench presented in section 4.2.1. The converter is connected to the grid emulator. The detailed circuit configuration is shown in Fig. 6.22, and Table 4.2 lists the basic parameters. The converter's switching frequency is 16 kHz, the dc-link voltage 700 V, and the phase voltage magnitude $\hat{V}_{S,1} = 325$ V. Two test cases are considered: First, reference jumps of i_d and i_q validate the current controller performance and models. Second, the control is tested during type A and type E faults to validate the overall control structure considering the interaction of the PR-controllers with the DSOGI-PLL. As an example, Fig. 6.22 shows the phase voltages for the type E fault without zero-sequence voltage.
The SSM contains the closed-loop transfer function of the current control and converter delay neglecting the voltage limitation. In contrast, the LSM contains the derived control structure used in the previous sections (see Fig 6.14).

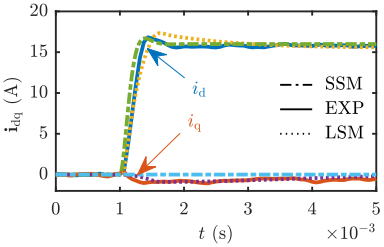


Figure 6.23: Comparison of SSM, LSM, and experimental (EXP) results for a reference step of $i_{\mathrm{d}}^{*} = 16$ A.

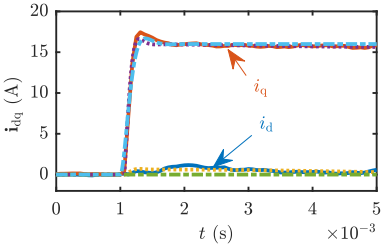


Figure 6.24: Comparison of SSM, LSM, and experimental (EXP) results for a reference step of $i_{\mathrm{q}}^{*} = 16$ A.

The step responses of the currents in Fig. 6.23 and 6.24 show only minor differences between the SSM, LSM, and experiment (EXP). However, the LSM shows slightly larger deviations than the SSM, but the error is below 5% for all values. Moreover, the currents are accurately controlled to the reference values for all analyzed models. The step responses derived with the LSM and test bench show a coupling between dq-components, but the effect is negligible. The step response of the negative sequence currents is not shown here since very similar characteristics are expected.

The reference steps only validate the current controller models and performance without the interaction of the PLL. Therefore, the control is tested again with a type A fault with a phase jump of -42 degrees and magnitude step of 0.5 pu. In contrast to the simulation scenarios, the current references are constant before and during the fault. Moreover, the converter power is measured since the grid currents are not available in the dq-frame of the grid. The results are presented in Fig. 6.25 and show that the LSM accurately describes the time constant and oscillation of the converter power, which is dominated by the PLL dynamics. The comparably large deviation at the beginning of the fault is caused by the slope limitation of the voltage step and phase angle jump of the grid emulator. The test is repeated for a type E fault with a phase jump of 24 degrees (0.41 rad), which is the same scenario used in the previous sections. The results in Fig. 6.26 demonstrate the equivalence between LSM and experiment and thus validate the high fidelity of the model.

The overall findings of this section are threefold: First, the presented dual sequence control enables fast and accurate positive and negative sequence current injection. Second, the proposed voltage limitation guarantees safe limitation, fast dynamics, and lower harmonics in steady-state. Third, the derived analytical model accurately describes the control performance during reference steps and grid faults, which is validated for different grid scenarios and reference steps. Additionally, the model provides a suitable algorithm to extract the positive and negative sequence currents in the simulation without using a post-processing decomposition.

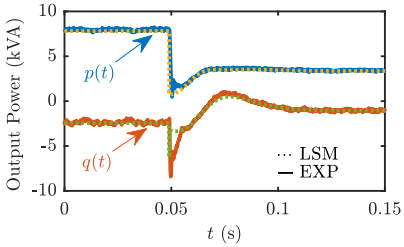


Figure 6.25: Type A fault with $|\underline{Z}_F|$=0.5 pu, r_F=0 pu, and r_S=10 pu with converter current references $\mathbf{i}^*_{dq}$ = [16 5] A.

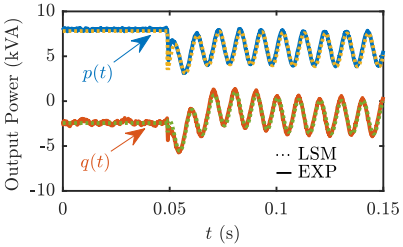


Figure 6.26: Type E fault with $|\underline{Z}_F|$=1 pu, r_F=0 pu, and r_S=10 pu with converter current references $\mathbf{i}^*_{dq}$ = [16 5] A

The presented control scheme enables the converter to accurately inject the current references into the grid even during severe grid faults. In the next step, the impact of different current references on the converter and grid voltage support must be analyzed.

6.2 Impact of Unbalanced Grid Faults on Grid Converters: Model and Analysis of DC-link Oscillations

Since the positive and negative sequence currents can be sufficiently controlled, the impact of FRT operation on converters can be discussed. Unbalanced grid faults may lead to double-fundamental frequency oscillations in the active power that propagate to the dc-link of the converter. Three models must be derived to sufficiently describe this effect. First, the accurate description of the ac-power based on unbalanced grid voltages and converter currents must be derived. Second, the model must describe the relation of ac-currents and voltages on the dc-link currents and voltages, respectively. Third, the effect of the power- or current-oscillations in the dc-link on the dc-link voltage must be modeled considering the dc-link capacitor design.

Particularly for unbalanced systems, the modified $p-q$ theory provides a convenient description of the three-phase instantaneous active power and the instantaneous imaginary power according to [19, pp.82-87]. For simplicity, both power terms are simply denoted by active and imaginary power in the following discussion. The theory divides the power into the active power p_{ac} that comprises any energy flow per time unit between two nodes of a system, and the imaginary power q_{ac} that only propagates between the phases [19, p.80]. The active power is defined as dot product of the phase currents $\mathbf{i}$ and phase voltages $\mathbf{v}$ in the time domain:

$$p_{AC} = \mathbf{v} \cdot \mathbf{i} \quad . \tag{6.11}$$

The norm of the cross product of the components describes the total imaginary power as follows:

$$q_{\mathrm{AC}} = -\left(\mathbf{i} \times \mathbf{v}\right) \cdot \mathbf{1} \quad . \tag{6.12}$$

The description is valid in any reference frame such as abc, $\alpha\beta$, or dq. In the following analysis, only the fundamental frequency components, i.e., positive and negative sequence components, are considered, which leads to the power approximation according to:

$$p_{\mathrm{AC}} \approx \underbrace{\mathbf{v}^{+} \cdot \mathbf{i}^{+} + \mathbf{v}^{-} \cdot \mathbf{i}^{-}}_{\bar{P}_{\mathrm{ac}}} + \underbrace{\mathbf{v}^{+} \cdot \mathbf{i}^{-} + \mathbf{v}^{-} \cdot \mathbf{i}^{+}}_{\tilde{p}_{\mathrm{ac}}} \quad , \tag{6.13}$$

$$q_{\mathrm{AC}} \approx -\left(\underbrace{-\left(\mathbf{i}^{+} \times \mathbf{v}^{+}\right) \cdot \mathbf{1} + \left(\mathbf{i}^{-} \times \mathbf{v}^{-}\right) \cdot \mathbf{1}}_{\bar{Q}_{\mathrm{ac}}} + \underbrace{\left(\mathbf{i}^{-} \times \mathbf{v}^{+}\right) \cdot \mathbf{1} + \left(\mathbf{i}^{+} \times \mathbf{v}^{-}\right) \cdot \mathbf{1}}_{\tilde{q}_{\mathrm{ac}}} \right) \quad . \tag{6.14}$$

In case positive and negative sequence components are apparent, i.e., $\mathbf{i}^{+}$ and $\mathbf{i}^{-}$ or $\mathbf{v}^{+}$ and $\mathbf{v}^{-}$, the power terms contain a dc-component $\bar{P}_{\mathrm{ac}}$ or $\bar{Q}_{\mathrm{ac}}$ and an ac-component $\tilde{p}_{\mathrm{ac}}$ and $\tilde{q}_{\mathrm{ac}}$ oscillating with double fundamental frequency $2\omega_1$. The instantaneous active power of the ac-side propagates to the dc-side of the converter:

$$p_{\mathrm{dc,\,inst}}\left(t\right) = p_{\mathrm{ac,\,inst}}\left(t\right) \quad . \tag{6.15}$$

The dc-side power can be divided into a dc-component and a double-fundamental frequency component as follows:

$$v_{\mathrm{dc}} = V_{\mathrm{o}} + v \quad , \qquad i_{\mathrm{dc}} = I_{\mathrm{o}} + i \quad , \tag{6.16}$$

where V_{o} and I_{o} denote the dc operating point, and v and i contain only alternating terms. These definitions lead to the expression for the active power that focuses on the $2\omega_1$ oscillations caused by unbalanced currents and voltages:

$$\underbrace{V_{\mathrm{o}} I_{\mathrm{o}}}_{\bar{P}_{\mathrm{dc}}} + \underbrace{v I_{\mathrm{o}} + V_{\mathrm{o}} i + v i}_{p_{\mathrm{dc}}} = \underbrace{v_{\alpha}^{+} i_{\alpha}^{+} + v_{\alpha}^{-} i_{\alpha}^{-} + v_{\beta}^{+} i_{\beta}^{+} + v_{\beta}^{-} i_{\beta}^{-}}_{\bar{P}_{\mathrm{ac}}} + \underbrace{v_{\alpha}^{-} i_{\alpha}^{+} + v_{\alpha}^{+} i_{\alpha}^{-} + v_{\beta}^{-} i_{\beta}^{+} + v_{\beta}^{+} i_{\beta}^{-}}_{\tilde{p}_{\mathrm{ac}}} \quad . \tag{6.17}$$

The following description neglects all other frequency components and thus assumes:

$$p_{\mathrm{ac},2\omega 1} \gg p_{\mathrm{ac},\omega 1} + \sum_{k=3}^{\infty} p_{\mathrm{ac},k\omega 1} \quad . \tag{6.18}$$

Finally, the generic expression of the alternating term of the ac-power $p_{ac,2\omega1}$ using the magnitude $P_{\mathrm{ac},2\omega_1}$ and the corresponding angle γ_p can be derived:

$$\underbrace{vI_o + V_o i + vi}_{p_{\mathrm{dc}}} = \underbrace{v_\alpha^- i_\alpha^+ + v_\alpha^+ i_\alpha^- + v_\beta^- i_\beta^+ + v_\beta^+ i_\beta^-}_{p_{\mathrm{ac}}} \approx p_{ac,2\omega1} = P_{\mathrm{ac},2\omega_1} \cos\left(2\omega_1 t + \gamma_p\right) \quad . \tag{6.19}$$

The nonlinear equation in 6.19 has no analytical solution. Therefore, vi and vI_o are set to zero in most publications that focus on the dc-link oscillations during unbalanced faults [17], [18] and assume:

$$vi \ll vI_\mathrm{o} \ll V_\mathrm{o} i \quad . \tag{6.20}$$

The first term of the inequality is typically valid since the alternating parts v and i should be at least one magnitude smaller than the dc operating points. However, the second part is not valid for all converter configurations and is particularly critical for low voltage high-power converters. Consequently, vI_o is not neglected in the following analysis.
The dc-current oscillations are defined as generic oscillations with the frequency $2\omega_1$ and the magnitude $I_{\mathrm{dc},2\omega1}$ similar to the active power $p_{ac,2\omega1}$, which leads to:

$$p_{\mathrm{ac}}(t) \approx p_{\mathrm{ac},2\omega1}(t) = vI_o + V_o i = \left(\frac{1}{C_{\mathrm{dc}}} \int I_{\mathrm{dc},2\omega1} \cos\left(2\omega_1 t\right) \mathrm{d}t\right) I_o + V_o I_{\mathrm{dc},2\omega1} \cos\left(2\omega_1 t\right) . \tag{6.21}$$

This equation can be analytically solved by defining $X_{C,2\omega1} = 1/\omega_1 C_{\mathrm{dc}}$ to obtain $I_{\mathrm{dc},2\omega1}$ according to:

$$I_{\mathrm{dc},2\omega_1} = \frac{P_{\mathrm{ac},2\omega1}}{I_\mathrm{o} X_{C,2\omega1}} \sqrt{\frac{1}{1+\rho^2}} \frac{\cos\left(2\omega_1 t + \gamma_p\right)}{\cos\left(2\omega_1 t + \tan^{-1}(-\rho)\right)} \quad \text{with} \quad \rho = \frac{V_\mathrm{o}}{I_\mathrm{o} X_{C,2\omega1}} \quad . \tag{6.22}$$

Rearranging the equations above and assuming $\cos\left(2\omega_1 t + \gamma_p\right) \approx \cos\left(2\omega_1 t + \tan^{-1}(-\rho)\right)$ yields the expressions for the double fundamental frequency component of the dc-link voltage:

$$V_{\mathrm{dc},2\omega1} = I_{\mathrm{dc},2\omega1} X_{C,2\omega1} = X_{C,2\omega1} P_{\mathrm{ac},2\omega1} \sqrt{\frac{1}{\left(I_\mathrm{o} X_{C,2\omega1}\right)^2 + V_\mathrm{o}^2}} = \frac{P_{\mathrm{ac},2\omega1}}{I_\mathrm{o}} \sqrt{\frac{1}{1+\rho^2}} \quad . \tag{6.23}$$

The expression $1 \ll \rho$ is equivalent to $vI_\mathrm{o} \ll V_\mathrm{o} i$ by considering $X_{C,2\omega1} = v/i$. Setting $\rho \to \infty$ corresponds to $vI_\mathrm{o} \approx 0$ and leads to the conventional expression for the dc-link voltage oscillations:

$$V_{\mathrm{dc},2\omega1} \approx \frac{P_{\mathrm{ac},2\omega1}}{V_\mathrm{o}} X_{C,2\omega1} \quad , \tag{6.24}$$

which verifies the calculations.

The derived model is compared to a numerical model, which considers the current control and a switched converter model, to verify its fidelity. The test scenario is a type G fault with balanced current injection according to Fig. 6.27. The type G fault is chosen because it can

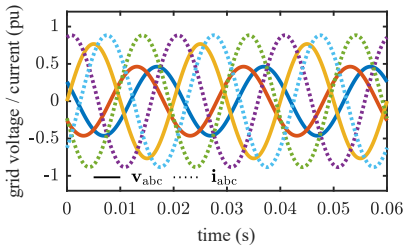


Figure 6.27: Phase voltages and currents during a type G fault considering balanced current injection.

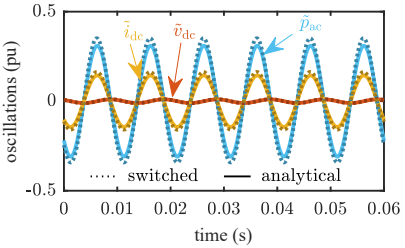


Figure 6.28: Comparison of dc-link current, voltage and active power oscillations between the switched model and the derived analytical model during a type G fault.

be easily emulated with an auto-transformer, which is necessary for validating the models in the next section. Moreover, it has similar voltage and phase angle characteristics as the type E fault. The results of the model comparison are shown in Fig. 6.28 and indicate a high fidelity of the model. The deviations in the range of 10% are caused by the line impedances that slightly shift the operating points of the switched model in comparison to the analytical model.

The dc-link capacitor design has a strong impact on the effect of power oscillations on the dc-link voltage. The derived model can be used to analyze dc-link oscillations considering typical dc-link capacitor designs. The hold-up time criterion is a standard approach to design dc-link capacitors for grid converters based on the stored energy ΔW [154]. The energy is chosen to buffer a required power ΔP over the time T_r assuming that the power input from the generation unit is zero. During this time, the dc-link voltage V_dc should not violate the maximum voltage deviation ΔV. The stored energy in the capacitor is approximated with:

$$\Delta W = \frac{1}{2} C_\mathrm{dc} \left(V_\mathrm{o}^2 - (V_\mathrm{dc} + \Delta V)^2 \right) = C_\mathrm{dc} \left(V_\mathrm{dc} \Delta V + \frac{1}{2} \Delta V^2 \right) \quad . \tag{6.25}$$

This expression is combined with the generic description of the energy to include the design parameters according to:

$$\Delta W = \frac{\Delta P T_\mathrm{r}}{2} \leq C_\mathrm{dc} \left(V_\mathrm{dc} \Delta V + \frac{1}{2} \Delta V^2 \right) \quad . \tag{6.26}$$

Finally, the criterion for the dc-link capacitor C_dc is obtained:

$$C_\mathrm{dc} \geq \frac{\Delta P T_\mathrm{r}}{\Delta V \left(2 V_\mathrm{dc} + \Delta V \right)} \quad . \tag{6.27}$$

The hold-up time design parameter can be directly used to verify the assumption $vI_\mathrm{o} \ll V_\mathrm{o}i$. Substituting the design rule for C_dc in 6.23 and considering normalized quantities $\Delta p = \Delta P/(V_\mathrm{dc}I_\mathrm{o})$ and $\Delta v = \Delta V/V_\mathrm{dc}$ yields:

$$vI_\mathrm{o} \ll V_\mathrm{o}i \qquad \Leftrightarrow \left(\frac{2\omega_1 T_\mathrm{r}}{2\Delta v + \Delta v^2}\Delta p\right)^2 \gg 1 \quad . \tag{6.28}$$

The description links the design rule for the dc-link capacitor with the assumption to simplify the calculation of $V_{\mathrm{dc},2\omega 1}$. This makes it possible to decide based on T_r, Δv, and Δp if the exact relation of $V_{\mathrm{dc},2\omega 1}$ (see 6.23) or the simplified relation (see 6.24) should be used for determining $V_{\mathrm{dc},2\omega 1}$.

The section presented a model of the dc-link oscillations, which accurately predicts the impact of the fault voltages and converter currents on the dc-link oscillations. Since the current reference generator define the converter currents dependent on the fault voltages, their impact on the power oscillations is discussed in the next section. Additionally, the experimental validation of the dc-link oscillations using different current generators is presented.

6.3 Dual Sequence Current Reference Calculation Schemes, Voltage Support Schemes, and the Grid Codes

The main goal of converter current control is to provide active and reactive power to the grid. Current reference generators calculate the required currents according to given active and reactive power references using the grid voltage measurements. The current reference generation is straightforward for balanced systems. However, unbalanced systems raise new challenges of current reference calculation and introduce more flexibility for the active and reactive power injection since the power may be provided in positive and negative sequence. Grid codes require positive and negative sequence currents depending on the fault voltage but typically neglect power oscillation constraints and resistive parts of the line impedances.

There are four basic algorithms for current reference generators proposed in the literature [52], [155], [156]. The algorithms aim to achieve specific power or current properties, which are briefly summarized here. The Balanced Positive Sequence Control (BPSC) balances the output currents. It is identical to solely positive sequence current generators and thus suffers from large active and reactive power oscillations at the double fundamental frequency. The Instantaneous Active–Reactive Control (IARC) rejects the active and reactive power oscillations at double fundamental frequency but suffers from low order harmonics.

The Positive- and Negative-Sequence Control (PNSC) and Average Active–Reactive Control (AARC) reject the active or imaginary power oscillations, respectively, for the power references $P^* = 1$ pu and $Q^* = 0$ pu. Notably, this characteristic changes with the power setpoints. For the setpoint $P^* = 0$ pu and $Q^* = 1$ pu, the PNSC rejects the imaginary power oscillations, whereas the AARC rejects active power oscillations. This high sensitivity to the power setpoints is the major drawback of these algorithms. The Flexible Positive and Negative Sequence Control (FPNSC) provides a generic algorithm that includes all these strategies by introducing two parameters to adjust the power characteristics [52, pp.267-269]. A brief discussion on rejecting active and imaginary power oscillations based on this algorithm is given in [52, p.269], and a specific power reference generator to reject the active power oscillations is presented in [16].
In the literature, the current reference generators mentioned above are not analyzed regarding their grid voltage support. Several current reference generators predominantly support the grid voltages during unbalanced faults by increasing the voltage in the faulty phases as close as possible to the tolerance band of the normal operation. Additionally, they prevent the healthy phases from exceeding the maximum permissible phase voltage [26]. However, these algorithms, which are denoted as Voltage Support Schemes (VSSs), critically depend on the SCR and rely on a line impedance estimation. These implementation problems make them critically sensitive to grid parameter variations.

Converter current limitation may deteriorate the grid voltage support capability because the converter typically injects its maximum current during deep voltage sags. Most current limitation algorithms limit the reference currents to guarantee the maximum converter current [16], [23] [85]. However, this approach critically depends on the current reference generator or VSS and sequence decomposition. Therefore, a straightforward current limitation is proposed that conserves the voltage and current characteristics and thus the characteristics of power oscillations.

The rest of this section is organized as follows: in the first section, two reference generators are derived from the FPNSC that reject the active and reactive power oscillations independent of the power reference setpoint. Then, a dual sequence Vector Current Limitation (VCL) is proposed that conserves the power oscillation properties of the current reference generators. In the third section, the voltage support strategies are presented that guarantee optimum voltage recovery, and the impact of the line impedance estimation on the support characteristics is discussed. Finally, the current reference generators are compared considering maximum power oscillations, voltage support, and stability.

6.3.1 Rejection of Power Oscillations Considering the Current Limitation

A current reference generator to reject power oscillation is proposed in [16]. However, in the following section, current reference generators based on the Flexible Positive and Negative Sequence Controls (FPNSCs) are derived to reject active or reactive power oscillations. The FPNSC defines two parameters, i.e., k_p and k_q, for separation of active and reactive currents in positive and negative sequence [23]. The power references P^* and Q^* can be provided in positive and negative sequence by adjusting k_p or k_q in the range of [0...1]. In the extreme cases $k_p = k_q = 1$ and $k_p = k_q = 0$, the converter provides only positive sequence power or negative sequence power, respectively. The active and reactive current references ($\mathbf{i}^*_{p,\mathrm{FPNSC}}$ and $\mathbf{i}^*_{q,\mathrm{FPNSC}}$) are calculated in the $\alpha\beta$-frame with the expressions:

$$\mathbf{i}^*_{p,\mathrm{FPNSC}} = P^* \left(\frac{k_p}{|\mathbf{v}^+|^2}\mathbf{v}^+ + \frac{1-k_p}{|\mathbf{v}^-|^2}\mathbf{v}^- \right) \quad , \qquad \mathbf{i}^*_{q,\mathrm{FPNSC}} = Q^* \left(\frac{k_q}{|\mathbf{v}^+|^2}\mathbf{v}^+_\perp + \frac{1-k_q}{|\mathbf{v}^-|^2}\mathbf{v}^-_\perp \right) \quad , \tag{6.29}$$

where $\mathbf{v}^+$ and $\mathbf{v}^-$ denote the positive and negative sequence voltage vectors in $\alpha\beta$-frame, respectively; and $\mathbf{v}^+_\perp$ and $\mathbf{v}^-_\perp$ denote the corresponding orthogonal voltages. These components can be determined by a simple matrix operation according to:

$$\mathbf{v}_\perp = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \mathbf{v} \quad . \tag{6.30}$$

Substituting the expressions in 6.29 in the equations for the instantaneous power in 6.11 and 6.12 results in the power oscillations:

$$P_{\mathrm{ac},2\omega 1} = \sqrt{P^{*2}\left[k_p VUF + (1-k_p)\,VUF^{-1}\right]^2 + Q^{*2}\left[k_q VUF - (1-k_q)\,VUF^{-1}\right]^2} \quad , \tag{6.31}$$

$$Q_{\mathrm{ac},2\omega 1} = \sqrt{Q^{*2}\left[k_q VUF + (1-k_q)\,VUF^{-1}\right]^2 + P^{*2}\left[k_p VUF - (1-k_p)\,VUF^{-1}\right]^2}. \tag{6.32}$$

With the expressions in 6.31, the parameters k_p and k_q can be determined to achieve $P_{\mathrm{ac},2\omega 1} = 0$ as follows:

$$k_p = \frac{|\mathbf{v}^+|^2}{|\mathbf{v}^+|^2 - |\mathbf{v}^-|^2} \quad , \qquad k_q = \frac{|\mathbf{v}^+|^2}{|\mathbf{v}^+|^2 + |\mathbf{v}^-|^2} \quad . \tag{6.33}$$

By inserting these expressions into 6.29, the current reference generator denoted as Zero Active Power Oscillation Control (ZAPOC) is defined according to:

$$\left[\mathbf{i}^*_{p,\mathrm{ZAPOC}}\ \mathbf{i}^*_{q,\mathrm{ZAPOC}}\right]^{\mathrm{T}} = \left[\frac{P^*}{|\mathbf{v}^+|^2 - |\mathbf{v}^-|^2}\left(\mathbf{v}^+ - \mathbf{v}^-\right) \frac{Q^*}{|\mathbf{v}^+|^2 + |\ \mathbf{v}^{-|2}}\left(\mathbf{v}^+_\perp + \mathbf{v}^-_\perp\right) \right]^{\mathrm{T}} \quad . \tag{6.34}$$

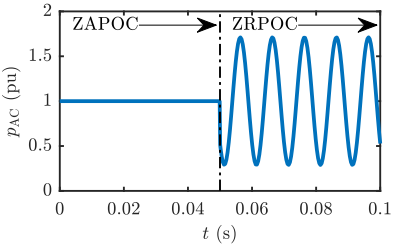


Figure 6.29: Active power injected by the converter using the ZAPOC and ZRPOC during a type E fault with $|\underline{Z}_F|$=0.5 pu.

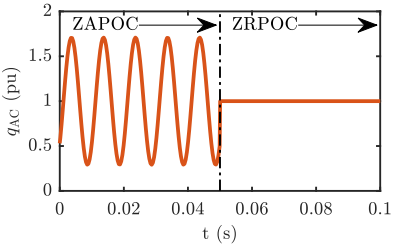


Figure 6.30: Imaginary power injected by the converter using the ZAPOC and ZRPOC during a type E fault with $|\underline{Z}_F|$=0.5 pu.

The same process can be repeated to obtain the current reference generator that guarantees $Q_{\mathrm{ac},2\omega 1} = 0$, which is denoted as Zero Reactive Power Oscillation Control (ZRPOC). The current references are calculated with:

$$\left[\mathbf{i}^*_{p,\,\mathrm{ZRPOC}} \;\; \mathbf{i}^*_{q,\,\mathrm{ZRPOC}}\right]^{\mathrm{T}} = \left[\frac{P^*}{|\mathbf{v}^+|^2 + |\mathbf{v}^-|^2}\left(\mathbf{v}^+ + \mathbf{v}^-\right) \frac{Q^*}{|\mathbf{v}^+|^2 - |\,\mathbf{v}^{-|2}}\left(\mathbf{v}^+_\perp - \mathbf{v}^-_\perp\right)\right]^{\mathrm{T}} . \quad (6.35)$$

The presented current reference strategies are tested in a simulation with a current source, which directly injects the reference currents into the grid. Fig. 6.29 and Fig. 6.30 show the active and imaginary power for a type E fault with $|\underline{Z}_F|$=0.5 pu. At $t = 0.05$ s, the current reference generator is switched from ZAPOC to ZRPOC. For the ZAPOC, the active power oscillations p_{AC} are zero, whereas the imaginary power oscillations q_{AC} have a large amplitude of 0.6 pu. The ZRPOC leads to the exact opposite behavior. These simulation results confirm the expected characteristics of both derived current reference generators.

As discussed before, the current reference generator cannot be sufficiently analyzed in a realistic scenario without considering the current limitation. Therefore, a suitable limitation algorithm must be derived that conserves the aforementioned current reference characteristics, e.g., current balancing or active power oscillation rejection [157]. Several approaches are introduced in the literature to sufficiently limit the maximum converter current. The simplest method proposes a static limitation with predefined ratios of the active and reactive current [87]. The static limitation cannot achieve optimum converter operation and system support for different grid scenarios. More advanced techniques utilize additional virtual impedances and observers with the drawback of increasing complexity [85], [86], [87], [89].
Suitable algorithms to conserve the power characteristics should guarantee that the ratios of positive to negative sequence are constant and the ratio of active to reactive current in positive and negative sequence. This behavior can be achieved by equal scaling of the reference current components. The idea is explained for the reference currents $\mathbf{i}^*$ by using the

active power oscillation definition in 6.17 and combining it with a current limitation factor $k_{i,\mathrm{lim}}$ as follows:

$$\mathbf{i}^*_{\mathrm{lim}} = k_{i,\mathrm{lim}}\mathbf{i}^* \Rightarrow \qquad \tilde{p}_{\mathrm{ac,lim}} = k_{i,\mathrm{lim}}\left(v^-_\alpha i^{*+}_\alpha + v^+_\alpha i^{*-}_\alpha + v^-_\beta i^{*+}_\beta + v^+_\beta i^{*-}_\beta\right) = k_{i,\mathrm{lim}}\tilde{p}_{\mathrm{ac}} \quad . \tag{6.36}$$

This description indicates that the factor $k_{i,\mathrm{lim}}$ only scales the power component $\tilde{p}_{\mathrm{ac}}$. The achieved characteristic is very promising because the scaling conserves the power oscillation rejection presented in 6.34 and 6.35 since $\tilde{p}_{\mathrm{ac,lim}}|_{\tilde{p}_{\mathrm{ac}}=0} = 0\ \forall k_{i,\mathrm{lim}}$ and $\tilde{q}_{\mathrm{ac,lim}}|_{\tilde{q}_{\mathrm{ac}}=0} = 0\ \forall k_{i,\mathrm{lim}}$. The limitation factor $k_{i,\mathrm{lim}}$ can be calculated as ratio of the actual converter current magnitude $|\mathbf{i}^*_{\alpha\beta}|$ and the maximum converter current $\hat{I}_{\mathrm{max}}$. This implementation is similar to the Vector Voltage Limitation (VVL) in section 6.1.1. However, during unbalanced grid faults, the current trajectory may be an ellipse in the $\alpha\beta$-frame so that the magnitude $|\mathbf{i}^*_{\alpha\beta}|$ is not constant. Therefore, the maximum current magnitude can be calculated with $\max|\mathbf{i}^*_{\alpha\beta}| = |\mathbf{i}^*_{\alpha\beta,\mathrm{lim}}| = |\mathbf{i}^{+*}_{\alpha\beta}| + |\mathbf{i}^{-*}_{\alpha\beta}|$. Then, the ellipse can be scaled with

$$k_{i,\mathrm{lim}} = \frac{\hat{I}_{\mathrm{max}}}{|\mathbf{i}^{+*}_{\alpha\beta}| + |\mathbf{i}^{-*}_{\alpha\beta}|} \quad , \tag{6.37}$$

so that $|\mathbf{i}^*_{\alpha\beta}|$ never exceeds $\hat{I}_{\mathrm{max}}$ and $|\mathbf{i}^*_{\alpha\beta,\mathrm{lim}}| = \hat{I}_{\mathrm{max}}$. The final limitation scheme is presented in Fig. 6.31. The structure is identical to the PDVVL (see 6.1.1) but contains the magnitude calculation of $|\mathbf{i}^*_{\alpha\beta}|$ based on the sequence decomposition of the DSOGI. Note that the DSOGI adds a delay here so that only the peak current limitation is active during transients and the vector limitation is only active in steady-state. The impact of the limitation on the current trajectory $\mathbf{i}^*_{\alpha\beta}$ in steady-state is depicted in Fig. 6.32a.

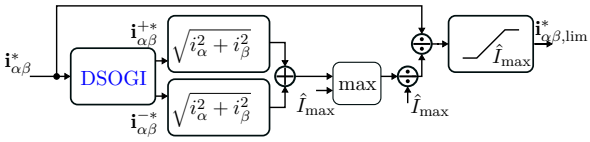


Figure 6.31: Saturation method for converter currents considering the positive and negative sequence.

The reference calculation can be performed in any reference frame. For PR-controllers, it is convenient to calculate the currents directly in the $\alpha\beta$-frame. Unfortunately, the current amplitudes in the α/β-frame cannot accurately describe the maximum phase currents for unbalanced systems with phase shift δ_{e} between positive and negative sequence. This leads to the characteristic that $|\mathbf{i}^{+*}_{\alpha\beta}| + |\mathbf{i}^{-*}_{\alpha\beta}| > \max\left(\hat{I}^*_1,\ \hat{I}^*_2,\ \hat{I}^*_3\right)$. This relation indicates that the limitation based on $|\mathbf{i}^{+*}_{\alpha\beta}| + |\mathbf{i}^{-*}_{\alpha\beta}| < \hat{I}_{\mathrm{max}}$ not exceeds the maximum phase currents but also does not reach the maximum current during unbalanced faults with $\delta_{\mathrm{e}} \neq 0$. This characteristic is

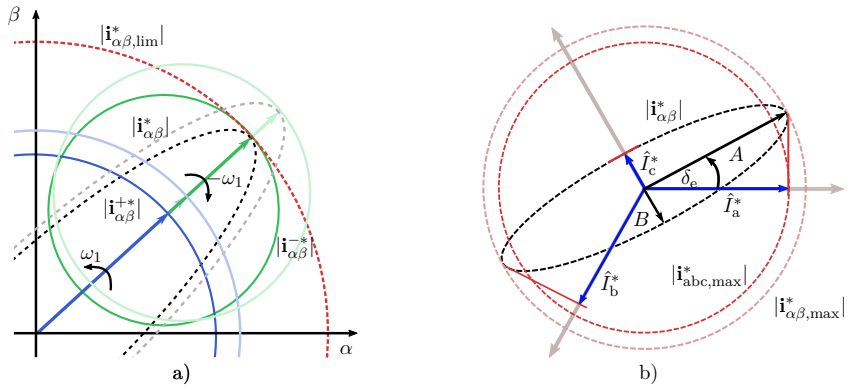


Figure 6.32: a) Proposed limitation with equal scaling of the positive and negative sequence; b) Difference between phase currents in abc-frame and $\alpha\beta$-frame considering the ellipse parameters A, B, and δ_e.

shown in Fig. 6.32b. This figure also introduces the ellipse parameters A, B, and δ_e that are necessary to calculate the maximum phase currents $\hat{I}_j|_{j=[1,2,3]}$ according to:

$$\hat{I}^*_j|_{j=[a,b,c]} = \sqrt{B^2 \cdot \sin^2\left(\delta_e + (j-1)\cdot\frac{4}{3}\pi\right) + A^2 \cdot \cos^2(\delta_e + (j-1)\cdot\frac{4}{3}\pi)} \tag{6.38}$$

considering the phase angles of the positive and negative sequence:

$$\delta_{+1} = \mathrm{atan2}\left(\frac{i^{+*}_\beta}{i^{+*}_\alpha}\right) \qquad \delta_{-1} = \mathrm{atan2}\left(\frac{i^{-*}_\beta}{i^{-*}_\alpha}\right) \Rightarrow \qquad \delta_\mathrm{e} = \frac{\delta_{+1} + \delta_{-1}}{2} \tag{6.39}$$

and the diagonals of the ellipse:

$$A = |\mathbf{i}^{+*}_{\alpha\beta}| + |\mathbf{i}^{-*}_{\alpha\beta}| \qquad B = |\mathbf{i}^{+*}_{\alpha\beta}| - |\mathbf{i}^{-*}_{\alpha\beta}| \quad . \tag{6.40}$$

With these expressions, the limitation factor $k_{i,\mathrm{lim}}$ can be directly calculated according to:

$$k_{i,\mathrm{lim}} = \hat{I}_\mathrm{max} / \max\left(\hat{I}^*_a \;\hat{I}^*_b \;\hat{I}^*_c\right) \quad . \tag{6.41}$$

In combination with the current reference generators, the proposed limitation is simulated during different type G faults with varying sag depths or VUF, respectively. The power references are set to $P^* = .5$ pu and $Q^* = .5$ pu, and the maximum current to $\hat{I}_\mathrm{max} = 1$ pu. The simulation results in Fig. 6.33 confirm that the current magnitudes are sufficiently limited. However, the current magnitudes of the limitation scheme in $\alpha\beta$-frame significantly differ from the limitation in abc-frame. Particularly, the AARC, PNSC, and ZAPOC show

significant deviations in the maximum phase currents between both limitation schemes. In the worst case, the ZAPOC injects 13% less current with the limitation in the $\alpha\beta$-frame than in abc-frame. This current deviation is not acceptable for optimum grid support. The ZRPOC and BPSC do not differ since $\delta_e = 0$ for both strategies. Consequently, the $\alpha\beta$-amplitudes correspond to the abc-frame amplitudes.
Once the currents are sufficiently limited, the impact of the current limitation on the active power oscillations can be analyzed. Fig. 6.34 shows the active power oscillations during the same type G faults as before. The results confirm that the current limitation scales $P_{\mathrm{ac},2\omega1}$. The ZAPOC shows identical results with and without limitation and completely rejects the active power oscillation. In contrast, the ZRPOC and PNSC cause the largest active power oscillations. This characteristic verifies the analysis in 6.36.

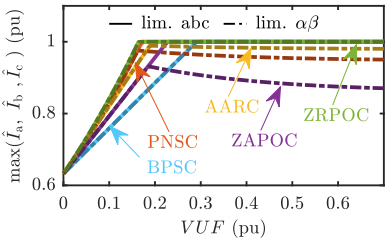


Figure 6.33: Comparison of the current limitation in the abc-frame and $\alpha\beta$-frame using different current reference generators during type G faults with different VUF. This plot highlights the deviation between the phase current amplitudes and amplitudes in $\alpha\beta$-frame.

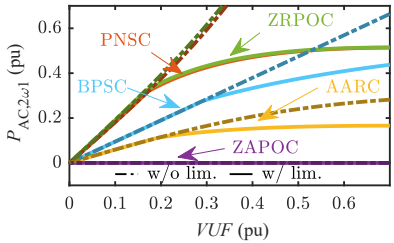


Figure 6.34: Impact of the current limitation on the active power oscillation amplitude $P_{\mathrm{ac},2\omega1}$ using different current reference generators during type G faults with different VUF.

The ZAPOC shows promising results for rejecting active power oscillations. The proposed limitation scheme also enables the converter to reject the power oscillations during current limitation. Moreover, the limitation strategy does not deteriorate the dynamics since it does not decompose the sequences like solutions from the literature [16], [23], [85]. The performance of the current generators with limitation and the dc-link models are validated in the following part.

6.3.2 Validation of the Control Characteristics and DC-Link Oscillations

The current reference generators with limitation are tested with the same experimental setup as the dynamic responses, as shown in Fig. 6.22. Additionally, the setup contains a

dc-link current measurement to validate the impact of active power oscillations at $2\omega_1$ on the dc-link. Moreover, a step transformer is used to emulate a two-phase fault that corresponds to a type G fault since the zero sequence component does not affect the converter terminal voltages. The sag depth is changed in the range of VUF=0-0.7 pu, and the power references are $P^* = 1$ pu and $Q^* = 0$ pu. The active power oscillations, imaginary power oscillations, and dc-link currents are evaluated by performing an FFT and comparing the $2\omega_1$ components to LSM simulation results. The LSM contains the derived control structure and an averaged converter model according to Fig. 6.14. The current reference generators are implemented with a *MATLAB* function, which is used in the simulation and RCP system of the test-bench. The results for the power oscillations of the BPSC, AARC, PNSC, ZAPOC, and ZRPOC schemes are shown in Fig. 6.35 and 6.36. The LSM and experimental results differ significantly but the basic power oscillation properties of the current reference generators are confirmed. The ZAPOC leads to zero active power oscillations $P_{\mathrm{ac},2\omega1}$, whereas the ZRPOC rejects imaginary power oscillations $Q_{\mathrm{ac},2\omega1}$. Due to the setpoint of $P^* = 1$ pu and $Q^* = 0$ pu, the power oscillation rejection can also be achieved with the PNSC and AARC. However, for different power setpoints, the oscillations for these reference generators will change. The largest $P_{\mathrm{ac},2\omega1}$ occurs for the AARC and ZRPOC since they reject $Q_{\mathrm{ac},2\omega1}$. Contrarily, the PNSC and ZAPOC yield the largest $Q_{\mathrm{ac},2\omega1}$ and the BPSC leads to active and imaginary power oscillations.

The impact of the power oscillations on the dc-link is validated by analyzing the $2\omega_1$-oscillations of the dc-link current $I_{\mathrm{dc},2\omega1}$ with an FFT, as shown in Fig. 6.37-6.39. Fig. 6.37 shows the measured currents of the Power Supply to highlight the large oscillations in the dc-link current due to the active power oscillations. Note that the dc-link current i_{dc} is not shown in the time domain due to the large distortions at switching frequency. However, an FFT of i_{dc} in Fig. 6.38 confirms that the ZRPOC sufficiently mitigates the oscillations. Moreover, it is proven that dc-link oscillations at $2\omega_1$ are fully described by the instantaneous active power oscillations, as predicted by the modified *pq*-theory. Consequently, the ZAPOC can sufficiently reject the dc-link oscillations at $2\omega_1$ in any power setpoint. In contrast, the ZRPOC leads to the largest oscillation amplitudes since it rejects the imaginary power oscillations.

The experiment successfully validated the power characteristics of the current reference generators. Moreover, the impact of the power oscillations on the dc-link is proven. The ZAPOC could sufficiently reject the dc-link oscillations during unbalanced faults. However, the limitation of the active power oscillations is only one objective of the converter operation in unbalanced systems. The converter must predominantly support the grid voltage. Hence, the indicators for the converter capability to support the grid voltage are derived in the next section.

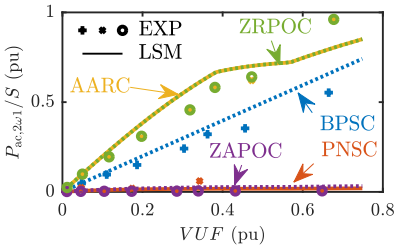


Figure 6.35: Comparison of simulation and experimental results for the active power oscillation amplitude $P_{ac,2\omega1}$ using different current reference generators during type G faults with different VUF.

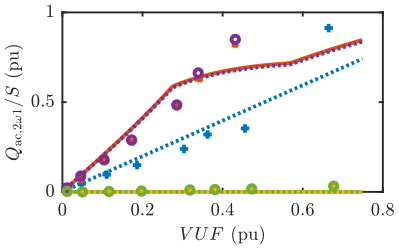


Figure 6.36: Comparison of simulation and experimental results for the imaginary power oscillation amplitude $Q_{ac,2\omega1}$ using different current reference generators during type G faults with different VUF.

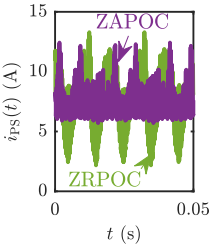


Figure 6.37: Measurement of i_{PS} during type G fault with VUF=0.4 using ZAPOC and ZRPOC.

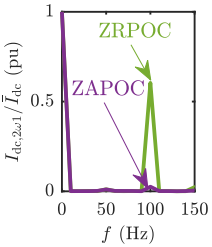


Figure 6.38: FFT of i_{dc} during type G fault with VUF=0.4 to determine $I_{dc,2\omega1}$.

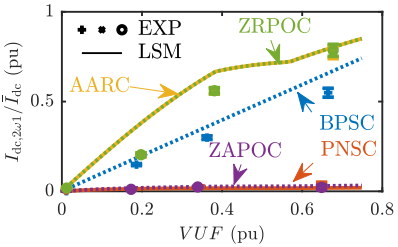


Figure 6.39: Comparison of simulation and experimental results for $I_{dc,2\omega1}$ using different current reference generators during type G faults with different VUF.

6.3.3 Grid support based on Voltage Support Scheme (VSS) and VDE-AR-N 4110

The grid support of converters focuses on voltage support during faults. The converter should try to increase the positive sequence voltage and reduce the unbalance by rejecting the negative sequence voltage. The grid code requires a reactive current in the positive and negative sequence dependent on the positive and negative sequence grid voltages, as already shown in Fig. 3.10 [11]. However, this support strategy has two severe drawbacks. First, the voltage support with reactive current is only applicable for inductive grid, i.e., the strategy might fail for distribution grids with typically significant resistive parts in the line impedance. Second, a large increase in the positive sequence voltage may lead to overvoltages in the healthy phases. Several research contributions focus on developing a more sophisticated VSS to overcome these drawbacks [26], [23]. The basic VSS algorithm is based on [26]. It was extended to inductive-resistive grid impedances by [23]. The basic idea of the VSS is presented in [26] and [23] with changes in the notation. For the sake of completeness, it is

repeated here: first, the maximum and minimum phase voltages are extracted according to:

$$\min\left(V_a, V_b, V_c\right) = \sqrt{\left|\mathbf{v}^+\right|^2 + \left|\mathbf{v}^-\right|^2 + 2\left|\mathbf{v}^+\right|\left|\mathbf{v}^-\right| y} \tag{6.42}$$

$$\max\left(V_a, V_b, V_c\right) = \sqrt{\left|\mathbf{v}^+\right|^2 + \left|\mathbf{v}^-\right|^2 + 2\left|\mathbf{v}^+\right|\left|\mathbf{v}^-\right| x} \tag{6.43}$$

using the angle definitions

$$y = \min\left(\cos(\gamma), \cos\left(\gamma - \frac{2\pi}{3}\right), \cos\left(\gamma + \frac{2\pi}{3}\right)\right) \quad , \tag{6.44}$$

$$x = \max\left(\cos(\gamma), \cos\left(\gamma - \frac{2\pi}{3}\right), \cos\left(\gamma + \frac{2\pi}{3}\right)\right) \text{ with } \gamma = \operatorname{asin}\left(\frac{v_\alpha^+ v_\beta^- + v_\beta^+ v_\alpha^-}{\left|\mathbf{v}^+\right|\left|\mathbf{v}^-\right|}\right) \quad . \tag{6.45}$$

The maximum and minimum reference voltages are then derived according to 6.46, where the desired maximum is slightly changed to sufficiently handle small imbalances, as proved in [26].

$$\max\left\{V_a^*, V_b^*, V_c^*\right\} = \min\left(\overline{\mathcal{V}}, \underline{\mathcal{V}} + \max\left\{V_a, V_b, V_c\right\} - \min\left\{V_a, V_b, V_c\right\}\right) \tag{6.46}$$

$$\min\left\{V_a^*, V_b^*, V_c^*\right\} = \underline{\mathcal{V}} \tag{6.47}$$

$\overline{\mathcal{V}}$ and $\underline{\mathcal{V}}$ indicate the desired maximum and minimum voltages for all three phases and are typically defined in the normal tolerance band of 0.9-1.1 pu or for FRT according to the voltage boundaries [20]. With these defined boundaries, the reference voltages for the positive and negative sequence can be calculated by solving:

$$\left|\mathbf{v}^{+*}\right| = \sqrt{\frac{x\underline{\mathcal{V}}^2 - y\overline{\mathcal{V}}^2 + \sqrt{\left(y\overline{\mathcal{V}}^2 - x\underline{\mathcal{V}}^2\right)^2 - \left(\overline{\mathcal{V}}^2 - \underline{\mathcal{V}}^2\right)^2}}{2(x-y)}} \quad , \tag{6.48}$$

$$\left|\mathbf{v}^{-*}\right| = \sqrt{\frac{x\underline{\mathcal{V}}^2 - y\overline{\mathcal{V}}^2 - \sqrt{\left(y\overline{\mathcal{V}}^2 - x\underline{\mathcal{V}}^2\right)^2 - \left(\overline{\mathcal{V}}^2 - \underline{\mathcal{V}}^2\right)^2}}{2(x-y)}} \quad . \tag{6.49}$$

Finally, the reference currents are obtained using the estimated line and fault impedances R and X, and the voltage $\mathbf{v}_\mathrm{S}$:

$$\begin{aligned} \left|\mathbf{i}_{p,\mathrm{VSS}}^*\right| &= \tfrac{R}{X^2+R^2}\left(\left|\mathbf{v}^{+*}\right| - \left|\mathbf{v}_\mathrm{S}^+\right| + \left|\mathbf{v}^{-*}\right| - \left|\mathbf{v}_\mathrm{S}^-\right|\right) \quad , \\ \left|\mathbf{i}_{q,\mathrm{VSS}}^*\right| &= \tfrac{X}{X^2+R^2}\left(\left|\mathbf{v}^{+*}\right| - \left|\mathbf{v}_\mathrm{S}^+\right| - \left|\mathbf{v}^{-*}\right| + \left|\mathbf{v}_\mathrm{S}^-\right|\right) \end{aligned} \quad . \tag{6.50}$$

The main drawback is the uncertain impedance values that deteriorate the voltage estimation and current references. This problem is not discussed in the literature [26], [28], and [20], but

is analyzed in the following. Therefore, the impedance terms of 6.50 can be rearranged by defining the impedance ratio $r_S = X/R$, which leads to:

$$\frac{R}{X^2+R^2} = \frac{1}{X}\cdot\frac{r_S}{1+r_S^2}; \qquad \frac{X}{X^2+R^2} = \frac{1}{X}\cdot\frac{r_S^2}{1+r_S^2} \quad . \tag{6.51}$$

This derivation indicates that the impedance magnitude, i.e., X, scales the current references $\left|\mathbf{i}^*_{p,\mathrm{VSS}}\right|$ and $\left|\mathbf{i}^*_{q,\mathrm{VSS}}\right|$ given in 6.50. Since the reference current cannot be reached in most applications (the maximum converter current is too small), this scaling is not critical. Hence, the impedance ratio dominates the impact of the line impedance on the VSS. For most grid types, this ratio is well known as summarized in Table 3.1. Consequently, the grid voltage estimation is more critical for the implementation of the VSS than the line impedance estimation. Unfortunately, the algorithm only determines the magnitudes of the reference currents (see 6.50) and thus is an RMS-based algorithm, which typically suffers from slow dynamics. Due to these critical problems, the following evaluation only considers the VSS to assess the grid voltage support capability of the current reference generators.

6.4 Evaluation of Dual Sequence Power Reference Schemes during Fault Ride-Through

The presented current reference generators are often analyzed regarding their maximum current injection and power oscillation characteristics [52], [16], [85]. However, the grid support capability is not part of these contributions. Publications that deal with voltage support mainly focus on the VSS and analyze the voltage characteristics during single-phase faults [26], [23], [20]. In [28], the grid support goal is combined with the mitigation of active power oscillations. This contribution utilizes the VSS that is not applicable due to the drawbacks mentioned in the previous section. Moreover, none of these contributions discusses the stability of the current reference generators. In this section, the different current reference strategies are evaluated regarding their converter utilization and optimum grid support using the VSS as reference. The grid scenarios are type C and type E faults to show the difference between single-phase faults and two-phase faults. The stability margin of the different algorithms based on the minimum SCR is identified for the same fault scenarios to include an indicator for the stability into the evaluation.

The VSS algorithm identifies the optimum control behavior to support the grid voltage. Assuming that the converter cannot reach the current necessary for completely recovering the voltage, the absolute current value is not of interest for the grid support. Based on the VSS in 6.50, the voltage support relies on two important criteria: first, the positive sequence voltage should be increased considering the maximum voltage of the healthy phase. Second,

the negative sequence voltage should be reduced to increase the minimum phase voltage without exceeding the voltage limit with the maximum phase voltage.
The active and reactive power serve as inputs for the current reference generators and are thus adjustable according to the grid impedance ratio. Hence, the current reference generators can achieve the same characteristic as the VSS. However, the ratio of the positive and negative sequence current is fixed by the applied algorithm, e.g. ZAPOC, or k_p and k_q for the FPNSC. Thus, their overall voltage support characteristics must be evaluated and compared to the VSS.
For the evaluation, the model and control depicted in Fig. 6.14 are extended with the current reference generators and a weak grid scenario with SCR=5 pu. The impedance ratios are chosen according to Table 3.1 with $r_{\mathrm{S,hv}} = 10$, $r_{\mathrm{S,mv}} = 1.2$, and $r_{\mathrm{S,lv}} = 0.129$. The power references are selected according to this impedance ratio to achieve optimum grid support for every strategy. Only for the strategy defined in the VDE standard, the references are chosen according to Fig. 3.10. The active power oscillations $P_{\mathrm{ac},2\omega_1}$, the maximum phase voltage $\hat{V}_{\mathrm{max}}$, and minimum phase voltage $\hat{V}_{\mathrm{min}}$ are the indicators for converter utilization and grid voltage support to identify the best strategy for the different fault types and the predefined scenarios. The results for the high-voltage grid, medium-voltage grid, and low-voltage grid during a type C fault are presented in Fig. 6.40 and 6.41, respectively. The BPSC, PNSC, and ZRPOC suffer from large power oscillations and maximum phase voltages above the nominal voltage in high voltage grids. The ZAPOC and AARC achieve very similar results to the VSS, while the ZAPOC guarantees zero active power oscillations. Considering the low-voltage grid, the AARC behaves like the PNSC in the high-voltage grid and vice-versa. The different power references according to the impedance cause this effect. This sensitivity of these current generators makes them vulnerable to variations in the line impedance ratio. The VDE based algorithm suffers from the same sensitivity and achieves a deficient minimum phase voltage, particularly in the low-voltage and medium-voltage grid. Only the ZAPOC achieves very similar results compared to the VSS in all scenarios without relying on the sensitive grid voltage estimation of the VSS. The results for a type E fault are not presented here and confirm these conclusions.

The SCR is a crucial parameter for grid-following converters and critically affects their stability. The stability mainly depends on the SCR, the impedance ratio, and the applied current reference generator. The current reference generators are tested in fault scenarios considering different SCRs to assess their stability. Before the system gets unstable, the THD in the current rises significantly. To detect the stability boundary, a $\mathrm{THD}_i > 0.05$ pu after 200 ms of the fault initiation for a sampling window of 100 ms serves as an indicator for an insufficient stability. The results in Fig. 6.42 and Fig. 6.43 for a type C and type E fault, respectively, indicate that, particularly high-voltage grids are vulnerable to instability due to low SCRs. Moreover, the power reference generators critically affect stability. The ZAPOC and AARC already show an insufficient stability margin at SCR<5 for the high-voltage grid.

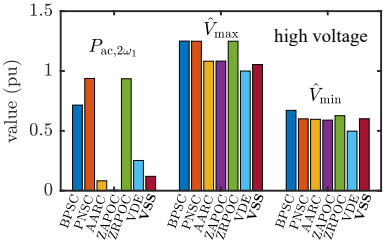


Figure 6.40: Comparison of active power oscillations, the maximum phase voltage, and the minimum phase voltage for different current reference generators for a type C fault with $|\underline{Z}_F|$=0.05 pu, SCR=5 pu, and $r_{S,hv} = 10$.

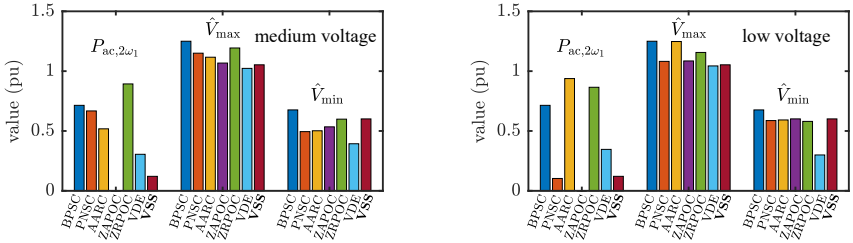


Figure 6.41: Comparison of active power oscillations, the maximum phase voltage, and the minimum phase voltage for different current reference generators for a type C fault with $|\underline{Z}_F|$=0.05 pu, SCR=5 pu, and $r_{S,mv} = 1.2$ (left) or $r_{S,lv} = 0.129$ (right).

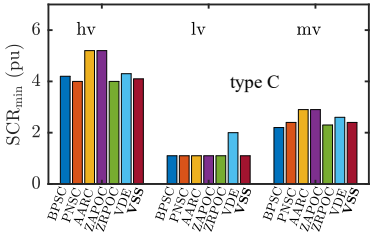


Figure 6.42: Minimum SCR for stable operation with power quality requirement $THD_i < 0.05$ during a type C fault with $|\underline{Z}_F|$=0.05 pu.

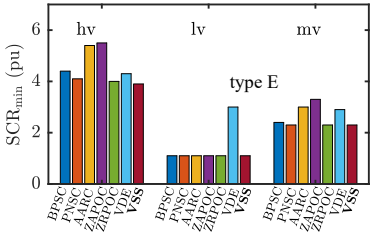


Figure 6.43: Minimum SCR for stable operation with power quality requirement $THD_i < 0.05$ during a type E fault with $|\underline{Z}_F|$=0.05 pu.

In comparison, the ZRPOC and PNSC are stable down to SCRs larger than 4. The fault type has a small impact on the SCR_{min} of the current reference generators.

The evaluation of the current reference generators indicates that the ZAPOC is a suitable strategy to reject active power oscillations considering the maximum and minimum phase voltages. Unfortunately, the stability of the ZAPOC must be carefully proved since it seems

to be vulnerable to instability for low SCRs. The VSS is identified as a suitable reference for the evaluation but is not applicable since it is too sensitive on the grid voltage estimation. The VDE compliant strategy suffers from low maximum and minimum phase voltages due to prioritizing the reactive current.

Weak grid conditions enable inverters to participate actively in the voltage recovery during and after faults. However, the interaction of the injected current with the PCC voltage in weak grids makes the converter control prone to instability mechanisms. As presented, the applied current reference generator has a large impact on the minimum SCR for stable operation. Besides the impact of the current reference generator, two major interactions contribute to instability mechanisms. These mechanisms comprise the interaction of the current control with the grid impedance and the interaction of the PLL with the current control and grid impedance. The next section presents the stability assessment for both mechanisms.

6.5 Methods for Transient Stability Assessment of Dual Sequence Current Controls in Weak Grids

Stability in weak grids is critically affected by the current control, PLL, and current reference generator. This section focuses on the first two controller components. The current control could be unstable due to large line impedances because the impedances mainly define the control plant. Additionally, the interaction between PLLs, the current control, and the line impedance cause transient stability mechanisms. At first, the stability of the current control is analyzed using an LTI-model that accurately represents the PR-controller characteristics. Second, a method based on Lyapunov's functions to assess the transient stability of the current control and PLL is derived.

6.5.1 Stability of PR-Current Controllers in Weak Grids

Linear transfer functions can describe the current control based on PR-controllers if the PLL and current reference generator are neglected. This linear model enables the stability analysis of different weak grid conditions described by the SCR. The basic control structure of the LCL-filter is shown in Fig. 6.44. The complete LCL-filter is considered in this analysis since resonances and filter dynamics become critical in weak grid conditions. The model additionally considers the delay of the measurements denoted with $\tau_{\mathrm{d,m}}$. Rearranging this block-diagram leads to the transfer functions for the grid current $\mathbf{i}_2$ to the current reference $\mathbf{i}_1^*$ and for the grid current $\mathbf{i}_2$ to the grid voltage $\mathbf{v}_\mathrm{S}$. The detailed derivation is shown in appendix A.5, and the closed-loop transfer functions are presented in 6.52 using the transfer

functions defined in A.24. These transfer functions are valid in $\alpha\beta$-frame and can be applied to the α and β component separately.

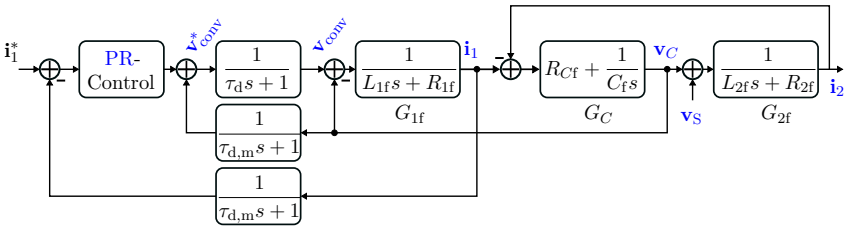


Figure 6.44: Model of the current control for a converter with LCL-filter using PR-controllers.

$$G_{\mathrm{Conv}}(\mathbf{v}_{\mathrm{S}}=0) = \frac{\mathbf{i}_2(s)}{\mathbf{i}_1^*(s)} = \frac{G_{\mathrm{IL}}G_{2\mathrm{f}}}{1-G_{\mathrm{IL}}G_{2\mathrm{f}}G_{\mathrm{FB3}}} \tag{6.52}$$

$$G_{\mathrm{S}}(\mathbf{i}_1^*=0) = \frac{\mathbf{i}_2(s)}{\mathbf{v}_{\mathrm{S}}(s)} = \frac{-G_{2\mathrm{f}}}{1-G_{\mathrm{IL}}G_{2\mathrm{f}}G_{\mathrm{FB3}}} \tag{6.53}$$

The model is verified with time-domain simulations (numerical model) considering an averaged converter model with LCL-filter and current control. The parameters are identical to the hardware test bench presented in section 4.2.1. The SCR is varied by changing the impedances $L_{2\mathrm{f}}$ and $R_{L2\mathrm{f}}$ for different impedance ratios r_{S} according to the low-voltage, medium-voltage, and high-voltage grid definitions presented in Table 3.1. For the analytical model, the transfer functions are applied to the α and β components simultaneously. The results for the step responses in Fig. 6.45 emphasizes the high fidelity of the analytical LTI-model.

The step responses show that the oscillations and overshoot get larger with decreasing SCR, which indicates a decreasing stability margin. To analyze this effect more accurately, Fig. 6.46 presents the eigenvalues of the transfer function G_{Conv}. The findings are twofold: First, the impedance ratio highly affects the stability, and the inductive characteristic of the high-voltage grid makes it more vulnerable to control instability. Second, the SCR deteriorates the stability margin since the critical eigenvalues close to the imaginary axis move towards the right half-plane for decreasing SCR. However, the analyzed system is not unstable even for low SCRs.

The presented LTI-model sufficiently describes the PR-current control since it does not contain critical nonlinear parts. However, the interaction of the current control and PLL cannot be neglected during severe grid faults. Hence, more sophisticated methods are necessary to analyze the stability of this nonlinear system.

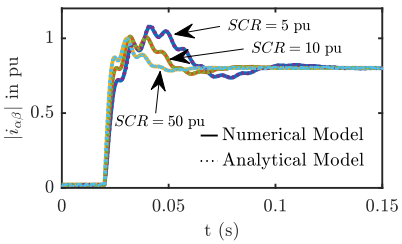


Figure 6.45: Comparison of the current step response of $|\mathbf{i}_{\alpha\beta}|$ between the analytical LTI-model and the numerical model considering different SCRs.

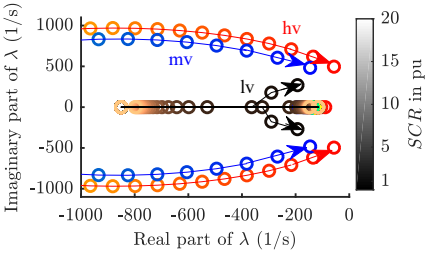


Figure 6.46: Comparison of eigenvalues of the G_{Conv} for different impedance ratios and SCRs.

6.5.2 Method for Transient Stability Assessment based on Lyapunov's Direct Method

The Loss of Synchronization (LOS) caused by the coupling of the PLL with the current control in weak grids attracts much attention in recent research. Several contributions assess the LOS characteristics of the VOC with SRF-PLL and PI-controllers by nonlinear analysis techniques such as the Equal Area Criterion (EAC) and phase portrait [147], [158], [8]. However, these approaches suffer from several drawbacks. First, the EAC is only applicable for plants without proportional gain [159], which is not valid for the analyzed PLL model with current control. Second, the phase portrait is typically only applicable to second-order systems [97], [148]. Additionally, it is based on the manifold in the state-space and therefore relies on ODE-solvers such as standard numerical models. Hence, analytical methods based on the system equations are still demanded [8]. Lyapunov's direct method is a powerful technique to fill this gap.

The following section presents a Lyapunov function for VOC with SRF-PLL in weak grids considering resistive or inductive line impedances. To the best of the author's knowledge, this function was not derived before. Based on this Lyapunov function, an estimate for the Region of Attraction (ROA) can be extracted, which can be used to derive design criteria for the PLLs or identify critical grid scenarios.

The equivalent circuit of the VOC with an averaged converter model and PLL in the dq-frame is shown in Fig. 6.47. Due to the weak grid connection, the converter current $\mathbf{i}^*_{\text{dq,PLL}}$ influences the PCC voltages $v_{\text{d,PCC}}$ and $v_{\text{q,PCC}}$ according to:

$$\begin{aligned} v_{\text{d,PCC}} &= -\omega_1(t) L_{\text{S}} i^*_{\text{q,PLL}} + R_{\text{S}} i^*_{\text{d,PLL}} + v_{\text{d,S}} \quad , \\ v_{\text{q,PCC}} &= \omega_1(t) L_{\text{S}} i^*_{\text{d,PLL}} + R_{\text{S}} i^*_{\text{q,PLL}} + v_{\text{q,S}} \quad . \end{aligned} \tag{6.54}$$

The equivalent circuit can be combined with the PLL model, which is also shown in Fig. 6.47.

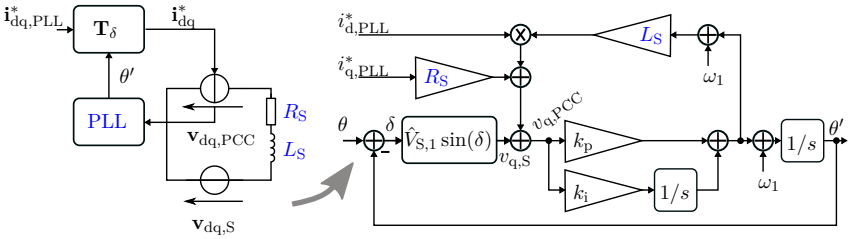


Figure 6.47: Equivalent circuit and model for the interaction of the PLL and current control in weak grids.

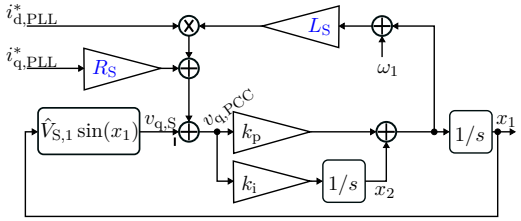


Figure 6.48: Model for the dynamics of the PLL and current control in weak grids.

The low-pass filter of the PLL is neglected to reduce the system order and simplify applying Lyapunov's method. This structure indicates that the converter reference currents change the input voltage of the PLL $v_{\mathrm{q,PCC}}$ and thus influence the dynamics of the grid synchronization. Since the scope of the analysis are the dynamics and not the steady-state, the inputs θ' and ω_1 can be set to zero. Note that $\omega_1 L_\mathrm{S}$ should still be considered to include the impact of L_S on $v_{\mathrm{q,PCC}}$ correctly. These assumptions lead to the dynamic model shown in Fig. 6.48. This model can still describe steps in the grid phase angle θ' by changing the initial condition of x_1, which corresponds to δ. The derived dynamic model, presented in Fig. 6.48, leads to the nonlinear state-space description:

$$\dot{\mathbf{X}} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \frac{1}{1 - k_\mathrm{p} L_\mathrm{S} i^*_{\mathrm{d,PLL}}} \begin{bmatrix} x_2 + k_\mathrm{p}\omega_1 L_\mathrm{S} i^*_{\mathrm{d,PLL}} + k_\mathrm{p} R_\mathrm{S} i^*_{\mathrm{q,PLL}} - k_\mathrm{p}\hat{V}_{\mathrm{S},1}\sin(x_1) \\ (x_2 + \omega_1)\, k_\mathrm{i} L_\mathrm{S} i^*_{\mathrm{d,PLL}} + k_\mathrm{i} R_\mathrm{S} i^*_{\mathrm{q,PLL}} - k_\mathrm{i}\hat{V}_{\mathrm{S},1}\sin(x_1) \end{bmatrix}. \tag{6.55}$$

With these system equations, the equilibrium points $\mathbf{x}_\mathrm{e}$ can be derived by calculating $\mathbf{x}_\mathrm{e} = \mathbf{x}|_{\dot{\mathbf{X}}=0}$, which yields two different equilibria ($\mathbf{x}_{\mathrm{e}1}$ and $\mathbf{x}_{\mathrm{e}2}$) in the range of $0 < x_1 < \pi$ according to:

$$x_{1,\mathrm{e}1} = \sin^{-1}\left(\frac{\omega L_\mathrm{S} i^*_{\mathrm{d,PLL}} + R_\mathrm{S} i^*_{\mathrm{q,PLL}}}{\hat{V}_{\mathrm{S},1}}\right),\ x_{1,\mathrm{e}2} = \pi - \sin^{-1}\left(\frac{\omega L_\mathrm{S} i^*_{\mathrm{d,PLL}} + R_\mathrm{S} i^*_{\mathrm{q,PLL}}}{\hat{V}_{\mathrm{S},1}}\right), \tag{6.56}$$

and

$$x_{2,\mathrm{e1}} = x_{2,\mathrm{e2}} = 0 \quad . \tag{6.57}$$

These expressions indicate that the equilibria shift with the voltage drop over the grid impedance $\underline{Z}_\mathrm{S}$ and thus depend on the converter reference currents $\mathbf{i}^*_{\mathrm{dq,PLL}}$. The stability properties of these equilibria can be analyzed with the phase portrait, similar to the analysis presented in [146], which is based on the $P-\delta$ diagram of the EAC. For details on this analysis refer to [146]. The equilibrium $x_{1,\mathrm{e1}}$ is stable since the trajectories will converge to this point even after small perturbations. Consequently, $x_{1,\mathrm{e1}}$ is a Stable Equilibrium Point (SEP), which is denoted with $x_{1,\mathrm{SEP}}$. In contrast, $x_{1,\mathrm{e2}}$ is unstable even for small perturbations and thus is called Unstable Equilibrium Point (UEP) ($x_{1,\mathrm{UEP}}$). The UEP may serve as a stability boundary, i.e., if x_1 exceeds this value, the system becomes unstable. Unfortunately, this analysis method cannot describe the dynamics of transient stability phenomena.
The dynamics significantly depend on the PLL design parameters. Tuning this PLL structure is straightforward since a second-order system accurately represents it. Hence, the PI-parameters are designed according to the damping ζ and the settling time $t_{\mathrm{set},\delta}$ [70, pp.131-136]. The PI parameter k_p and k_i can be derived as follows:

$$k_\mathrm{p} = \frac{2 \cdot 4.6}{\hat{V}_{\mathrm{S},1} t_{\mathrm{set},\delta}}; \qquad k_\mathrm{i} = \frac{\hat{V}_{\mathrm{S},1} k_\mathrm{p}^2}{4\zeta^2} \quad . \tag{6.58}$$

Now, the model can be verified with a numerical simulation model using these design rules and the grid scenarios introduced in chapter 5. The numerical simulation model contains an averaged converter model, SRF-PLL, and current control. The converter parameters are again set to $\hat{V}_{\mathrm{S},1} = 325$ V and $S = 10$ kVA, and the damping factor ζ is varied between 0.5 and 0.7. Fig. 6.49 and 6.50 present the system trajectories in the state-space (x_1/x_2-plain) for a resistive or inductive weak grid defined by SCR=1.25 and $r_\mathrm{S} = 0.129$ or $r_\mathrm{S} = 10$, respectively. As expected, the numerical model and analytical model show identical results. The simulated trajectories indicate that larger damping leads to decreasing overshoot and thus a larger transient stability margin. In the case of the inductive grid, a LOS can be observed for $\zeta = 0.5$. The results indicate that the resistive grid is more stable than the inductive grid.
The previous analysis based on phase portraits provides no significant benefit of the analytical model compared to the time-domain simulation since the results still depend on ODE-solvers. At this point, Lyapunov's direct method is applied to derive stability criteria based on the system equations. Therefore, the Lyapunov candidate is chosen according to 6.59 since it achieved sufficient results for the PLLs in stiff grids (see section 5.8).

$$V = \int_0^{x_1} \sin(\sigma)\, d\sigma + \frac{1}{2} p x_2^2 = 1 - \cos(x_1) + \frac{1}{2} p x_2^2 \tag{6.59}$$

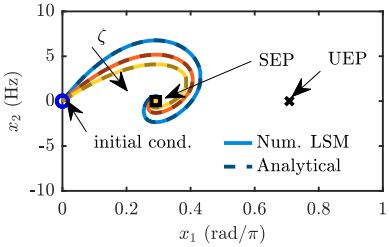


Figure 6.49: Comparison of the state trajectory for the SRF-PLL between the analytical and numerical model considering a weak resistive grid with SCR=1.25 and $r_S = 0.129$ during reactive current injection $\mathbf{i}_{dq} = [0 \;\; 24.6\text{ A}]$. The PLL is tuned to $t_{set,\delta} = 0.1$ s and ζ is varied from 0.5 to 0.7.

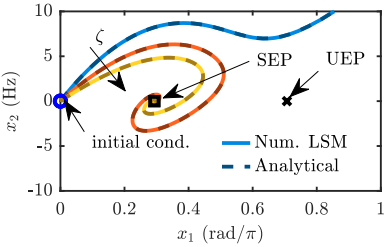


Figure 6.50: Comparison of the state trajectory for the SRF-PLL between the analytical and numerical model considering a weak inductive grid with SCR=1.25 and $r_S = 10$ during active current injection $\mathbf{i}_{dq} = [24.6\text{ A} \;\; 0]$. The PLL is tuned to $t_{set,\delta} = 0.1$ s and ζ is varied from 0.5 to 0.7.

To apply this Lyapunov candidate to the dynamic model, the SEP must be shifted into the origin by adding $x_{1,SEP}$ in the trigonometric term according to:

$$\dot{\mathbf{X}} = \frac{1}{1 - k_p L_S i^*_{d,PLL}} \begin{bmatrix} x_2 + k_p \omega_1 L_S i^*_{d,PLL} + k_p R_S i^*_{q,PLL} - k_p \hat{V}_{S,1} \sin(x_1 + x_{1,SEP}) \\ (x_2 + \omega_1) k_i L_S i^*_{d,PLL} + k_i R_S i^*_{q,PLL} - k_i \hat{V}_{S,1} \sin(x_1 + x_{1,SEP}) \end{bmatrix} . \tag{6.60}$$

Substituting the system equations according to 6.60 in the derivative $\dot{V}$ yields:

$$\begin{aligned} \dot{V} = & \frac{\sin(x_1)}{1 - k_p L_S i^*_{d,PLL}} \left(x_2 + k_p \omega_1 L_S i^*_{d,PLL} + k_p R_S i^*_{q,PLL} - k_p \hat{V}_{S,1} \sin(x_1 + x_{1,SEP}) \right) \\ & + \frac{p x_2}{1 - k_p L_S i^*_{d,PLL}} \left((x_2 + \omega_1) k_i L_S i^*_{d,PLL} + k_i R_S i^*_{q,PLL} - k_i \hat{V}_{S,1} \sin(x_1 + x_{1,SEP}) \right) . \end{aligned} \tag{6.61}$$

This complex expression makes it challenging to derive a parameter p to guarantee $\dot{V} < 0$ in the whole state-space. Therefore, LaSalles invariance principle can be applied that limits the requirements for Lyapunov stability to a bounded region Ω_1 [98]. Theorem VI and VII in [98, pp.58-59] are used in the following analysis and can be summarized as follows: Let Ω_1 be a bounded subset of the state-space that is described by $V(\mathbf{x}) < l$. Let Ω_1 contain the origin $\mathbf{x} = 0$ and Ω_1 fulfills the condition $\dot{V}(\mathbf{x}) < 0$ for all $\mathbf{x} \neq 0$, "then the origin is asymptotically stable, and above all, every solution in Ω_1 tends to the origin as $t \to +\infty$" [98, pp.58-59]. Choosing p according to 6.62 leads to a region that fulfills these requirements. For the details on deriving this expression refer to appendix B.

$$p = \frac{1}{k_i \sqrt{\hat{V}^2_{S,1} - \left(\omega_1 L_s i^*_{d,PLL} + R_s i^*_{q,PLL} \right)^2}} \tag{6.62}$$

With the Lyapunov function in 6.59, the contour $V(\mathbf{x}) = l$, Ω_1, and the ROA can be extracted. The method is tested for a resistive, weak grid considering different SCRs, i.e., 1.25 and 3.

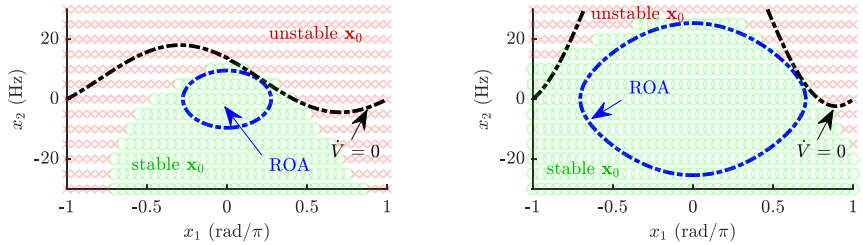


Figure 6.51: Estimated ROA and numerical stability results considering a weak resistive grid with $r_S = 0.129$ and SCR=1.25 (left) or SCR=3 (right) during reactive current injection $\mathbf{i}^*_{dq} = [0 \;\; 24.6]$ A or $\mathbf{i}^*_{dq} = [0 \;\; 10.2]$ A, respectively. The PLL is tuned to $t_{set,\delta} = 0.1$ s and $\zeta = 0.5$.

Fig. 6.51 presents the results for the ROA. Moreover, the numerical simulation is performed for various initial conditions $\mathbf{x}_0$. Varying initial conditions of x_1 represent phase jumps and different x_2 correspond to frequency steps. The stability results for the trajectories starting from the initial conditions are plotted in the same figure. The red cross indicates unstable trajectories. A green circle indicates that the trajectory starting at this initial point will converge to the equilibrium.

The results confirm the theoretical expectation that any trajectory which starts within the ROA will converge to the SEP in the origin. Some trajectories outside the ROA may be stable since the extracted ROA is only an estimate of the real one. Extending the estimated ROA to the real one is an optimization problem of finding an optimum Lyapunov function for the analyzed system. However, the presented method accurately predicts a ROA of the system without solving the differential equations. The comparison between the two SCR scenarios shows that the ROA significantly shrinks for smaller SCRs. Moreover, the analysis shows that the proposed stability criterion according to the UEP in 6.56 is insufficient since dynamics in x_2 tremendously decrease the stable range of x_1.

Unfortunately, the presented Lyapunov function cannot be applied to inductive grids since $\dot{V}$ has an unbounded non-negative region next to the origin. This problem can be solved by slightly changing the Lyapunov candidate according to [160, pp.202-205]:

$$V = \int_0^{x_1} \sin(\sigma) d\sigma + \frac{1}{2} p x_2^2 + \beta x_2 \sin(x_1) \quad , \qquad \beta = -1.7 \cdot p k_i L_S i^*_{d,PLL} \quad . \tag{6.63}$$

The additional parameter β can be chosen to create a negative region of $\dot{V}$ near the origin. However, determining this value is not straightforward and more details on the calculation are given in appendix B. The results presented in Fig. 6.52 indicate a very small ROA for very weak, inductive grids with SCR=1.25, whereas the ROA estimate for the SCR=3 shows a significantly larger stable region. Compared to the resistive grid, the inductive grid is particularly prone to LOS since the stable x_2 range further decreases due to the coupling of the impedance X_S with the angular frequency ω_1.

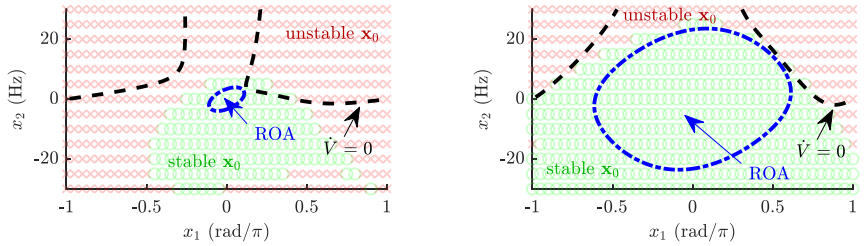


Figure 6.52: Estimated ROA and numerical stability results considering a weak inductive grid with $r_S = 10$ and SCR=1.25 (left) or SCR=3 (right) during active current injection $\mathbf{i}^*_{dq} = [24.6 \;\; 0]$ A or $\mathbf{i}^*_{dq} = [10.2 \;\; 0]$ A, respectively. The PLL is tuned to $t_{set,\delta} = 0.1$ s and $\zeta = 0.5$.

The estimated ROA and stability region in the state-space enable transient stability assessment of two different operational scenarios. First, grid faults with phase jumps may lead to steps of x_1, which could be outside the stable state-space region or ROA and thus would lead to LOS. For example, if a phase jump of $\pi/2$ occurs in the scenario for SCR=1.25 shown in Fig. 6.52, the system will be unstable. Contrarily, for SCR=3 the converter is stable even for faults with large phase jumps of $3\pi/4$.

The second scenario covers reference steps of the converter currents, which shift the equilibrium on the x_1-axis according to 6.56. Particularly interesting is the case where the SEP of the current references $\mathbf{i}^*_{dq} = [0 \;\; 0]$ pu is outside the stable region of the nominal operating point $\mathbf{i}^*_{dq} = [1 \;\; 0]$ pu. That means the converter control will be unstable for current reference steps from 0 pu to the nominal value.

Based on the estimated ROA for a given short-circuit power of the grid, the maximum nominal current $i^*_{d,max}$ for stable operation can be derived. This is done for the weak, inductive grid assuming different damping ratios ζ of the PLL. For better comparability, $i^*_{d,max}$ is normalized with the short circuit current of the grid. The results highlight that $i^*_{d,max}$ can be increased by at least 25% by choosing a larger damping factor for the PLL, as shown in Fig. 6.53. The same analysis is repeated by using a simulation model based on Fig. 6.48 and analyzing the stability of the step response of the currents. The current $i^*_{d,max}$ differs significantly between both models but the increase of the maximum current with the damping factor is in the same range of 25%. These findings confirm that the estimated ROA sufficiently predicts the stability analytically but may lead to conservative results. However, further efforts to improve the estimation of the ROA may increase its accuracy to track the stability boundary.

The presented transient stability framework analytically describes the LOS mechanism using Lyapunov's direct method and Lasalle's invariance principle. The proposed method and Lyapunov function evaluate stability of grid-following converters in weak grids by estimating the ROA. The analysis indicates the insufficient stability prediction of EAC-based approaches

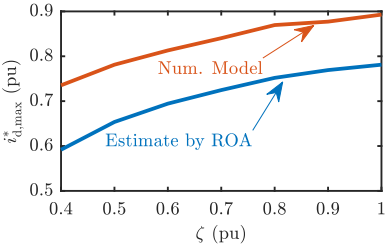


Figure 6.53: Maximum converter current $i^*_{\mathrm{d,max}}$ for stable operation depending on the damping factor of the PLL considering a weak, inductive grid with $r_{\mathrm{S}} = 10$. The time constant of the PLL is tuned to $t_{\mathrm{set},\delta} = 0.1$ s.

and accurately predicts stability considering the dynamics of x_2. Moreover, the ROA enables transient stability assessment of the PLL parameter design and can calculate the maximum converter current for stable operation analytically.

This chapter highlights that grid-following control might suffer from insufficient stability in weak grid conditions predominantly caused by the interaction of PLL with the current control. The current reference generator may further deteriorate the stability. The grid-forming converter control may enhance the control performance and stability in weak grids, which is proved in the following chapter.

7 Grid-forming Converter Control for Fault Ride-Through in Weak Grids

The grid-forming control enables converters to stably operate in very weak grids (SCR<5) or even in islanded mode, where the converter is not connected to the main grid. Such controls typically rely on droop control with cascaded voltage and current control, as presented in section 3.4.2. Designing these controls is complex since the grid scenario defined by the SCR, grid topology and converter count significantly affects stability, dynamics, and stationary control performance [161]. Accordingly, the first part of this chapter presents the controller design for two parallel operating converters that are connected to a weak grid with varying SCR, as shown in Fig. 4.8. The controller design is evaluated based on the step responses of the active power, which are unstable for most of the analyzed controller parameters. Consequently, a virtual impedance is used to sufficiently damp and stabilize the system without changing the droop parameters. The design is verified by estimating linear transfer functions for step responses that are extracted from the simulation and experimental test bench.

Grid-forming controls are typically implemented for balanced three-phase systems but converters should be able to handle unbalanced grid scenarios such as single-phase and two-phase faults during FRT. Therefore, a first approach for compensating unbalances in microgrids has been presented in [162], and a negative sequence droop-control is introduced in [163]. However, none of these research contributions considers unbalanced faults and discuss the problem of oscillating active power. Accordingly, enhanced grid-forming control to handle severe unbalanced grid faults by supporting the grid voltage while sufficiently rejecting active power oscillations is still an open issue. To fill this gap, the current reference generators for the VOC are adopted to grid-forming controls in the second part of this chapter.

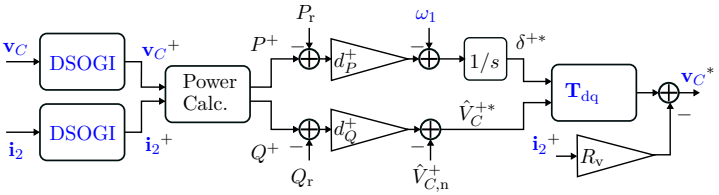


Figure 7.1: Droop control for the positive sequence with power calculation, DSOGI, and virtual impedance damping resistor R_v.

7.1 Design of Positive Sequence Droop-Control with Virtual Impedance

Basic droop control structures typically contain three design parameters, i.e., the proportional gains d_P^+ and d_Q^+, and the low-pass filter frequency $\omega_{\mathrm{f},PQ}$. To sufficiently operate droop control in unbalanced grids, the converter power should be calculated with the positive sequence currents and voltages, which requires to decompose the positive and negative sequence components. This is done by a DSOGI, which provides the capacitor voltage $\mathbf{v}_C{}^+$ and grid current $\mathbf{i}_2{}^+$ to calculate the positive sequence power P^+ and Q^+, as presented in Fig. 7.1. The DSOGI additionally introduces a filter that replaces the conventional LPF G_F introduced in Fig. 3.15. Consequently, only the droop coefficients d_P^+ and d_Q^+ can be designed to achieve the desired steady-state and dynamic performance.

Since the two parameters d_P^+ and d_Q^+ affect both steady-state and dynamics, a virtual impedance may provide an additional design parameter to separately adjust the dynamics. Therefore, R_v serves as virtual resistor in series to the grid impedance and damps the dynamic response, whereas the steady-state effect is compensated by adjusting the power reference P_r by adding $R_\mathrm{v} I_\mathrm{r}$. I_r denotes the setpoint of the converter current. With the additional design parameter R_v, the droop gains can be chosen to achieve a desired steady-state and may be selected according to grid voltages tolerances, as follows:

$$d_P^+ = \frac{\Delta\omega_\mathrm{n}}{P_\mathrm{r}} = \frac{0.2\ \mathrm{Hz} \cdot 2\pi}{P_\mathrm{r}} \quad , \qquad d_Q^+ = \frac{\Delta\hat{V}_{\mathrm{S,n}}^+}{Q_\mathrm{r}} = \frac{0.1\ \hat{V}_{\mathrm{S},1}}{Q_\mathrm{r}} \quad , \tag{7.1}$$

where $\Delta\omega_\mathrm{n}$ is the maximum deviation of the fundamental grid frequency ω_1, and $\Delta\hat{V}_{\mathrm{S,n}}^+$ is the maximum deviation from the nominal grid voltage at the fundamental frequency. Then, the dynamics can be adjusted by selecting R_v, which is done in the following by defining an operational scenario and analyzing the step responses of the active power.

For the operational scenario, the converter setup according to Fig. 4.8 with the parameters of Table 4.1 is used. The active power rating of the converters is selected to P_r=1 kW and the reactive power rating to Q_r=1 kVar. The grid voltage is 400 V at 50 Hz, and the

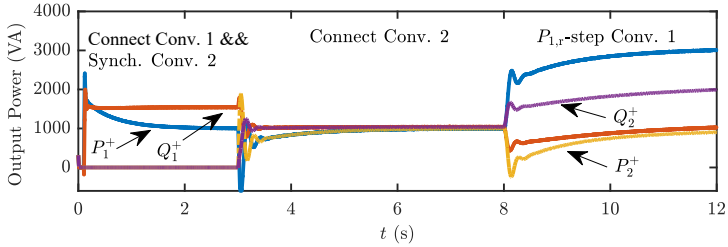


Figure 7.2: Exemplary test scenario of two parallel converters connected to the grid with SCR=3 containing the segments: 1. connection 1st converter and synchronization process of 2nd converter, 2. connection of 2nd converter, and 3. reference step of $P_{1,r}$.

grid-side filter inductances L_{2f} serve as line impedance $\underline{Z}_L$ between converter and PCC. The source impedance $\underline{Z}_S$ is varied to adjust the SCR from very weak (SCR=3) to weak grids (SCR=5) assuming an impedance ratio of $r_S = 10$. The current control is designed according to pole-zero cancellation with $\tau_i = 100\ \mu$s and the voltage control according to the SO with a phase margin of 50 degrees.

A typical operational scenario for parallel converters is shown in Fig. 7.2, consisting of three events: first, a single converter is connected to the grid and the second converter synchronizes on the PCC voltage. Then, the second converter is connected to the PCC followed by an active power step of the first converter as the third event. This scenario contains two critical transient processes: At first, connecting the second converter results in a transient process of the PCC voltage, active power, and reactive power. Second, the active power step causes another transient process. To analyze these transient processes, the time-domain waveforms can be evaluated regarding settling time and overshoot. However, these quantities only indicate stability and cannot sufficiently describe damping and eigenfrequencies of critical modes of oscillation. Therefore, the control system is identified by estimating a linear transfer function to extract the modes that dominate the dynamics, and it is analyzed how control and grid parameters affect them.
There exist several approaches to identify control systems based on the input-output characteristic such as the Prony analysis [164], [165]. In the following investigation, the *MATLAB* function *tfest* described in [166] is used to estimate the linear transfer function. The step response of the active power from the second converter is used as input data, and the count of poles and zeros is increased until sufficient accuracy of 10% for the normalized root-mean-squared error is achieved. Comparing the time-domain waveforms in Fig. 7.3 demonstrates the high accuracy of the estimated transfer function. The results for the step responses demonstrate that larger virtual resistances sufficiently damp the oscillations. This effect gets even more obvious by analyzing the eigenvalues of the estimated transfer functions for varying SCRs and R_v shown in Fig. 7.4. For $R_v \leq 3$ the system is unstable whereas

increasing R_v improves damping of critical poles. The SCR does not significantly affect the critical modes of oscillation. The analysis indicates that $R_v = 5\ \Omega$ provides sufficient damping in the presented scenario, as verified in Fig. 7.3, and thus is chosen for further investigations. One significant advantage of the estimation method is that it can be applied to measurement

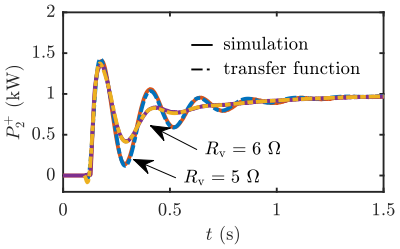


Figure 7.3: Comparison of step responses of the active power of the second converter with $R_v = 5\ \Omega$ and $R_v = 6\ \Omega$ during connection process to the PCC operating in a very weak grid with SCR=3.

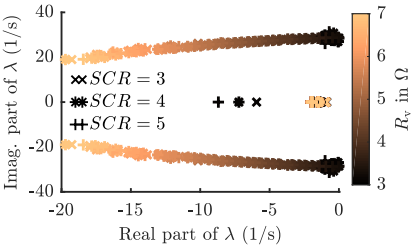


Figure 7.4: Eigenvalues of the active power step response of the second converter with $R_v = 3...6\ \Omega$ during connection process to the PCC operating in a very weak grid to weak grid SCR=3...5.

data in the same way as for simulation results. The corresponding experimental test scenario is performed with the parallel converter test bench presented in Fig. 4.10, where the grid emulator provides the grid voltage, and an inductor with $L_S = 40$ mH and $R_S = 1.3\ \Omega$ serves as $\underline{Z}_L$, which leads to a SCR of 5. The results in Fig. 7.5 and 7.6 compared to Fig. 7.3 and 7.4 highlight the high fidelity of the simulation, even if the measurement has a slightly larger damping of the critical modes of oscillation. Moreover, the experimental results confirm the finding that the virtual impedance R_v sufficiently stabilizes the control dynamics.

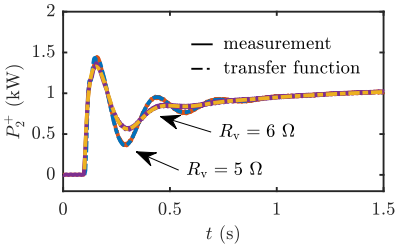


Figure 7.5: Measurement of step responses of the active power of the second converter with $R_v = 5\ \Omega$ and $R_v = 6\ \Omega$ during connection process to the PCC operating in a weak grid with SCR=5.

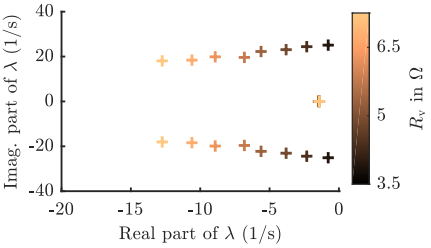


Figure 7.6: Eigenvalues of the measured active power step response of the second converter with $R_v = 3.3\ ...\ 7\ \Omega$ during connection process to the PCC operating in a weak grid with SCR=5.

Once the suitable design parameters are selected for the positive sequence droop in weak and very weak grids, the system achieves a satisfactory performance in the normal operation.

However, the FRT raises further challenges such as properly calculating the negative sequence reference voltage and choosing the maximum converter current. Therefore, the droop control is extended to the negative sequence considering additional power characteristics according to the current reference generators, as described in the previous chapter.

7.2 Droop Control for Unbalanced Operation Scenarios Considering Fault Ride-Through

The droop concept can be directly extended to the negative sequence as proposed in [163]. Therefore, the Thevenin equivalent circuit presented in Fig. 4.4 is assumed for the positive and negative sequence, so that the power can be described as follows:

$$P = \frac{\hat{V}_{\mathrm{S},1}\hat{V}_{C,1}}{|X_\mathrm{S}|}\delta^+ + \frac{\hat{V}_{\mathrm{S},-1}\hat{V}_{C,-1}}{|X_\mathrm{S}|}\delta^- = P^+ + P^- \quad , \tag{7.2}$$

$$Q = \frac{\hat{V}_{\mathrm{S},1}\hat{V}_{C,1} - (\hat{V}_{\mathrm{S},1})^2}{|X_\mathrm{S}|} - \frac{\hat{V}_{\mathrm{S},-1}\hat{V}_{C,-1} - (\hat{V}_{\mathrm{S},-1})^2}{|X_\mathrm{S}|} = Q^+ - Q^- \quad , \tag{7.3}$$

where $\hat{V}_{\mathrm{S},-1}$ denotes the negative sequence of the grid voltage, $\hat{V}_{\mathrm{C},-1}$ is the capacitor voltage in the negative sequence, δ^- is the angle difference between these voltages, and X_S describes the inductive line impedance. These expressions indicate that the droop characteristics according to 3.45 and 3.46 are also valid for the negative sequence. This negative sequence droop control is a potent control for normal operation, i.e., VUF<0.03, and enhances power sharing among the generation units but may not sufficiently recover PCC voltages or reject active power oscillations during faults. Accordingly, the negative sequence droop control must be extended to cover these objectives and to achieve the desired performance for active power oscillations, maximum phase voltages, VUF, and stability.

One major problem of grid-forming controls occurs during limitation of the current. Cascaded controls are prone to controller latch-up and require sophisticated limiting concepts [31]. However, grid-forming controls are mainly applied due to their stability and voltage support in weak grids, and thus the maximum converter current should be properly designed to meet the requirements of the grid scenarios considering the SCR. Assuming that the converter provides the current to completely recover the voltages at the PCC during faults, the maximum converter current $|\mathbf{i}_{2,\max}|$ can be calculated with the rated current $|\mathbf{i}_{2,\mathrm{r}}|$ as follows:

$$|\mathbf{i}_{2,\max}| = SCR|\mathbf{i}_{2,\mathrm{r}}| - \frac{\left|\mathbf{v}_\mathrm{S}^+\right|}{|\underline{Z}_\mathrm{S}|} - \frac{\left|\mathbf{v}_\mathrm{S}^-\right|}{|\underline{Z}_\mathrm{S}|} = SCR|\mathbf{i}_{2,\mathrm{r}}| - \frac{\left|\mathbf{v}_\mathrm{S}^+\right|(1+VUF)}{|\underline{Z}_\mathrm{S}|} \quad . \tag{7.4}$$

The expression shows that the converter must provide an additional grid current depending on the SCR during faults, whereas faults with $\left|\mathbf{v}_\mathrm{S}^+\right| = 0$ demand the largest current. This case corresponds to type A faults with $\underline{Z}_\mathrm{F}$=0 pu. The analysis indicates that the grid-forming

control should be operated in grids with small SCRs since the current rating of the converter gets unnecessarily large for large SCRs. Accordingly, in the following analysis, the control does not limit the converter current since the maximum converter current should be designed considering the maximum SCR to guarantee sufficient grid support.
The grid support strategy is straightforward for the grid-forming converters since they should simply hold the positive sequence voltage in the nominal band while rejecting the negative sequence voltage. This characteristic is achieved by selecting the negative voltage reference $\mathbf{v}_C^- = 0$. From the converter point of view, this operation might be critical due to large active power oscillations. These oscillations are described by the instantaneous power theory according to:

$$\tilde{p}_{\text{ac}} = \mathbf{v}_C^+ \cdot \mathbf{i}_2^- + \mathbf{v}_C^- \cdot \mathbf{i}_2^+ \quad . \tag{7.5}$$

This expression holds also for the converter power by assuming $\mathbf{v}_C \approx \mathbf{v}_{\text{conv}}$ and $\mathbf{i}_2 \approx \mathbf{i}_1$. In the case of $\mathbf{v}_C^- = 0$, $\tilde{p}_{\text{ac}}$ only depends on $\mathbf{i}_2^-$, which is determined by the negative sequence of the grid voltage and line impedance, and is not controlled by the converter.
In order to reject the active power oscillations, the negative sequence voltage $\mathbf{v}_C^-$ must be derived as follows. First, the negative sequence current $\mathbf{i}_2^-$ that sufficiently rejects the active power oscillations can be calculated according to:

$$\tilde{p}_{\text{ac}} = \mathbf{v}_C^+ \cdot \mathbf{i}_2^- + \mathbf{v}_C^- \cdot \mathbf{i}_2^+ = 0 \Rightarrow \qquad \mathbf{i}_2^- = -\frac{\mathbf{v}_C^- \cdot \mathbf{i}_2^+}{\mathbf{v}_C^+} \Rightarrow \qquad \mathbf{i}_2^- = -\frac{\mathbf{v}_C^- \left(\mathbf{v}_C^+ - \mathbf{v}_{\text{S}}^+\right)}{\mathbf{Z}^+ \mathbf{v}_C^+} \quad . \tag{7.6}$$

Second, substituting 7.6 in the expressions for the Thevenin equivalent circuit (see Fig. 4.4) leads to:

$$\mathbf{v}_C^- = \mathbf{Z}^- \cdot \mathbf{i}_2^- + \mathbf{v}_{\text{S}}^- \Rightarrow \qquad \mathbf{v}_C^- = -\mathbf{Z}^- \cdot \frac{\mathbf{v}_C^- \left(\mathbf{v}_C^+ - \mathbf{v}_{\text{S}}^+\right)}{\mathbf{Z}^+ \mathbf{v}_C^+} + \mathbf{v}_{\text{S}}^- \tag{7.7}$$

$$\mathbf{v}_C^- = \frac{\mathbf{v}_C^+}{\left(1 + \mathbf{Z}^- \left(\mathbf{Z}^+\right)^{-1}\right) \mathbf{v}_C^+ - \mathbf{Z}^- \left(\mathbf{Z}^+\right)^{-1} \mathbf{v}_{\text{S}}^+} \mathbf{v}_{\text{S}}^- \text{ with} \qquad \mathbf{Z}^- \left(\mathbf{Z}^+\right)^{-1} = 1, \tag{7.8}$$

whereas

$$\mathbf{Z}^+ = \begin{bmatrix} R_{\text{S}} & -\omega_1 L_{\text{S}} \\ \omega_1 L_{\text{S}} & R_{\text{S}} \end{bmatrix} \text{ and } \mathbf{Z}^- = \begin{bmatrix} R_{\text{S}} & \omega_1 L_{\text{S}} \\ -\omega_1 L_{\text{S}} & R_{\text{S}} \end{bmatrix} \quad . \tag{7.9}$$

These expressions yield the AARC strategy for grid-forming controls according to 7.10. To derive the PNSC strategy to reject oscillations in the imaginary power is similar to the AARC

and is presented in appendix C. The BPSC is obtained by simply choosing $\mathbf{v}_C^- = \mathbf{v}_S^-$ to achieve $\mathbf{i}_2^-$=0.

$$\mathbf{v}_{C,\text{AARC}}^- = \frac{\mathbf{v}_C^+}{2\mathbf{v}_C^+ - \mathbf{v}_S^+}\mathbf{v}_S^- \qquad \mathbf{v}_{C,\text{PNSC}}^- = \frac{\mathbf{v}_C^+}{\mathbf{v}_S^+}\mathbf{v}_S^- \qquad \mathbf{v}_{C,\text{BPSC}}^- = \mathbf{v}_S^- \tag{7.10}$$

The voltage reference values depend on the grid voltage $\mathbf{v}_S$, which is typically not known, and thus must be replaced by $\mathbf{v}_{PCC}$. Using $\mathbf{v}_{PCC}$ for calculating the reference alters the power characteristics, particularly, in very weak grids since $\mathbf{v}_{PCC}$ then highly depends on the converter currents.
The reference schemes are based on instantaneous quantities that could be directly calculated from measured voltages and currents and thus provide time-domain signals. However, for implementing these expressions typically LPFs are necessary to sufficiently prevent coupling with the cascaded voltage control. Therefore, a scaling factor k^- is defined that can be calculated with the magnitudes of the voltages, as exemplarily shown for the AARC:

$$k_{\text{AARC}}^- = \frac{|\mathbf{v}_C^+|}{2|\mathbf{v}_C^+| - |\mathbf{v}_{PCC}^+|} \Rightarrow \qquad \mathbf{v}_{C,\text{AARC}}^- = G_F^- k_{\text{AARC}}^- \mathbf{v}_{PCC}^- \quad . \tag{7.11}$$

k^- is low-pass filtered by G_F^- to achieve the desired decoupling from the cascaded control. The shortcoming of this approach is that the angle information of the positive sequence gets lost and thus, the positive sequence angle difference between $\mathbf{v}_S^+$ and $\mathbf{v}_C^+$ is assumed to be zero, which is only valid for $P^+ = 0$. This assumption is not critical for inductive grids that predominantly demand reactive power for supporting the grid voltage.

Basically, only the grid-forming VSS and AARC are of interest since they are designed to support the grid or reject active power oscillations, respectively. Hence, only these two control schemes are analyzed and compared in detail. The controls are tested in the scenario where two converters operate in parallel connected to a very weak grid with SCR=3 and $r_S = 10$. Two different test cases are selected to evaluate their performance:

- test case 1: two parallel converters during a type C fault with $|\underline{Z}_F|$=0.05 pu,
- test case 2: two parallel converters during a type E fault with $|\underline{Z}_F|$=0.05 pu.

The converter and control parameters are chosen according to the previous section and the LPF for k^- is selected to 20 Hz to achieve sufficient decoupling from the cascaded control loops. The results for test case 1 in Fig. 7.7 and Fig. 7.8 confirm the theoretically derived control objectives. The AARC sufficiently decreases the active power oscillations, whereas the VSS satisfactorily balances the PCC voltages. The active power oscillations are not exactly zero due to the assumptions for implementing the AARC, i.e., $\mathbf{v}_{PCC}^+ = \mathbf{v}_S^+$ and $P^{+*} = 0$. The test case 2 in Fig. 7.9 and 7.10 highlights that the AARC may completely reject the oscillations, and the VSS sufficiently balances the voltages.

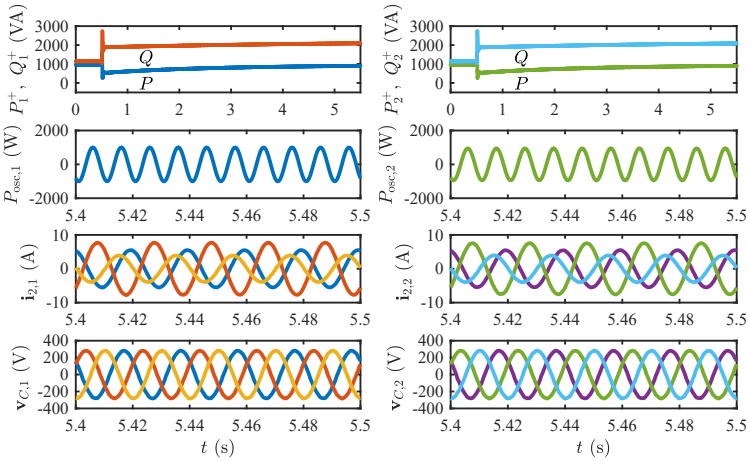


Figure 7.7: Parallel converter operation during test case 1 with SCR=3 and grid-forming VSS.

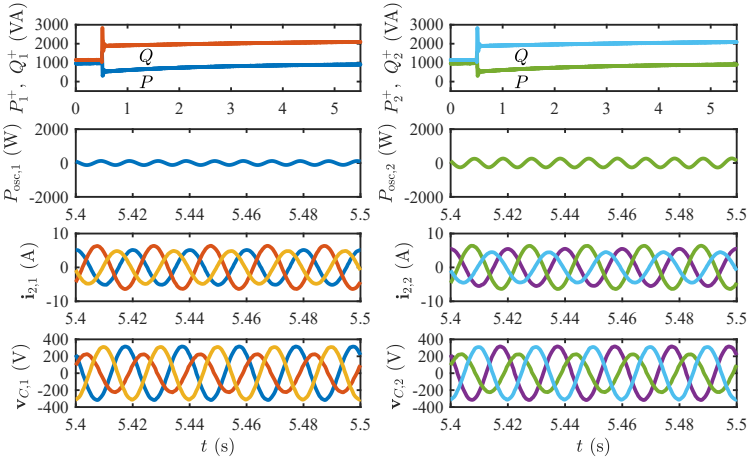


Figure 7.8: Parallel converter operation during test case 1 with SCR=3 and grid-forming AARC.

The time-domain analysis already presented the steady-state and dynamic characteristics. Now, both strategies are compared regarding their performance indicators for supporting grid voltages, reject power oscillations, and demanding large converter currents. As presented in the previous chapter, the critical indicators are $\hat{V}_{\max}$, $P_{\mathrm{ac},2\omega 1}$, $\hat{V}_{\min}/\hat{V}_{\max}$, and $\hat{I}_{\max}$. These are summarized in Table 7.1 for both test cases and confirm the expected characteristics that the AARC reduces active power oscillation $P_{\mathrm{ac},2\omega 1}$ while suffering from large voltage unbalance

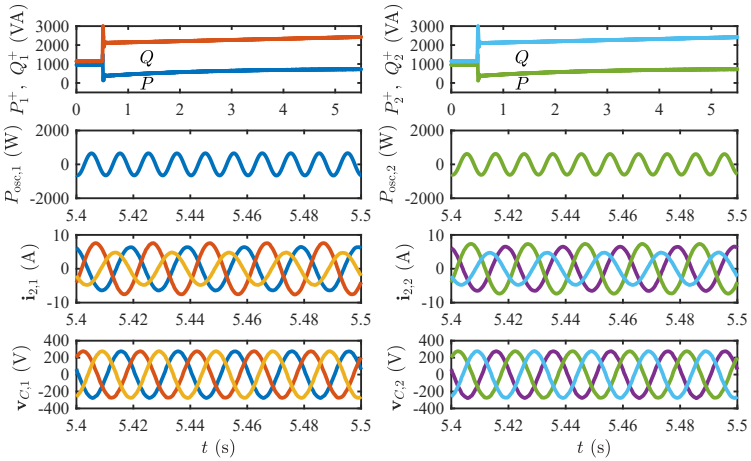


Figure 7.9: Parallel converter operation during test case 2 with SCR=3 and grid-forming VSS.

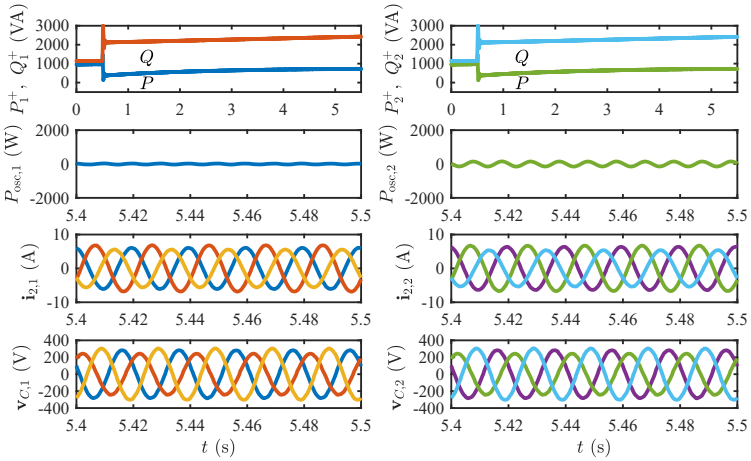


Figure 7.10: Parallel converter operation during test case 2 with SCR=3 and grid-forming AARC.

$\hat{V}_{\mathrm{min}}/\hat{V}_{\mathrm{max}}$ and possible overvoltages $\hat{V}_{\mathrm{max}}$. The VSS sufficiently balances the voltages but leads to large active power oscillations. In the test cases, predominantly the droop control affects the positive sequence voltage and causes comparably small $\hat{V}_{\mathrm{max}}$ for the VSS. This can be easily overcome by adjusting the voltage setpoints of the droop control. Both strategies result in similar current ratings indicated by $\hat{I}_{\mathrm{max}}/I_{\mathrm{r}}$. For the presented scenario, the current rating is in the range of 2 pu but crucially depends on the SCR, as described above, and

Table 7.1: Comparison of grid-forming VSS and AARC during a type C and type E fault with $|\underline{Z}_F|$=0.05 pu and SCR=3.

Fault	type C				type E			
Scheme	VSS		AARC		VSS		AARC	
Indicator	Conv. 1	Conv. 2	Conv. 1	Conv. 2	Conv. 1	Conv. 2	Conv. 1	Conv. 2
$\hat{V}_{\max}$ (pu)	0.88	0.89	0.97	0.98	0.85	0.86	0.94	0.94
$P_{\mathrm{ac},2\omega 1}$ (W)	1010	958	124	273	665	625	34	153
$\hat{V}_{\min}/\hat{V}_{\max}$ (pu)	1.00	0.99	0.71	0.61	.99	0.99	.80	0.80
$\hat{I}_{\max}/I_{\mathrm{r}}$ (pu)	2.2	2.2	1.8	1.8	2.2	2.1	2.0	1.9

thus will change significantly for other SCRs. The comparison clearly highlights the trade-off between rejecting active power oscillations and the VUF (here expressed as $\hat{V}_{\min}/\hat{V}_{\max}$). If a converter should predominantly support the grid voltage by applying the VSS strategy, the active power oscillations should be considered in the dc-link design. If balancing of the grid voltages is not necessary, the AARC with its small active power oscillations and slightly decreased current rating is an appropriate solution.

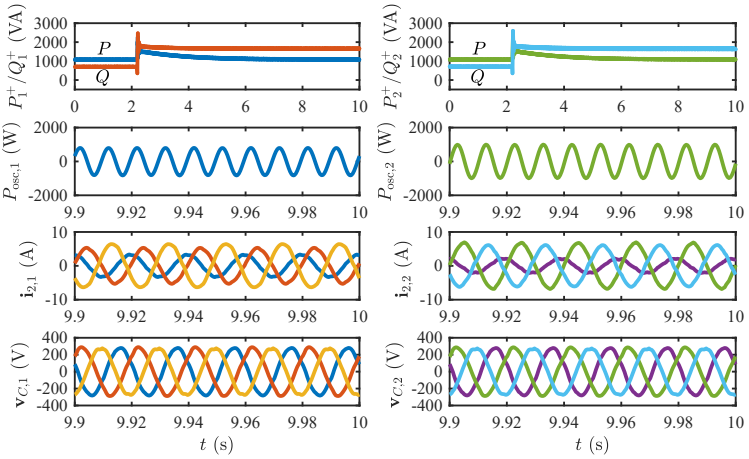


Figure 7.11: Measurement of test case 1 with SCR=5 and grid-forming VSS.

To experimentally validate the controls, the parallel converter test bench (see Fig. 4.8 and 4.10) is used in the same configuration as in the previous section. The operational scenario is chosen according to the defined test cases 1 and 2. The SCR has been selected to 5. The results for test case 1 are shown in Fig. 7.11, and the results of test case 2 are presented in the appendix C. Both test cases confirm the numerical simulation results, and thus the

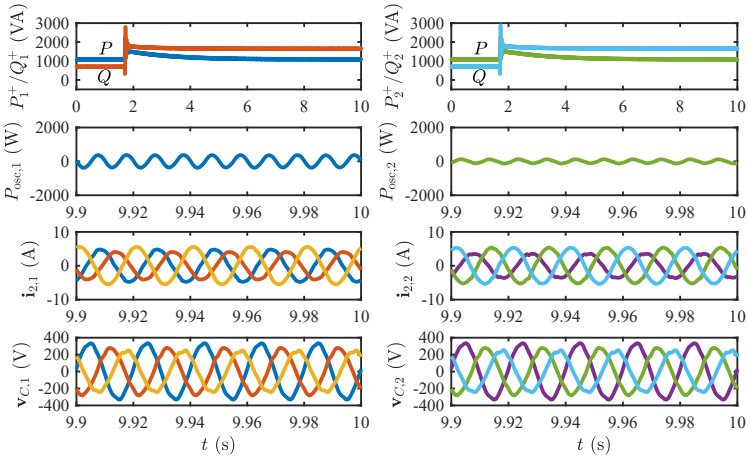


Figure 7.12: Measurement of test case 1 with SCR=5 and grid-forming AARC.

theoretical description. The grid voltages and currents contain significant harmonics, that are caused by a resonance between both converters. However, the parallel converters are successfully operated during unbalanced grid faults providing additional services such as rejecting active power oscillations or balancing the PCC voltages.

All in all, grid-forming controls are stable in very weak grids down to SCRs=1 but suffer from large current ratings in stiff grids during severe grid faults. However in stiff grids, grid-following controls achieve a stable control behavior and might be a better choice. Consequently, a combination of both controls may be a sufficient solution to flexibly operate in both weak and stiff grids.

8 Conclusion and Outlook

The research in this thesis aimed at the modeling of grid converters to identify and enhance critical converter and controller parts for operating in unbalanced and weak grids.

The Phase-Locked Loop (PLL) is identified as control-bottleneck and crucial structure for grid-following controls since it provides grid synchronization and sequence decomposition. Consequently, an analytical model is derived that describes the coupling between active and reactive power during grid faults caused by the PLL, which critically deteriorates converter current dynamics. Therefore, an adjustment of the current reference for the fault clearing is proposed to prevent overvoltages at the converter terminals. During fault initiation, only the PLL design can be optimized to meet objectives for settling times of reactive currents, and thus fast grid voltage support. Therefore, a multi-fidelity design process is proposed that guarantees grid code conformity for most PLLs and identifies PLLs that cannot comply with grid codes.

Due to recent grid codes, dual sequence current controls to inject positive and negative sequence currents during unbalanced faults are crucial to sufficiently support the grid voltages. Therefore, a VOC-based dual-sequence control with enhanced current and voltage limitation scheme is presented to improve dynamics and guarantee positive and negative sequence grid support. Different current reference generators and a Voltage Support Scheme (VSS) are compared regarding their grid support, converter utilization, and stability. The comparison indicates that current reference generators may accomplish similar grid support like the VSS by injecting active and reactive power according to the line impedance ratio. Consequently, the proposed Zero Active Power Oscillation Control (ZAPOC) provides a suitable trade-off between converter utilization and support of the grid voltages.

VOC may show insufficient stability in steady-state and during transient processes. Three critical controller parts are identified: PLLs, current reference generators, and the coupling of PLLs with the current control in weak grids. During severe grid faults, critical instability phenomena are identified for the LSRF, DSRF, and DSOGI-PLL, and an analytical stability criterion for the LSRF-PLL is derived based on Lyapunov's direct method. Stability of the

current reference generators in steady-state is assessed by determining the minimum Short Circuit Ratio (SCR). This evaluation indicates that VOC is prone to instability starting from SCR<5 depending on the applied current reference generator. The coupling of PLLs with the current control in weak grids is analyzed with Lyapunov's direct method. The stable state-space region or Region of Attraction (ROA), respectively, could be successfully determined and indicates that inductive grids are much more critical for transient stability of converters.

To overcome the stability problems of VOC, grid-forming controls can be used to operate converters in very weak grids. It is shown, that the converter current rating can be directly derived with the SCR. Accordingly, grid-forming controls are particularly suitable for very weak grids, whereas increasing SCRs require very large current ratings of the converters. Fortunately, for large SCRs the VOC achieves satisfactory results and grid-forming controls might not be necessary. The grid-forming controls can also be utilized for grid support during unbalanced faults by directly applying a VSS. In contrast, the proposed grid-forming AARC rejects the active power oscillations, and thus improves the converter utilization.

All models and findings are thoroughly verified by a multi-fidelity modeling approach utilizing analytical models for explaining the mechanisms, large-signal numerical models to verify the analytical models and their assumptions, and a hardware test bench to experimentally validate the models and to identify critical effects that are not captured by the model.

Based on these results and findings, several emerging topics are identified that may achieve valuable contributions to extend the presented investigations.
The analysis of converter controls during unbalanced faults by using symmetrical components theory yields accurate results. However, the positive and negative sequence may couple due to PLLs, current reference generators, and power calculations of the converter control. This coupling cannot be sufficiently described with LTI-models, whereas LTP-models provide promising analysis tools to capture these coupling mechanisms.
The transient stability analysis and the stability assessment by sophisticated methods such as Lyapunov's direct method should be extended to prefilter PLLs and advanced control structures. This promising method derives analytical stability criteria that are valuable for understanding the dynamics of grid converter controls.
For validating the models, the test benches may be extended by a Power Hardware in the Loop (PHIL) system to emulate grid nodes of larger grid structures. This would enable the analysis to focus on larger and more realistic power systems and still achieve a high fidelity of the converter and its control due to the converter prototypes.

The overall investigations indicate that grid-following converters achieve satisfactory control performance for stiff to weak grids, whereas grid-forming converters show satisfactory results for weak to very weak grids. Consequently, converter-dominated grids may rely on a diverse distribution of grid-following and grid-forming converters to benefit from the performance

of both structures. Throughout the work on this thesis the author's opinion solidified that the amount of sophisticated and complex control structures for grid converters is steadily increasing, while analytical methods to assess stability, control performance and physical understanding are still urgently demanded for less complex structures. Therefore, future research may focus on enhancing mature methods from power system engineering to the needs of the analysis of power electronics systems and their sophisticated controls.

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Publications

The following papers were published during my work in the department of power electronics at TU Berlin. They are based in part on the results of this thesis:

- H. Just, H. Yang, M. Eggers, M. Kaufmann-Bühler and S. Dieckerhoff, "Assessing Power Factor Distortion and Transient Current Response of Grid Converters During Fault Ride-Through with Extended PLL Models," in **2020 IEEE 21th Workshop on Control and Modeling for Power Electronics (COMPEL)**, Aalborg, Denmark, 2020.
- H. Just, H. Yang, M. Eggers, P. Teske and S. Dieckerhoff, "Multi-Fidelity Model-based PLL Design for Enhanced Dynamics and Transient Stability during Fault Ride-Through," in **2020 IEEE 21th Workshop on Control and Modeling for Power Electronics (COMPEL)**, Aalborg, Denmark, 2020.
- H. Yang, H. Just, M. Eggers and S. Dieckerhoff, "Wirtinger Calculus Based Modeling and Analysis of VSG-Dominated Grids," in **2020 IEEE 21th Workshop on Control and Modeling for Power Electronics (COMPEL)**, Aalborg, Denmark, 2020.
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- B. Freudenberg, H. Just, J. Saur, D. Römer, S. Dieckerhoff, "Grid Integration and Control of a Stacked Multicell Converter under Asymmetric Grid Conditions," in **19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)**, Warsaw, Poland, 2017.
- H. Just, B. Freudenberg, S. Dieckerhoff, "Analysis and Experimental Verification of Current Limiting Methods for Grid Converters under Unbalanced Load Conditions," in **18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)**, Karlsruhe, Germany, 2016.

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A Theory

A.1 Converter Losses

Semiconductor losses of power converters can be separated into conduction losses and switching losses. Assuming an inverter half-bridge that is controlled by an SPWM, the conduction losses of the IGBT ($P_{\text{cond (T)}}$) and diode ($P_{\text{cond (D)}}$) can be calculated according to [5, pp.277-279]:

$$P_{\text{cond (T)}} = \left(\frac{1}{2\pi} + \frac{m \cdot \cos(\varphi)}{8}\right) \cdot V_{\text{CE0}} \cdot \hat{I}_1 + \left(\frac{1}{8} + \frac{m \cdot \cos(\varphi)}{3\pi}\right) \cdot r_{\text{CE}} \cdot \hat{I}_1^2 \quad , \tag{A.1}$$

$$P_{\text{cond (D)}} = \left(\frac{1}{2\pi} - \frac{m \cdot \cos(\varphi)}{8}\right) \cdot V_{\text{F0}} \cdot \hat{I}_1 + \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) \cdot r_{\text{F}} \cdot \hat{I}_1^2 \quad , \tag{A.2}$$

where m is the modulation index, $\cos(\varphi)$ is the power factor, V_{CE0} is the collector-emitter threshold voltage, r_{CE} is the on-state resistance of the IGBT, $\hat{I}_1$ is amplitude of the current at fundamental frequency, V_{F0} is the forward threshold voltage, and r_{F} is the on-state resistance of the diode.
Calculating the overall conduction losses and rearranging the equations above to derive the dependency on $m\cos(\varphi)$ leads to:

$$\begin{aligned} P_{\text{cond}} = P_{\text{cond (D)}} + P_{\text{cond (T)}} = & \tfrac{1}{2\pi}\left(V_{\text{CE0}} + V_{\text{F0}}\right)\hat{I}_1 + \tfrac{1}{8}\left(r_{\text{CE}} + r_{\text{F}}\right)\hat{I}_1^2 \\ & + \tfrac{m\cdot\cos(\varphi)}{8}\left(V_{\text{CE0}} - V_{\text{F0}}\right)\hat{I}_1 + \tfrac{m\cdot\cos(\varphi)}{3\pi}\left(r_{\text{CE}} - r_{\text{F}}\right)\hat{I}_1^2 \quad . \end{aligned} \tag{A.3}$$

This expression indicates that the conduction losses do not depend on $m\cdot\cos(\varphi)$ for $V_{\text{CE0}} \approx V_{\text{F0}}$ and $r_{\text{CE}} \approx r_{\text{F}}$. A real example that fulfills this requirement is the *Semikron MiniSKiiP 35NAB12T4V1* module used for the converter prototype presented in section 4.2.1.

A.2 Symmetrical Components Theory

This section provides additional information for the sequence decomposition in different reference frames and focuses on the expressions for the negative sequence and inverse transformations derived in section 3.2.

The transformation matrix $\underline{\mathbf{T}}_-$ and $\underline{\mathbf{T}}_0$ for the negative sequence and zero sequence in abc-frame is given by:

$$\vec{\mathbf{x}}^-_{\mathrm{abc}} = \begin{bmatrix} \vec{x}^-_{\mathrm{a}} \\ \vec{x}^-_{\mathrm{b}} \\ \vec{x}^-_{\mathrm{c}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \underline{a}^2 & \underline{a} \\ \underline{a} & 1 & \underline{a}^2 \\ \underline{a}^2 & a & 1 \end{bmatrix} \vec{\mathbf{x}}_{\mathrm{abc}} = \frac{1}{3} \underline{\mathbf{T}}_- \vec{\mathbf{x}}_{\mathrm{abc}} \quad , \tag{A.4}$$

$$\vec{\mathbf{x}}^0_{\mathrm{abc}} = \begin{bmatrix} \vec{x}^0_{\mathrm{a}} \\ \vec{x}^0_{\mathrm{b}} \\ \vec{x}^0_{\mathrm{c}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \vec{\mathbf{x}}_{\mathrm{abc}} = \frac{1}{3} \underline{\mathbf{T}}_0 \vec{\mathbf{x}}_{\mathrm{abc}} \quad . \tag{A.5}$$

Rearranging these expressions leads to the instantaneous sequence decomposition based on the operator q as described by:

$$\vec{\mathbf{x}}^-_{\mathrm{abc}} = \frac{1}{3} \begin{bmatrix} \vec{x}_{\mathrm{a}} - \frac{1}{2}(\vec{x}_{\mathrm{b}} + \vec{x}_{\mathrm{c}}) + \frac{\sqrt{3}}{2}(\underline{q}\vec{x}_{\mathrm{b}} - \underline{q}\vec{x}_{\mathrm{c}}) \\ \vec{x}_{\mathrm{b}} - \frac{1}{2}(\vec{x}_{\mathrm{c}} + \vec{x}_{\mathrm{a}}) + \frac{\sqrt{3}}{2}(\underline{q}\vec{x}_{\mathrm{c}} - \underline{q}\vec{x}_{\mathrm{a}}) \\ \vec{x}_{\mathrm{c}} - \frac{1}{2}(\vec{x}_{\mathrm{a}} + \vec{x}_{\mathrm{b}}) + \frac{\sqrt{3}}{2}(\underline{q}\vec{x}_{\mathrm{a}} - \underline{q}\vec{x}_{\mathrm{b}}) \end{bmatrix} \quad , \tag{A.6}$$

$$\vec{\mathbf{x}}^0_{\mathrm{abc}} = \frac{1}{3} \begin{bmatrix} \vec{x}_{\mathrm{a}} + \vec{x}_{\mathrm{b}} + \vec{x}_{\mathrm{c}} \\ \vec{x}_{\mathrm{a}} + \vec{x}_{\mathrm{b}} + \vec{x}_{\mathrm{c}} \\ \vec{x}_{\mathrm{a}} + \vec{x}_{\mathrm{b}} + \vec{x}_{\mathrm{c}} \end{bmatrix} \quad . \tag{A.7}$$

The decomposition can be performed in dq-frame or $\alpha\beta$-frame. The inverse of Clarke's transformation is given by:

$$\mathbf{T}^{-1}_{\alpha\beta 0} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \quad , \tag{A.8}$$

and the inverse Park transformation is defined according to:

$$\mathbf{x}_{\mathrm{abc}} = \begin{bmatrix} \cos(\omega_1 t) & -\sin(\omega_1 t) & 1 \\ \cos(\omega_1 t - \frac{2\pi}{3}) & -\sin(\omega_1 t - \frac{2\pi}{3}) & 1 \\ \cos(\omega_1 t + \frac{2\pi}{3}) & -\sin(\omega_1 t - \frac{2\pi}{3}) & 1 \end{bmatrix} \mathbf{x}_{\mathrm{dq0}} = \mathbf{T}^{-1}_{\mathrm{abc/dq0}} \mathbf{x}_{\mathrm{dq0}} \quad . \tag{A.9}$$

The inverse transformation of the sequentially applied Clarke and Park transform has the form:

$$\mathbf{x}_{\alpha\beta 0} = \begin{bmatrix} \cos(\omega_1 t) & -\sin(\omega_1 t) & 0 \\ \sin(\omega_1 t) & \cos(\omega_1 t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \mathbf{x}_{\mathrm{dq0}} = \mathbf{T}^{\mathrm{T}}_{\mathrm{dq0}} \mathbf{x}_{\mathrm{dq0}} \quad . \tag{A.10}$$

The ISC decomposition for the negative sequence in the dq-frame leads to:

$$\mathbf{x}_{\mathrm{dq}}^{-} = \begin{bmatrix} x_{\mathrm{d}}^{-} \\ x_{\mathrm{q}}^{-} \end{bmatrix} = \mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{x}_{\alpha\beta}^{-} = \frac{1}{2}\begin{bmatrix} \cos(\omega_1 t) & -\sin(\omega_1 t) \\ \sin(\omega_1 t) & \cos(\omega_1 t) \end{bmatrix}\begin{bmatrix} 1 & \underline{q} \\ -\underline{q} & 1 \end{bmatrix}\mathbf{x}_{\alpha\beta} \quad . \tag{A.11}$$

The effect of Park's transformation on the negative sequence indicates the coupling terms between positive and negative sequence according to:

$$\begin{aligned} \mathbf{x}_{\mathrm{dq}^{-}} = \mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{x}_{\alpha\beta} &= \mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{x}_{\alpha\beta}^{-} + \mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{x}_{\alpha\beta}^{+} + \sum_{n=-m}^{m}\mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{x}_{\alpha\beta}^{n} \\ &= \overline{\mathbf{x}}_{\mathrm{dq}}^{-} + \mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{T}_{\mathrm{dq}}^{\mathrm{T}}\overline{\mathbf{x}}_{\mathrm{dq}^{-}}^{+} + \sum_{n=-m}^{m}\mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{T}_{\mathrm{dq}^{\mathrm{n}}}^{\mathrm{T}}\mathbf{x}_{\mathrm{dq}^{-}}^{n} \\ &= \overline{\mathbf{x}}_{\mathrm{dq}}^{-} + \mathbf{T}_{\mathrm{dq}^{-2}}\overline{\mathbf{x}}_{\mathrm{dq}}^{+} + \sum_{n=-m}^{m}\mathbf{T}_{\mathrm{dq}^{-(1+\mathrm{n})}}\overline{\mathbf{x}}_{\mathrm{dq}}^{n}. \end{aligned} \tag{A.12}$$

Assuming that the phase angle of the negative sequence is unknown, the following expression can be derived for the negative sequence, which serves as basis for the PLL algorithms in chapter 5.

$$\begin{aligned} \mathbf{x}_{\mathrm{dq}}^{-} = \mathbf{T}_{\mathrm{dq}^{-1}}\mathbf{x}_{\mathrm{abc}} = &\underbrace{\hat{X}_{\mathrm{S},-1}\begin{bmatrix} \cos(\delta_{-1}) \\ \sin(\delta_{-1}) \end{bmatrix}}_{\overline{\mathbf{x}}_{\mathrm{dq}-}^{-}} \\ &+ \underbrace{\hat{X}_{\mathrm{S},1}\begin{bmatrix} \cos(2\omega_1 t + \delta_{+1}) \\ \sin(2\omega_1 t + \delta_{+1}) \end{bmatrix}}_{\mathbf{x}_{\mathrm{dq}-}^{+}} + \underbrace{\sum_{n=-m}^{m}\hat{X}_{\mathrm{S},n}\begin{bmatrix} \cos((n+1)\omega_1 t + \delta_n) \\ \sin((n+1)\omega_1 t + \delta_n) \end{bmatrix}}_{\mathbf{x}_{\mathrm{dq}-}^{n}} \end{aligned} \tag{A.13}$$

A.3 Symmetrical Optimum for PLLs

The Symmetrical Optimum (SO) is based on the open-loop characteristics of a type 2 plant according to section 5.4. The following expressions determine the PLL gain k_{p} based on the desired control bandwidth ω_{c}. The open-loop magnitude at the cross-over frequency can be derived as follows:

$$\left|\frac{k_{\mathrm{p}}\omega_{\mathrm{p}}\left(j\omega_{\mathrm{c}} + \omega_{\mathrm{z}}\right)}{\omega_{\mathrm{c}}^2\left(j\omega_{\mathrm{c}} + \omega_{\mathrm{p}}\right)}\right| = 1 \Leftrightarrow \quad \left|\frac{\omega_{\mathrm{c}}\left(j + \frac{\omega_{\mathrm{z}}}{\omega_{\mathrm{c}}}\right)}{\left(j\omega_{\mathrm{c}} + \omega_{\mathrm{p}}\right)}\right| = \frac{\omega_{\mathrm{c}}}{k_{\mathrm{p}}} \Leftrightarrow \quad \left|\frac{\left(j + \frac{\omega_{\mathrm{z}}}{\omega_{\mathrm{c}}}\right)}{\left(j\frac{\omega_{\mathrm{c}}}{\omega_{p}} + 1\right)}\right| = \frac{\omega_{\mathrm{c}}}{k_{\mathrm{p}}} \quad . \tag{A.14}$$

Analyzing the trigonometric expressions for the frequency definitions in section 5.4 leads the cross-over frequency ω_{c}:

$$\begin{matrix} \frac{\omega_{\mathrm{z}}}{\omega_{\mathrm{c}}} = \frac{1}{\tan(\phi_{\mathrm{z}})} = \frac{\cos(\phi_{\mathrm{z}})}{sin(\phi_{\mathrm{z}})} \\ \frac{\omega_{\mathrm{c}}}{\omega_{\mathrm{p}}} = \frac{sin(\phi_{\mathrm{p}})}{\cos(\phi_{\mathrm{p}})} \end{matrix} \quad , \tag{A.15}$$

$$\frac{\sqrt{\frac{\sin(\phi_z)^2+\cos(\phi_z)^2}{\sin(\phi_z^2)^2}}}{\sqrt{\frac{\cos(\phi_p)^2+\sin(\phi_p)^2}{\cos(\phi_p)^2}}} = \frac{\omega_c}{k_p} \quad , \tag{A.16}$$

$$\frac{\cos(\phi_p)}{\sin(\phi_z)} = \frac{\omega_c}{k_p} \quad . \tag{A.17}$$

Rearranging these equations leads to the design rule for k_p, as described by:

$$\begin{aligned} \cos\left(\tan^{-1}\left(\frac{\omega_c}{\omega_p}\right)\right) &= \cos\left(\tan^{-1}\left(\frac{\sqrt{\omega_z\omega_p}}{\omega_p}\right)\right) \\ &= \cos\left(\tan^{-1}\left(\sqrt{\frac{\omega_z}{\omega_p}}\right)\right) = \frac{1}{\sqrt{\frac{\omega_z}{\omega_p}+1}} \end{aligned} \quad , \tag{A.18}$$

$$\sin\left(\tan^{-1}\left(\frac{\omega_c}{\omega_z}\right)\right) = \sin\left(\tan^{-1}\left(\sqrt{\frac{\omega_p}{\omega_z}}\right)\right) = \sqrt{\frac{\omega_p}{\omega_z}}\frac{1}{\sqrt{\frac{\omega_p}{\omega_z}+1}} \quad , \tag{A.19}$$

$$\omega_c = k_p\frac{\cos(\phi_p)}{\sin(\phi_z)} = \frac{\sqrt{\frac{\omega_p}{\omega_z}+1}\sqrt{\omega_z}}{\sqrt{\frac{\omega_z}{\omega_p}+1}\sqrt{\omega_p}}k_p = \frac{\sqrt{\omega_p+\omega_z}}{\sqrt{\omega_z+\omega_p}}k_p = k_p \quad . \tag{A.20}$$

Then, the relation between ω_c and the maximum PM can be calculated as follows:

$$\frac{\partial PM}{\partial \omega_c} = 0 \quad , \tag{A.21}$$

$$\frac{1}{\omega_z}\frac{1}{\left(\frac{\omega_c}{\omega_z}\right)^2+1} - \frac{1}{\omega_p}\frac{1}{\left(\frac{\omega_c}{\omega_p}\right)^2+1} = 0 \quad , \tag{A.22}$$

$$\begin{aligned} \frac{\omega_c^2}{\omega_z^2}+\omega_z &= \frac{\omega_c^2}{\omega_p^2}+\omega_p \\ \omega_c^2\left(\frac{1}{\omega_z^2}-\frac{1}{\omega_p}\right) &= \omega_p - w_c \\ \omega_c^2 &= \frac{(\omega_p-\omega_q)}{\omega_p-\omega_z}\omega_z\omega_p \\ \omega_c &= \sqrt{\omega_z\omega_p} \end{aligned} \quad . \tag{A.23}$$

These expressions lead to the design rules for the PLL parameters k_p and k_i according to 5.33.

A.4 *LCL*-filter Transfer Function

The transfer functions can be calculated based on the block diagram. In order to obtain the transfer functions, the block diagram must be transformed to the normal form, as shown in Fig. A.1. From the normal form in Fig. A.1c, the transfer functions can be directly extracted and lead to 4.14.

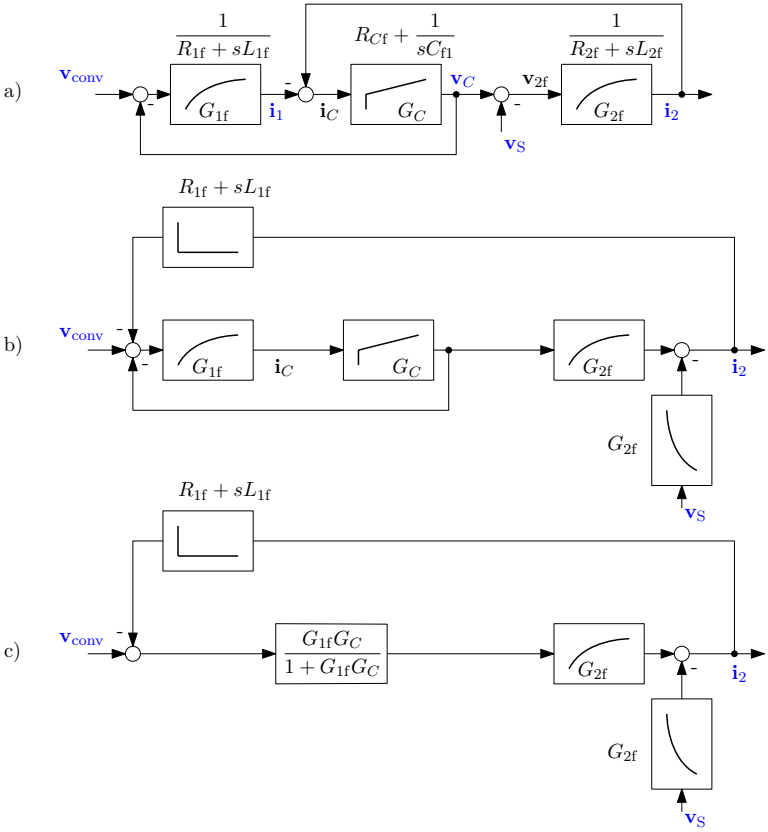

Figure A.1: Block diagram of the *LCL*-filter in Laplace domain.

A.5 Block Diagram Transformation of PR-Current Control

The control block diagram presented in Fig. 6.44 must be rearranged to derive the closes-loop transfer functions of the system, as shown in Fig. A.2. These transfer functions consider all delay terms in the feedback path $\tau_{\mathrm{d,m}}$ and the sampling or SPWM delay τ_{d} of the converter. Then, the block diagram can be further simplified by defining the following transfer functions:

$$G_{\mathrm{IL}} = \frac{G_{\mathrm{OL1}}}{1 - G_{\mathrm{OL1}}(G_{\mathrm{FB1}} + G_{\mathrm{FB2}})} \quad , \tag{A.24}$$

$$G_{\mathrm{OL1}} = \frac{G_{\mathrm{PR}} G_{\mathrm{d,conv}} G_{\mathrm{1f}} G_C}{1 - G_{\mathrm{PR}} G_{\mathrm{d,conv}} G_{\mathrm{1f}} G_{\mathrm{d,ADC}}} \quad , \tag{A.25}$$

$$G_{\mathrm{FB1}} = \frac{G_{\mathrm{d,ADC}}}{G_{\mathrm{PR}}} \quad , \tag{A.26}$$

$$G_{\mathrm{FB2}} = -\frac{1}{G_{\mathrm{PR}} G_{\mathrm{d,conv}}} \quad , \tag{A.27}$$

$$G_{\mathrm{FB3}} = -\left(\frac{G_{\mathrm{PR}} G_{\mathrm{d,conv}} G_{\mathrm{1f}}}{1 - G_{\mathrm{PR}} G_{\mathrm{d,conv}} G_{\mathrm{1f}} G_{\mathrm{d,ADC}}} \right)^{-1} \quad . \tag{A.28}$$

Based on these transfer functions, the block diagram shown in Fig. A.3 is obtained, and the closed-loop transfer functions of the PR-Current Control can be derived as follows:

$$G_{\mathrm{Conv}}(\mathbf{v}_{\mathrm{S}} = 0) = \frac{\mathbf{i}_2(s)}{\mathbf{i}_1^*(s)} = \frac{G_{\mathrm{IL}} G_{\mathrm{2f}}}{1 - G_{\mathrm{IL}} G_{\mathrm{2f}} (G_{\mathrm{d,ADC}} + G_{\mathrm{FB3}})} \quad , \tag{A.29}$$

$$G_{\mathrm{S}}(\mathbf{i}_1^* = 0) = \frac{\mathbf{i}_2(s)}{\mathbf{v}_{\mathrm{S}}(s)} = \frac{-G_{\mathrm{2f}}}{1 - G_{\mathrm{IL}} G_{\mathrm{2f}} (G_{\mathrm{d,ADC}} + G_{\mathrm{FB3}})} \quad . \tag{A.30}$$

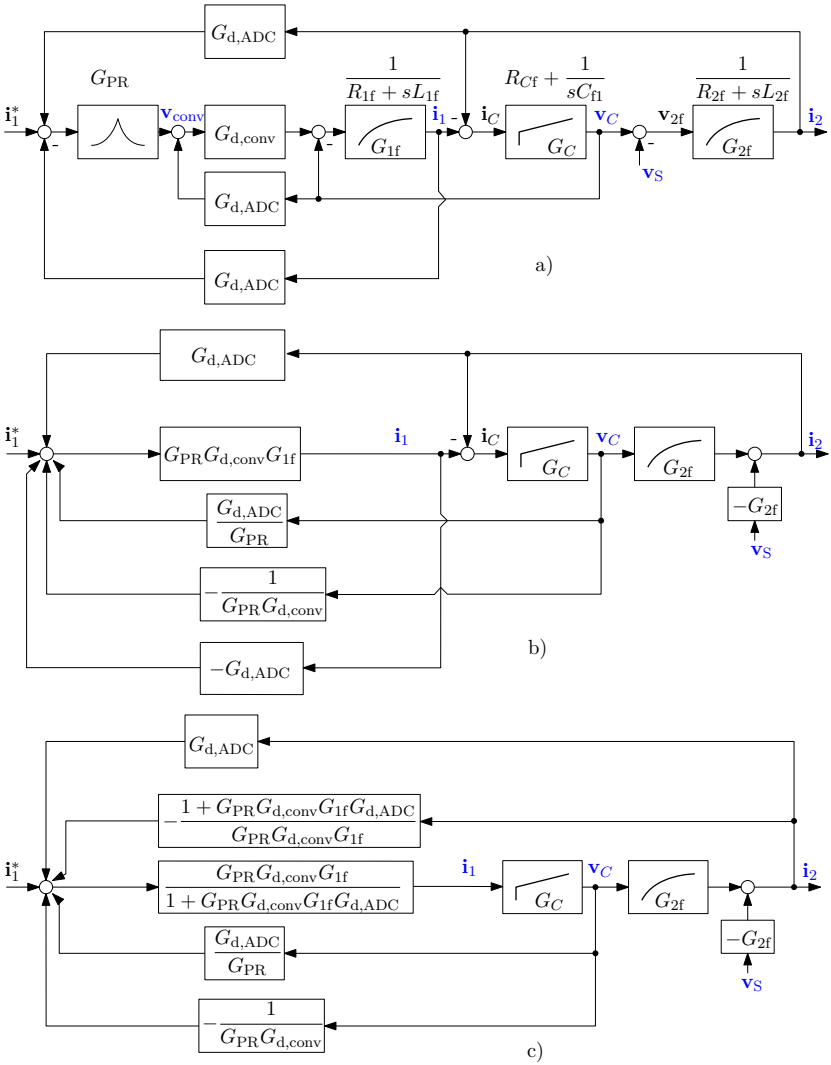

Figure A.2: Block Scheme of current control for transfer function extraction part 1.

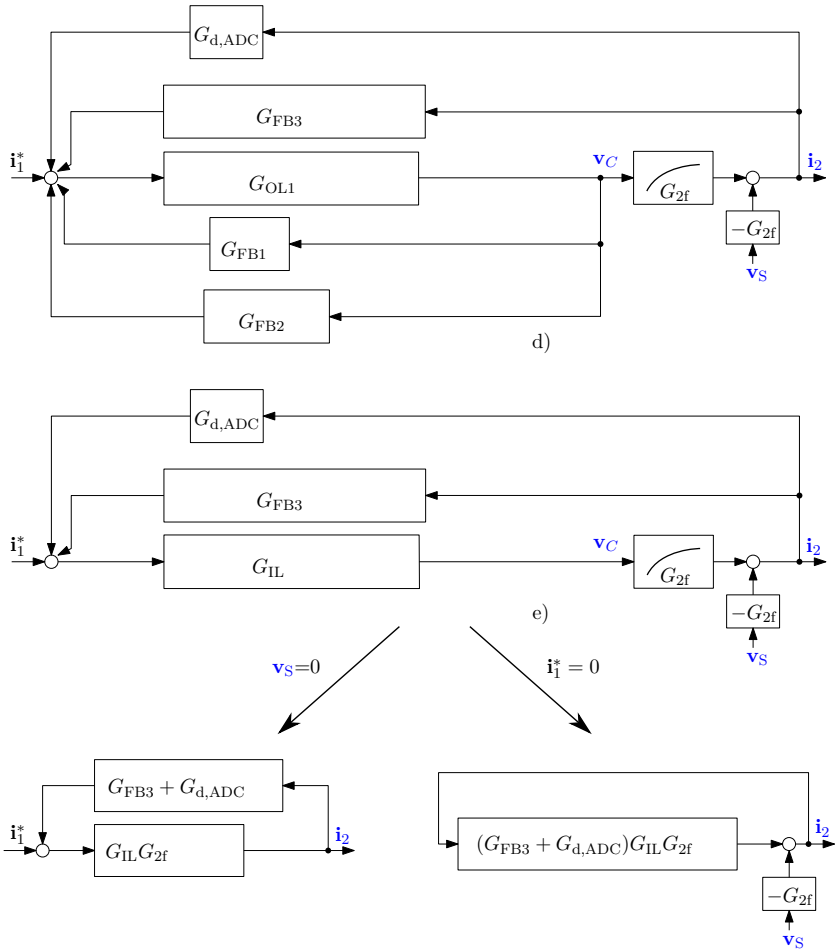

Figure A.3: Block Scheme of current control for transfer function extraction part 2

B Lyapunov Function for SRF-PLLs in Weak Grids

The derivative of the Lyapunov candidate according to 6.62 is described by:

$$\begin{aligned}\dot{V} = &\left(-\frac{k_\mathrm{i} L_s i_{\mathrm{d,PLL}} p}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1}\right) {x_2}^2 + \left(-\frac{1}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1} + \frac{k_\mathrm{i} \hat{V}_{\mathrm{S},1} p \sigma_1}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1}\right) x_2 \sin\left(x_1\right) \\ &+ (\sigma_4 + \sigma_2) x_2 \cos\left(x_1\right) + (-\sigma_4 - \sigma_2) x_2 + \frac{k_\mathrm{p} \hat{V}_{\mathrm{S},1} \sigma_1}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1} \sin\left(x_1\right)^2 \\ &+ (\sigma_5 + \sigma_3) \sin\left(x_1\right) \cos\left(x_1\right) + (-\sigma_5 - \sigma_3) \sin\left(x_1\right) \quad ,\end{aligned}$$

where

$$\begin{aligned}\sigma_1 &= \sqrt{1 - \frac{L_s {i_{\mathrm{d,PLL}}}^2 {w_0}^2}{\hat{V}_{\mathrm{S},1}^2} - \frac{2 L_s i_{\mathrm{d,PLL}} R_s i_{\mathrm{q,PLL}} w_0}{\hat{V}_{\mathrm{S},1}^2} - \frac{R_s {i_{\mathrm{q,PLL}}}^2}{\hat{V}_{\mathrm{S},1}^2}} \quad , \\ \sigma_2 &= \frac{k_\mathrm{i} L_s i_{\mathrm{d,PLL}} p w_0}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1} \quad , \\ \sigma_3 &= \frac{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} w_0}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1} \quad , \\ \sigma_4 &= \frac{k_\mathrm{i} R_s i_{\mathrm{q,PLL}} p}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1} \quad , \\ \sigma_5 &= \frac{k_\mathrm{p} R_s i_{\mathrm{q,PLL}}}{k_\mathrm{p} L_s i_{\mathrm{d,PLL}} - 1} \quad .\end{aligned} \tag{B.1}$$

The parameter p should be used to create a negative definite region of $\dot{V}$ near the origin. This can be achieved if $x_2 \sin\left(x_1\right)$ is zero, and leads to p according to 6.62.

The modified Lyapunov candidate according to 6.63 is used for the inductive grid, and its derivative can be calculated as follows:

$$
\begin{aligned}
\dot{V} = &\left(-\tfrac{\beta}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1}\right) {x_2}^2 \cos\left(x_1\right) + \left(-\tfrac{k_\mathrm{i} L_\mathrm{s} i_{\mathrm{d,PLL}} p}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1}\right) {x_2}^2 \\
&+ \tfrac{k_\mathrm{p} \hat{V}_{\mathrm{S},1} \beta \sigma_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} x_2 \sin\left(x_1\right) \cos\left(x_1\right) + \left(-\tfrac{1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} - \tfrac{k_\mathrm{i} L_\mathrm{s} i_{\mathrm{d,PLL}} \beta}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} + \tfrac{k_\mathrm{i} \hat{V}_{\mathrm{S},1} p \sigma_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1}\right) x_2 \sin\left(x_1\right) \\
&+ (\sigma_7 + \sigma_3) x_2 \cos\left(x_1\right)^2 + (\sigma_6 - \sigma_7 - \sigma_3 + \sigma_2) x_2 \cos\left(x_1\right) + (-\sigma_6 - \sigma_2) x_2 \\
&+ \left(\tfrac{k_\mathrm{p} \hat{V}_{\mathrm{S},1} \sigma_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} + \tfrac{k_\mathrm{i} \hat{V}_{\mathrm{S},1} \beta \sigma_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1}\right) \sin\left(x_1\right)^2 \\
&+ (\sigma_9 + \sigma_8 + \sigma_5 + \sigma_4) \sin\left(x_1\right) \cos\left(x_1\right) + (-\sigma_9 - \sigma_8 - \sigma_5 - \sigma_4) \sin\left(x_1\right) \quad ,
\end{aligned}
$$

where

$$
\begin{aligned}
\sigma_1 &= \sqrt{1 - \tfrac{L_\mathrm{s} {i_{\mathrm{d,PLL}}}^2 {\omega_1}^2}{\hat{V}_{\mathrm{S},1}^2} - \tfrac{2 L_\mathrm{s} i_{\mathrm{d,PLL}} R_\mathrm{S} i_{\mathrm{q,PLL}} \omega_1}{\hat{V}_{\mathrm{S},1}^2} - \tfrac{R_\mathrm{S} {i_{\mathrm{q,PLL}}}^2}{\hat{V}_{\mathrm{S},1}^2}}} \quad , \\
\sigma_2 &= \tfrac{k_\mathrm{i} L_\mathrm{s} i_{\mathrm{d,PLL}} p \omega_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_3 &= \tfrac{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} \beta \omega_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_4 &= \tfrac{k_\mathrm{i} L_\mathrm{s} i_{\mathrm{d,PLL}} \beta \omega_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_5 &= \tfrac{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} \omega_1}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_6 &= \tfrac{k_\mathrm{i} R_\mathrm{S} i_{\mathrm{q,PLL}} p}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_7 &= \tfrac{k_\mathrm{p} R_\mathrm{S} i_{\mathrm{q,PLL}} \beta}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_8 &= \tfrac{k_\mathrm{i} R_\mathrm{S} i_{\mathrm{q,PLL}} \beta}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad , \\
\sigma_9 &= \tfrac{k_\mathrm{p} R_\mathrm{S} i_{\mathrm{q,PLL}}}{k_\mathrm{p} L_\mathrm{s} i_{\mathrm{d,PLL}} - 1} \quad .
\end{aligned}
\tag{B.2}
$$

The parameter β can be used to reject the ${x_2}^2$ dependency in the first two terms to achieve a negative region near the origin. Setting these both terms to zero leads to $\beta = 1.7 \cdot k_\mathrm{i} L_\mathrm{s} i_{\mathrm{d,PLL}} p$ according to 6.63. The additional scaling factor of 1.7 compensates the $\cos\left(x_1\right)$ part to suppress the x_2^2 dependency for small, positive x_1 values.

C Power References for Grid-forming Converters

To derive the voltage reference for the negative sequence to reject the imaginary power oscillations, the following expressions are derived:

$$\tilde{q}_{\mathrm{ac}} = -\left(\mathbf{i}^{-} \times \mathbf{v}^{+}\right) \cdot \mathbf{1} - \left(\mathbf{i}^{+} \times \mathbf{v}^{-}\right) \cdot \mathbf{1} = 0 \quad , \tag{C.1}$$

$$\mathbf{v}_{C}^{-} = \frac{\mathbf{v}_{C}^{+}}{\left(1 - \mathbf{Z}^{-}\left(\mathbf{Z}^{+}\right)^{-1}\right)\mathbf{v}_{C}^{+} + \mathbf{v}_{\mathrm{S}}^{+}} \mathbf{v}_{\mathrm{S}}^{-} \text{ with } \qquad \mathbf{Z}^{-}\left(\mathbf{Z}^{+}\right)^{-1} = 1 \quad . \tag{C.2}$$

The imaginary power oscillations are rejected if the voltage is selected according to:

$$\mathbf{v}_{C,\mathrm{PNSC}}^{-} = \frac{\mathbf{v}_{C}^{+}}{\mathbf{v}_{\mathrm{S}}^{+}} \mathbf{v}_{\mathrm{S}}^{-} \quad . \tag{C.3}$$

The experimental validation is conducted for the test case 2 (type E fault) with the parallel converter test bench according to section 7.2. The results presented in Fig. C.2 and C.1 confirm the conclusion of section 7.2, that the grid-forming AARC successfully reduces the active power oscillations, whereas the grid-forming VSS balances the voltages. The remaining active power oscillations achieved with the AARC are caused by the implementation as discussed in section 7.2.

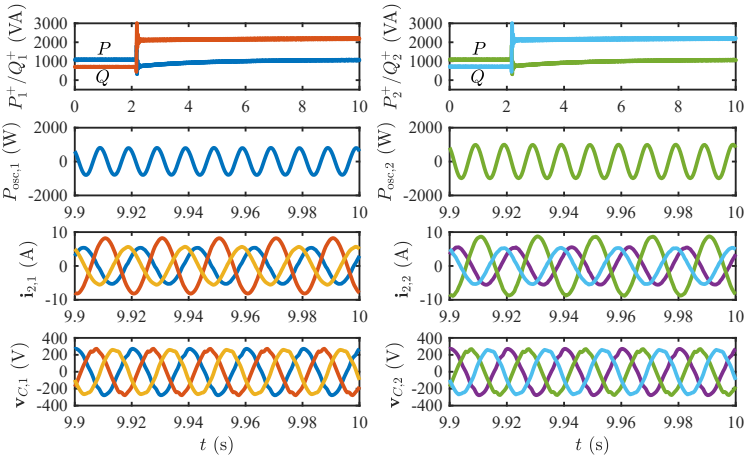

Figure C.1: Measurement of parallel converter operation during test case 2 with grid-forming VSS in a very weak grid with SCR=5.

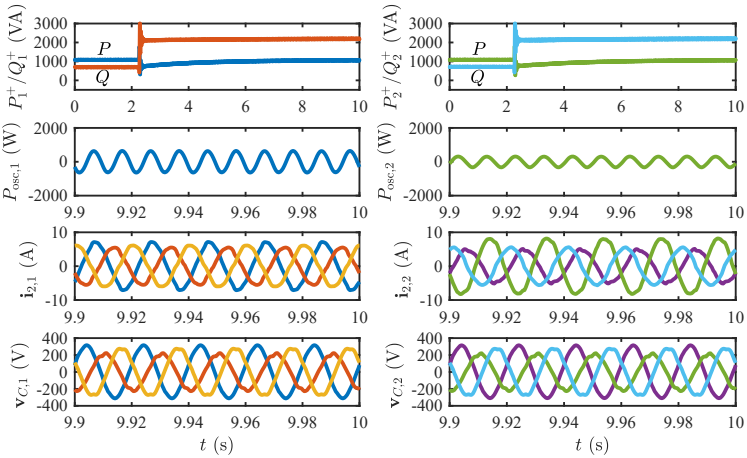

Figure C.2: Measurement of parallel converter operation during test case 2 with grid-forming AARC in a very weak grid with SCR=5.

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Modeling and control of power converters in weak and unbalanced electric grids

Grid converters increasingly affect power system operation due to the increasing share of renewable energy sources and less conventional power plants based on synchronous generators. This shift in power generation leads to converter-dominated weak grids, which are prone to critical stability phenomena but also enable converters to contribute to grid stability and voltage support. Converter controls predominantly determine how converters interact with the power system and must handle even severe operational scenarios such as unbalanced faults and weak grids. This thesis presents critical parts of converter controls and sophisticated control schemes to handle severe grid scenarios. These converter controls are modeled and analyzed to assess their characteristics, derive design criteria, and develop dedicated stability analysis methods for grid converters.

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