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Study and design of topologies and components for high power density DC-DC converters

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To my parents
Gaetano and Stefania

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Chapter 1
Introduction

Switching power converters are receiving considerable research attention in terms of size reduction while preserving, or increasing, the quantity of output power and the conversion efficiency they can provide. This attention is directly generated by the need of reducing the volume occupation in electronic systems directly addressable to power management. In fact, power management is often considered as a "ghost" functionality which is always necessary but should affect as minimum as possible the overall system requirements. In terms of occupied volume, this directly translates to the consideration that if the one occupied by power management can be reduced, there will be more space for adding functionality or simply to miniaturize the overall system.

This is mostly evident in consumer portable electronic devices, where this approach has contributed, together with the developments in other areas of electronics, to the possibility of adding several functional blocks without increasing the overall system's volume with respect to what was achievable in the past. As a consequence, this increased functionality, has led to a need of several different power rails which must supply different blocks such as CPUs, RF power amplifiers, displays, sensors and devices like cameras and lights.

Each of these blocks has very different requirements in terms of supply voltage, power, regulation and transient response. At the same time, in order to have an efficient power management which minimizes losses and parasitics, each of them requires its power supply to be as close as possible. Moreover, this increased complexity of the power management systems should have a minimum possible impact on overall system reliability and cost.

The challenges in power management mentioned above, have shifted the development of power supplies from solutions made of assembled discrete components towards solutions based on integrated power semiconductors. Initially, solutions were based on an integrated controller with external power switches, while nowadays are commonly available single power management integrated circuit (PMIC) systems which requires only few external passive components. In this evolution, integrated power electronics products, ranging from single power switches to very complex integrated power management solutions, have become one of the key market segments of many semiconductor companies and a main research topic for academic professionals working in power electronics.

When considering the miniaturization of a power converter, it is often required to maintain or increase the output power provided with previous solutions. It is often

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possible to consider a certain power density value as a target parameter to improve. Power density is given as a ratio of output power over converter volume and together with conversion efficiency is a key parameter in miniaturization. The roadmap for increasing power density is now moving from converters using single PMIC systems with external passive components to the so-called "Power Supply in Package" (PwrSiP), where the passive components are placed inside the same package of the PMIC. As a further step towards the miniaturization, the "Power Supply on Chip" (PwrSoC) [1] has passive components which are directly realized on the same die of the PMIC by means of stacking or direct monolithic integration.

For this aim, the size of passive components needs to be reduced. The principal way to reduce the size of passives is by reducing their required inductance and capacitance values which are, on a first approximation, directly proportional to the amount of energy storage required. As it will be briefly recalled in section 1.1, in order to reduce the energy storage, the switching frequencies of the new proposed power conversion solutions are increased, typically in the range from 1 MHz to 100 MHz. This increase usually provides a faster response to transients and the values of required passive components can be decreased by one or two orders of magnitude allowing new miniaturization possibilities. As drawbacks, switching losses are increasing with switching frequency requiring their careful analysis to achieve good efficiency, while implementation and control also requires additional attention.

For these reasons, the power density enhancement of DC/DC converters is driven by three main research areas which are closely related to each other. These are:

- semiconductor materials and devices;
- passive components;
- converter topologies and control.

In section 1.1 the principle behind the benefit related to the switching frequency increase will be reviewed. Sections 1.2, 1.3 and 1.4 will give additional details with respect to the main topics of the different research areas of interest mentioned above. Section 1.5 will outline the structure and aim of this dissertation.

1.1 Switching frequency increment

An ideal switching converter topology is composed of three circuital component types: switches, inductors and capacitors. Resistors are unwanted components due to their capability of dissipating real power. In order to understand how the passive components numerical values can be reduced, without modifying the input to output voltage transfer function, we can use the buck converter topology shown in Fig. 1.1 as an example. In this case, the resistor is used to model the load power absorption. The principle of operation of the most common switching converter topologies, including buck, can be found in [2] together with the techniques developed for their circuital analysis.

Briefly, the switches are alternatively turned on with a switching period:

$$T_s = \frac{1}{f_s} \tag{1.1}$$

where f_s is the switching frequency of the converter. The fraction of the period associated to the turn-on time of switch 1, connected to the input, is called duty cycle D and is defined as:

$$D = \frac{t_{on1}}{T_s}. \tag{1.2}$$

The rest of the period is associated to the turn-on time of switch 2.

This behavior produces the waveform $v_s(t)$, shown in Fig.1.1, for the voltage at the switching node. The L and C are basically a non dissipative filter used to extract the average of $v_s(t)$ on a switching period, such that the output voltage V_{out} is defined as:

$$V_{out} = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = \langle v_s \rangle_{T_s} = DV_{in}. \tag{1.3}$$

Ideally the output value is a constant voltage V_o proportional to the input voltage through a regulation set by the value of D. However, the L-C filter is not capable of completely separate the DC average of $v_s(t)$ from its frequency components and some residual ripple Δv will still be present in the output voltage V_{out}. Its dominant component is the first harmonic of the switching frequency as shown in Fig. 1.1, where its amplitude has been exaggerated to underline the phenomena.

In order to quantify the amount of residual ripple in V_{out} we can start considering the inductor current $i_L(t)$ shown in Fig. 1.1. In steady state, this current has a DC component which is set by the load absorption i_o and a ripple Δi_L given by the voltage swings seen by the inductor. For instance:

$$\Delta i_L = \frac{V_{in} - V_{out}}{L} DT_s = \left| -\frac{V_{out}}{L}(1-D)T_s \right|. \tag{1.4}$$

If we revert equation 1.4 in order to obtain the sizing of inductance value we have:

$$L = \frac{V_{in} - V_{out}}{\Delta i_L} DT_s \tag{1.5}$$

where the Δi_L typically has values in the range of 10 to 20% of the full-load output current [2] in order to maintain reasonably low peak currents through the switches and constrain losses in magnetic core inductors as we will see later on.

While the DC value of the inductor current I_o flows through the load, the triangular ripple Δi_L should ideally flow through the capacitor. Under this assumption, the capacitor current $i_C(t)$ looks like the waveform of Fig. 1.1. In steady state, during one switching period the capacitor stores and transfers the same amount of charge q for a zero net balance over the period.

Thus q, which corresponds to the grey highlighted area under $i_C(t)$ is:

$$q = C \cdot \Delta v = \frac{1}{2} \cdot \frac{\Delta i_L}{2} \cdot \frac{T_s}{2} \tag{1.6}$$

such that the output voltage ripple can be obtained as:

$$\Delta v = \frac{\Delta i_L T_s}{8C}. \tag{1.7}$$

The output ripple is reduced to zero for C which tends to infinity, thus a residual ripple will always persist. Moreover, additional ripple related to the equivalent series resistance of non-ideal capacitors should also be considered. Usually the output ripple is specified with values around few points percent with respect to V_{out}, depending on which type of load should be supplied.

Looking at equations 1.4 and 1.7 it is possible to notice how, maintaining the same specifications on Δi_L and Δv required by a specific design, the values of L and C can be reduced by increasing the switching frequency. The nominal value of the passive components can be considered, in first approximation, as linearly dependent to their geometrical size. This explains why the switching frequency increase is an important factor for converters' size miniaturization.

An interesting example related to a buck converter, showing the variation of L and C nominal values with increasing switching frequency, has been presented in [1] and is reported for completeness in Fig. 1.2. The values shown are estimated considering a basic set of specifications with $V_{in} = 5\ V$, $V_{out} = 1\ V$, $\Delta i_L = 0.3\ i_o$, $\Delta v = 0.02\ V_o$.

However, increasing the switching frequency requires cautious considerations with respect to the increment of switching losses related to switches and passives non-ideal behavior. These limits are addressed by different research areas and will be briefly reviewed in the following sections.

Still looking at equations 1.4 and 1.7 it is worth to mention that we could also reduce the values of L and C by reducing the V_{in} - V_{out} term which directly maps the voltage difference applied to inductor. Obviously, one cannot freely change the V_{in} and V_{out} in a buck converter because they are usually specifications and not design parameters, but this idea is exploited by many modified topologies as we will treat also in this thesis.

1.2 Semiconductor materials

Semiconductor devices used in converters switching at high frequencies should be capable of switching at high speed while presenting low on resistance. However, when considering a specific semiconductor technological process, these properties are inversely proportional due to the physical realization of the semiconductor devices.

The main loss contributions for a power switch are related to the presence of parasitics directly associated to their implementation. These usually cause a loss of

energy to turn on and off the switches, a loss of energy due to non-instantaneous turn on/off of the switches (current and voltage overlap at switching transitions) and phenomena of capacitive discharge [3, 4].

If we consider as an example, a MOSFET device, its drain to source on resistance R_{dson} is inversely proportional to its channel width. Once the value of R_{dson} is fixed, the conduction losses will be proportional to this value, independently of the switching frequency. In fact, it is possible to approximate the RMS value of the current as constant while increasing the switching frequency and maintaining the same ripple and power specifications.

The most straightforward way to minimize the conduction losses could seem the minimization of R_{dson} increasing the channel width. At the same time, the larger the channel width is, the higher is the parasitic capacitance seen from gate. This capacitance is often modeled as the input capacitance measured with drain and source short circuited: $C_{ISS} = C_{ds} + C_{gs}$. The charge required to charge this capacitance in order for the switch to turn on, is defined as gate charge Q_g and is directly proportional to the input capacitance. It follows that the power dissipated on gating P_g can be defined as:

$$P_g = Q_g V_{cc} f_s, \tag{1.8}$$

where V_{cc} is the driver supply voltage. The gating losses are higher when the channel width is higher, thus they directly oppose to the minimization of the switch's R_{dson}. Moreover, they increase linearly with switching frequency.

With respect to the current and voltage overlap loss contribution, which causes another part of the switching losses, we can estimate that:

$$P_{ov} = K(t_r + t_f) V_{ds} I_{ds} f_s \tag{1.9}$$

where K is a factor between 1/6 and 1/2 while t_r and t_f are the MOSFET rise and fall times [3].

With respect to the capacitive discharge of the switch output at turn on we have to consider the C_{ds} capacitance which gives:

$$P_{cap} = \frac{1}{2} C_{ds} V_{ds}^2 f_s. \tag{1.10}$$

There are different ways to minimize these contributions. A first solution is by acting on the voltages and currents applied to the switch at turn on and turn off in order to provide a “soft switching” transition. Techniques like the “zero voltage switching” (ZVS) or “zero current switching” (ZCS) aim to reduce to zero respectively the voltage or the current of the switch, by exploiting a resonance arranged within the converter passive components and some parasitic capacitance or inductance of the switches, or by properly adding passive elements. ZVS switching is preferred for the MOSFET because it aims at reducing both the overlap and capacitive discharge losses contribution. The idea of resonance is also used to reduce gate drive losses by employing resonant gate drivers.

However, as frequency is pushed higher, the previous solutions are limited by the fact that the conventional power devices (i.e. Si based devices) are approaching their performance limitations, imposed by semiconductor material properties. For this reason, a second solution for minimizing the switching losses is to use semiconductor materials which provides an improved $R_{dson} \cdot Q_g$ figure of merit with respect to silicon. This usually means also reduced input and output capacitances. As explained in [5] it is possible to define a power-frequency product of semiconductor devices. This figure of merit shows how novel structure and wide band-gap semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN) devices, achieve both low gate capacitances and resistances while maintaining low on-resistances. Their high carriers' saturated drift velocity allows a higher transition frequency with respect to Si processes (i.e. 2 times for SiC and 2.5 times for GaN considering an equal gate length) and their higher electric breakdown field (i.e. roughly 5 times higher for SiC and roughly 6 times higher for GaN) allows an higher power handling capability. Thus, they provide better high frequency performances for power applications.

As a drawback, they are nowadays emerging technologies which are significantly more expensive than Si to implement. Moreover, to the best of our knowledge, they require fabrication steps which do not allow to implement on the same die both the power switches and additional analog and digital functional blocks required for a complete PMIC. For this reason, the role of silicon is still dominant in product and research designs aiming at cost sensitive and general purpose power solutions, while new semiconductor material devices are at the moment relegated to niche markets of some specific high-end applications.

1.3 Passive components

1.3.1 Inductors

Among passives, magnetic components, both inductors and transformers, are key parts of switching converters topologies and pose a significant challenge in terms of size reduction. The switching frequencies with the potential of size reduction with respect to current converters are in the range of 1 MHz to 100 MHz [1]. Below 100 MHz it has been shown that inductors with magnetic cores are still capable of obtaining the same inductance values of an air-core inductor but requiring a smaller volume (higher inductance density) [6, 7, 8] and they can also provide advantages in terms of EMI due to magnetic flux confinement.

However, the miniaturization of magnetic components has not reported any major breakthrough in the past years leaving the power inductors as the bulkiest components in switching converters. Various geometries are actually being studied focusing on key parameters such as a high inductance value per unit area, low DC resistance for high current capability, and high Q-factor, for high efficiency [9, 10]. Toroidal cores, which provides a geometrical advantage on magnetic field confinement, due to the closure of the core and its intrinsic symmetry, are very complicated to implement with planar processes used for IC fabrication. Techniques borrowed

from micro electro-mechanical systems (MEMS) are applied for the realization of both cores and windings [11]. Among the possible geometries, shapes which differ from the toroidal one are evaluated to obtain a more favorable compatibility with planar processes [12]. Among these ideas it is worth citing racetrack inductors [13, 14], techniques exploiting wire bonding for the winding [15, 16] and techniques using spiral inductors embedded in magnetic composite materials [17].

As we anticipated, the high inductance density still requires the use of magnetic materials which provide high magnetic permeability but, at the same time, must be capable of withstanding significant currents (few to tens of Amperes for low power DC-DC point of load converters), meaning significant magnetic fields, without incurring into saturation. In order to provide the required inductance at high frequency, new magnetic materials are being studied.

A key technical problem in the study of magnetic materials suitable for the realization of miniaturized inductors is the compatibility with integrated circuit realization techniques. In fact, magnetic materials are not easy to deposit in such a way that their magnetic properties are preserved after deposition or can be steadily controlled. A main problem seems to be related to ensuring a magnetic isotropy or anisotropy of the material, depending on the required geometry and application. Deposition techniques like electroplating are used for core manufacturing but cannot guarantee a controlled anisotropy of the magnetic material. On the other hand, sputtering has shown to provide a controlled anisotropy of the manufactured core when a proper mechanical fixture is used to force an external magnetic field during the deposition [18, 19]. This allows to realize cores with better properties in terms of linearity of inductance and saturation.

Soft magnetic materials studied for the design of miniaturized power inductors and transformers present loss mechanisms related to magnetic hysteresis loop area which overall accounts for the quasi-static hysteresis and frequency-dependent eddy currents [2]. The estimation of magnetic material's losses depends much on the operating conditions of the core (i.e. applied current waveform shape, amplitude and frequency [20, 21], DC bias [22, 23], and temperature [24]) so it is important to characterize the hysteresis by investigation of these experimental parameters. Due to the high frequency of operation, new models and measurement techniques need to be developed, to characterize the magnetic materials of interest. Once these materials are correctly characterized their behavior in terms of inductance and power losses can be modeled, to find the optimal solution depending on the constraints set by the power conversion task required.

1.3.2 Capacitors

With respect to capacitors, the technology for the realization of miniaturized components working in a range up to 100 MHz and even more is already available. This development has been achieved under the drive of applications in digital electronics and RF telecommunications which require very stable capacitances capable of working at high frequency with low parasitic series inductance (ESL) and low parasitic series resistance (ESR). Ceramics are actually the most relevant dielectric material in these applications. In fact, due to the advent of new materials and multi-

layer ceramic capacitors (MLCC), in 1980's capacitors were a main drive to move from through-hole to SMD mounting techniques.

Today it is possible to recognize two different classes of ceramic capacitors, depending on their dielectric material. Class I is based on dielectrics realized with a fine granular mixture of paraelectric materials, like titanium dioxide TiO_2 , which is additivated with zinc, zirconium, niobium, magnesium, tantalum, cobalt and strontium, to improve the linearity of its characteristics [25]. This class offers the most stable capacitances while it has the lowest capacitance density. Ceramics belonging to this class are the NP0, CG and C0G for example. Class II ceramics are based on materials like barium titanate $BaTiO_3$ and suitable additives are aluminum silicate, magnesium silicate and aluminum oxide. These dielectrics have much higher permittivity than class I and therefore they have a better capacitance density. However, their permittivity is dependent on the applied field so they have capacitance values which are highly non-linear with temperature and voltage. Common materials of this class are X7R, Y5V, Z5U. Nowadays, MLCC SMD capacitors in size 1210 are available with capacitance values up to $220\ \mu F$ and $V_{Max} = 6.3\ V$[1] and, over the last few years, they already became a valid alternative to electrolytic and tantalum capacitors in applications as low voltage power supply decoupling.

However, referring to the miniaturization of power supplies, a gap in terms of capacitance density between SMD capacitors and integrated capacitors on silicon like CMOS or metal-insulator-metal (MIM) capacitors is still existing. Some PwrSiP have adopted solutions which used co-packaged SMD capacitors to provide the required decoupling to the converter, due to the fact that it is still very hard to achieve good capacitance density and low ESR and ESL for integrated capacitors without consuming much silicon area.

A promising technology is the passive integrated connective substrate (PICS) proposed by Ipdia [26, 27]. Matrices of deep pores realized on the Si surface with dry etching are used to maximize the capacitance density over area. The bottom electrode is realized with n^+ doped Si, the dielectric is a deposited layer and the top electrode is a layer of n^+ poly-silicon. The company claims[2] a capacitance density up to $2\ \mu F/mm^3$, ultra-low ESL performances which overperforms by more than *15 dB* an X7R ceramic capacitor in terms of frequency rejection [27] and very stable temperature behavior. However, even if these capacitors are realized on a Si substrate, they are realized on a separate die with respect to the rest of electronics. Moreover, even if it could be possible to consider a simultaneous fabrication with electronics on the same die, the vertical trench process required for their fabrication does not allow to place part of the circuitry under them.

Finally, as a general consideration, dielectric materials, as magnetic ones, are also limited due to their frequency dependent behavior. The dielectric constant is often modeled as a complex quantity which changes with frequency providing both

[1] March, 2015 [Online]: www.digikey.com

[2] March, 2015 [Online]: http://www.ipdia.com/index.php?page=our_products&cat_id=2

capacitance and resistive parasitic components. A higher switching frequency leads to increased losses and reduced capacitance value. In order to achieve higher frequency operation with higher efficiencies, better materials are required to reduce capacitor dissipation factor by 1/3 to 1/10 and increase capacitor energy and power densities 2 to 10 times those available today [5].

1.4 Converter topologies

Depending on the application, conventional converter topologies can provide significant limitations while moving towards higher switching frequencies and miniaturization. These limitations are related to switching and conduction losses or to the specific constraints imposed by switches and passive devices in terms of efficient behavior, maximum voltage and maximum current limitations.

For these reasons, a specific attention should be payed to converter circuital architectures, topologies and control techniques in order to develop solutions which minimizes the limitations previously mentioned. By circuital architectures it is intended the possibility of connecting several DC-DC converters of the same type or of different types in parallel or stacked in order to provide a single power conversion functionality while exploiting benefits like voltage or current sharing among the different sections. The most common example is the multiphase connection of buck converters where two or more buck converters are connected in parallel and switched with a phase difference such that their inductor currents are interleaved [28]. This allows to broaden the current load range while minimizing output current and voltage ripples due to interleaving. Parallel connections of different converters is generally used to enlarge the load range of converters with efficient behavior of the single unit limited to narrow loads [29]. In these cases, additional considerations related to the control of the different phases comes into play [30]. Other architectures are exploiting stacked connections of converter topologies in order to deal with higher input voltages in a modular way [31]. With respect to the circuital topologies of the converters and also their control techniques, a classification can be done depending on the switching frequency of the converter, where two main ranges are generically identified.

1.4.1 High frequency power conversion

Converters working in the range *1* to *30 MHz* are considered part of the high frequency (HF) power conversion. Generally speaking, these converters are usually requiring magnetic core inductors in order to achieve significant inductance density in the considered frequency range. They are usually based on Si devices and the frequency range allows a very good freedom in terms of circuital topology solutions. This freedom is mostly related to the capability of using CMOS and LDMOS devices in silicon processes for the realization of converters working with this frequency range. This allows the possibility of realizing power switches and auxiliary electronics (i.e. gate drivers, logic, error amplifiers, etc...) directly on the same silicon die greatly increasing the power density. The circuital topologies used for HF

power conversion exploits various techniques to overcome the limitations associated with power switches voltage and current ratings. Starting from the previously mentioned techniques of ZVS and ZCS, which are applied even to conventional topologies, there is strong drive towards a wide collection of new topologies aiming at solving specific limitations and, optionally, using also ZVS/ZCS. For example, voltage stacking or cascoding is adopted by connecting multiple power switches in series in order to block higher voltages using series of low voltage-rated devices which can have better $R_{dson} \cdot Q_g$ figure of merit and in general lower parasitics. Moreover, topologies made of multiple conversion stages are used to obtain a pre-regulation working at a lower frequency and a load regulation switching at higher frequency with a lower voltage swing on inductors and switches and thus reduced losses. In this direction, new topologies aiming at single-stage behavior, like the "High step-down multiphase buck", which will be treated in Chapter 2, or the "Multi-level converters" [32] results in favorable trade-offs in terms of decreasing the switching ripples, reducing the size of the filter elements, increasing the converter open-loop bandwidth, or increasing the converter efficiency.

In this frequency range, ordinary control techniques, based voltage mode or current mode controls [2] are being challenged by mixed signal control techniques. These techniques exploits digital acquisition of the output voltage to adopt a non linear control during load transients optimized to provide the minimum voltage deviation of the output [33]. This allows to reduce the current stress on components and a reduction of output passive components' sizes which can be based only on the physical limitation of the converter or even on the ripple requirements only.

1.4.2 Very high frequency power conversion

Above *30 MHz*, converters are considered part of the very high frequency (VHF) power conversion. In this frequency range, it is possible to design converters working with reduced inductance values such that air core inductors can be a main alternative in design. However, to achieve such dramatic increases in switching frequency while preserving a reasonable efficiency, it is necessary to counter the frequency dependent device loss mechanisms such as switching and gating losses. For this reason, these converters are usually implementing resonant ZVS/ZCS operation. Due to the need of limiting the gating losses and to the difficulty of implementing an high side gate driver at such high frequencies, this topologies are often based on a single ground referenced switch and the most commonly evaluated topologies are directly inspired to the Class-E power amplifier [34] although there are exceptions to this approach [35].

The principle of operation of Class-E based approach exploits the resonance between two or more passive components, usually an input choke inductor and a capacitor connected in parallel with the switch, to achieve zero voltage switching and zero current switching, by allowing switch turn-on when both its V_{ds} and dV_{ds}/dt are zero. Moreover, semiconductor device's parasitics (i.e. interconnection inductance and device capacitances) must be absorbed in this resonant circuit operation. The resonant operation requires switches rated for voltages much higher than the input voltage (i.e. around 2 to 3 times), due to the over-voltage generated by the resonant

behavior and in general the components' stress is higher than in hard switched topologies. In order to reduce this requirement, other topologies like the Class Φ_2 converter have been developed [36]. This topology use a multi-resonance operation (by adding an inductor and a capacitor) to reshape the switching node voltage waveform such that it has a lower maximum (i.e. a switch with a lower voltage rating can be used) and also reduces the sensitivity of ZVS on load.

In fact, VHF converters, due their resonant behavior, which is highly dependent on load impedance, tend to suffer from poor efficiency outside of nominal load operation. Circuital modifications or control techniques aiming at their efficient load range extension and regulation have been evaluated. A possible solution is by using an architecture composed by several parallel converters controlled with an on/off management depending on the load [29].

1.5 Thesis structure and contribution

Following the previous introduction, this thesis aims at the study and design of topologies and components for high power density DC-DC converters. It is clear that new circuital topologies can solve specific problems which arise when moving to higher switching frequencies. In order to leverage a possible integrated realization of the converter's active components on a single die we decided to focus on the use of available Si process technologies for our designs. These allow to use well established and reliable technologies sharing on the same die CMOS devices, which could be used to implement the auxiliary logic and analog circuitry, together with power devices such as lateral diffusion mosfets (LDMOS) and drain extended (DEMOS) power transistors which can be used to implement the converter's power stage.

This choice has led to the study and design of a novel integrated implementation of a four phases high step-down multiphase buck converter, which is presented in Chapter 2. At first, the performance comparison with a multiphase buck topology is recalled from previous literature contributions and expanded. This comparison underlines the benefits of the high step-down topology when moving to high step-down conversion from input to output voltage and at the same time moving to higher frequencies for power density enhancements. The main circuital design considerations and optimizations related to its integrated implementation are described. Measurement results are presented and compared against previous solutions in terms of achieved power density.

Still, considering high step-down topologies, but using indirect charge transfer, a preliminary study for a high power density stackable flyback architecture is presented in Chapter 3. As for the high step-down multiphase buck, the aim is to enhance the power density of the actual discrete components version of the converter moving to a modular architecture based on modules implementing an integrated flyback converter with co-packaged miniaturized transformer. The study has been focused on the study of literature on HF flyback converters and on the optimization of a micro-transformer which could be implemented as flyback inductor. Additional considerations have been focused on the implementation of primary side flyback

switch with commercially available discrete switches aiming at the development of a test-bench for the preliminary evaluation of transformer performances.

Due to the fact that HF converters are much dependent on magnetic core inductors performances, we have found of interest the modeling of magnetic core losses in order to improve the capability of optimizing the design of miniaturized magnetic core inductors. Chapter 4 reviews the losses contributions in magnetic core power inductors, considering their dependencies on operating conditions. Various core losses models are considered in order to obtain the most versatile model in terms of power inductors' typical current and voltage waveforms. A magnetic hysteresis model is described and its simulated results are compared against magnetic material hysteresis and losses behaviours obtained from datasheets.

As the modeling of magnetic hysteresis and its related losses requires quite a significant number of parameters and characterization, the design of an automated electronic system capable of hysteresis characterization on physical samples of magnetic materials used for HF power conversion is described in Chapter 5. Different measurements depending on frequency, temperature and magnetic field waveform are obtained focusing on the future idea of using them for modeling calibration.

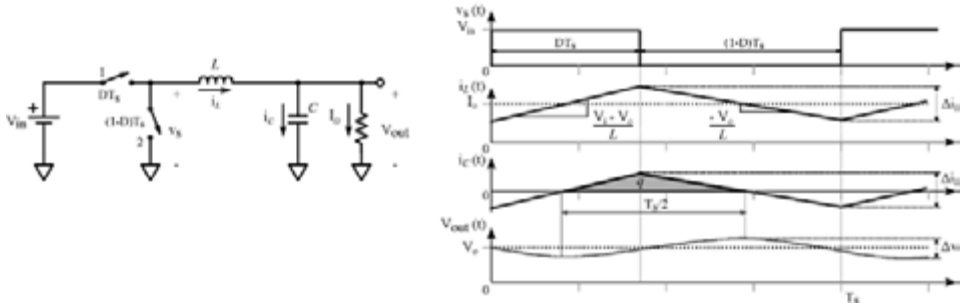

Fig. 1.1. Buck converter topology and related waveforms.

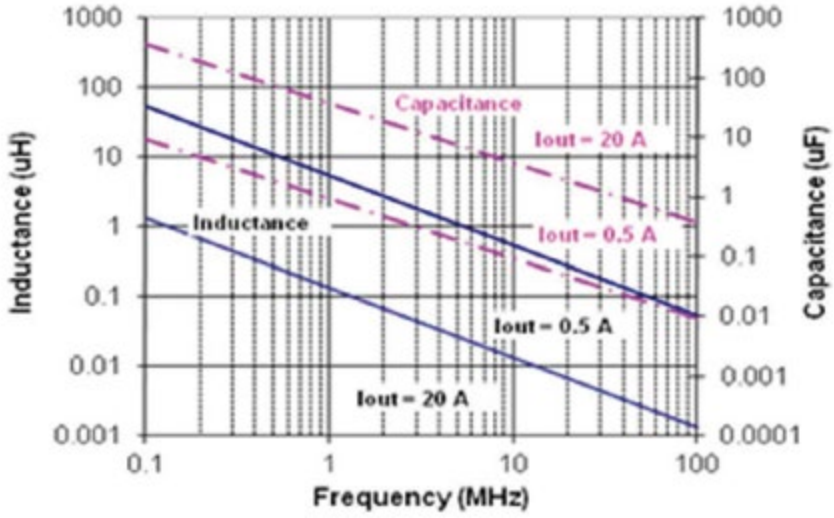

Fig. 1.2. Impact of increase in switching frequency on the relative value of passive elements for a buck converter [1].

Chapter 2
Integrated high step-down multiphase buck design

This chapter presents the design of an integrated high step-down multiphase buck converter. The design exploits the integration on a single die of a four phases high step-down power stage and drive architecture to obtain a switching frequency increase from the range of [*500 kHz*, *1 MHz*] of previously proposed solutions to a value of *10 MHz*. This provides a dramatic reduction of external passive components values and a relative increase in terms of output power density estimated taking into account the area of the converter. Moreover, the frequency increment can provide benefits in terms of dynamic behavior and output ripple reduction. In order to clarify this assumptions, the principle of operation of the high step-down multiphase buck is reviewed and the principal advantages with respect to a multiphase buck are underlined. The integrated realization allows to optimize the sizing of the power switches and to design a custom drive architecture. It also relieves the implementation burden associated with complex circuitry by minimizing parasitics related to interconnections. This advantage has been applied to design the auxiliary blocks required. Among them, a proper start-up sequence for this topology has been designed. Different values and types of commercial power inductors have been tested showing a trade-off between best power density and best efficiency.

2.1 Introduction

CPUs of actual PCs and laptops have supply voltages in the range 0.9-1.5 V and require up to several tens of Amperes when computing at full speed. They behave as highly dynamic loads with slew rates up to hundreds of $A/\mu s$ when the CPU switches from being idle to full processing. They are usually supplied by a point-of-load Voltage Regulator (VR) which directly converts power from the main power supply or battery (e.g. laptops), which provide voltages in 12-19 V range. The VR should not only be capable of working efficiently with a high step-down voltage conversion ratio, it should also provide the CPU the required current with an adequate dynamic response.

A widely adopted topology for this kind of VRs is the synchronous multiphase buck converter. This topology can provide quite large output currents, due to the multiphase architecture, and an output ripple reduction due to interleaved phase switching [37, 38]. Moreover, using switching frequencies up to hundreds of kHz per each of the n phases, a proper interleaving provides an equivalent output switch-

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ing frequency *n* times greater thus improving the transient response and reducing the output ripple. However, VRs based on multiphase bucks present some main issues. First of all, the high step-down voltage conversion requires the buck topology to work with very small duty cycles, around 10% (i.e. 1.2 V out with 12 V input) or lower. This causes a reduced range for duty, and thus output, regulation and ultimately limits the possibility of increasing the switching frequency. In fact, as the required on time of the high side switch becomes comparable with the driver rise time, duty cannot be controlled. Another issue related to the buck topology is that each switch must be rated to block the input voltage. This causes that the switches turn-on and turn-off power losses are directly proportional to the input voltage. Moreover, due to their voltage rating, the switches will usually have a worse figure of merit (FOM) than switches rated for lower voltages (e.g. higher $R_{dson} \cdot Q_g$). An additional drawback of a multiphase buck topology is related to the necessity of a current sensing technique monitoring the current balance between different phases.

In order to solve these issues, especially the limited duty cycle, two different methods have been evaluated in literature. The first one is based on a two-stage architecture where a pre-regulator stage provides a step-down conversion of the input voltage before applying it to the multiphase buck [39]. However, this method needs the introduction of many additional components, with respect to a multiphase buck, increasing the overall cost of the converter. The second method is based on maintaining a single-stage converter, trying to extend the duty cycle by means of transformers or coupled inductors [40, 41, 42]. These solutions have less additional components but are limited by the performances of the magnetics. Moreover, it is often required the design of custom magnetics, instead of using commercially available ones, increasing the cost and design time of the overall converter.

Another solution, which follows from the second method, is based on obtaining the duty cycle extension modifying the multiphase buck topology and adding capacitors instead of inductors. This solution which is referred to as “Extended-Duty Multiphase Buck” has been extensively described in [43]. A comparison with multiphase buck has been evaluated in [44] and additional characterizations of this solution for a different number of phases have been studied in [45, 46, 47] where the topology is referred as “High Step-Down Multiphase Buck”. The high step-down multiphase buck topology provides advantages, with respect to the multiphase buck topology, not only in terms of duty cycle extension but also in terms of voltage stress of the switches and automatic current balance between the different phases [45].

A reduced voltage stress of the switches, allows to use switches rated for a lower voltage. These usually have smaller parasitic capacitances and consequently can be switched faster. Moreover, their reduced voltage stress allows to reduce the switching losses of the converter. These advantages allows to increment the switching frequency of the converter which allows to decrease the size of inductors and capacitors while mitigating the increment of switching losses. In order to understand the advantages in the comparison between high step-down multiphase buck converter and standard multiphase buck converter, the operation principle of high step-down multiphase buck is recalled in section 2.2.

2.2 High step-down multiphase buck operation analysis

We will directly focus on the analysis of a four phases converter in order to have convenient notation and graphs which can be used throughout the rest of the chapter. Fig. 2.1 shows an ideal four phases high step-down buck topology. Different colors have been associated with signals related to each phase to allow an easier identification of the four phases. *HSx* labels identify the high side switches while *LSx* low side ones with *x* as the phase number. Between each phase's HS and LS switch, there are three intermediate flying capacitors C_{i1}, C_{i2} and C_{i3}, exception made for phase number *4*. For this reason, two switching nodes can be defined for the first three phases. The upper nodes of each flying capacitor are named *VNx* and the lower nodes, which correspond to the nodes connected to the inductor, are named *VLx*. As it is possible to notice, only the first phase's input is directly connected to the input voltage V_i. Other phases' inputs are connected to *VNx* node of phase *x-1*, in a kind of cascaded structure. With respect to the outputs, the inductors are connected in parallel as it happens in a standard multiphase buck to obtain a sum of their output currents with switching phase interleaving.

With four phases there are two possible switching schemes which can used for interleaving. In order to easily identify them, we can start by defining *k* as the number of non-adjacent High Side (HS) switches simultaneously turned on. Depending on which scheme is selected, we can have *k = 1, 2*. With *k = 1* we have a sequential switching of the four HS switches in a pattern 0-90°-180°-270° of phase shift between each HS logic signal. The second scheme, with *k = 2*, has a pattern which involves a switching of 2-by-2 non-adjacent HS switches in a pattern 0-180°-0-180°. A correct disoverlap must be respected between each phase HS and Low Side (LS) switches turn-ons and also between adjacent HS. The two switching schemes are analyzed in the following sections. For simplicity we will assume that each phase has the same duty cycle *D*.

2.2.1 Sequential high side switches turn-on: k=1 switching scheme

The *k = 1* switching scheme has only one HS switch turned on at a time. The logic signals necessary to control the switches in order to obtain this pattern are shown in Fig. 2.2.

As it is possible to notice, in order to keep this switching scheme, there is a constraint on maximum duty cycle:

$$D < \frac{1}{4}. \tag{2.1}$$

In order to calculate the voltage conversion ratio, we can proceed with the steady-state analysis of the converter. In order to simplify equations, we will define the voltages across flying capacitors as:

$$V_{Ci1} = VN1 - VL1; \tag{2.2}$$

$$V_{Ci2} = VN2 - VL2; \tag{2.3}$$

$$V_{Ci3} = VN3 - VL3. \tag{2.4}$$

The steady state waveforms of each of the switching nodes and currents are shown in Fig. 2.3.

There are eight different states during each switching period T_s. Instead of analyzing each different state, it is easier to analyze phase 1 over the whole period and apply similar considerations for the other phases.

HS1 is turned on for a time DT. During this phase L_1 is charged through C_{i1} with an applied voltage difference $V_{L1+} = V_i - V_{Ci1} - V_o$. Thus the current I_{L1} rises of a quantity:

$$\Delta I_{L1+} = \frac{V_i - V_{Ci1} - V_o}{L_1} DT_s, \tag{2.5}$$

with slope m_{1+}:

$$m_{1+} = \frac{V_i - V_{Ci1} - V_o}{L_1}. \tag{2.6}$$

LS1 is on for a time $(1-D)T$. L_1 is discharged on the output with an applied voltage difference $V_{L1-} = -V_o$. The current I_{L1} decreases of a quantity:

$$\Delta I_{L1-} = -\frac{V_o}{L_1}(1 - D)T_s, \tag{2.7}$$

with slope m_{1-}:

$$m_{1-} = -\frac{V_o}{L_1}. \tag{2.8}$$

By the assumption of steady state operation we have that inductor volt-second balance is constant, thus:

$$\Delta I_{L1+} = |\Delta I_{L1-}|, \tag{2.9}$$

which gives:

$$(V_i - V_{Ci1} - V_o)D = V_o(1 - D). \tag{2.10}$$

With respect to phase 2 we have a similar analysis, except for the fact that when HS2 is on we have a voltage difference on L_2 which is $V_{L2+} = V_{Ci1} - V_{Ci2} - V_o$. Consequently:

$$\Delta I_{L2+} = \frac{V_{Ci1} - V_{Ci2} - V_o}{L_2} DT_s \tag{2.11}$$

$$\Delta I_{L2-} = -\frac{V_o}{L_2}(1-D)T_s. \tag{2.12}$$

For phase 2 from volt-second balance we obtain:

$$(V_{Ci1} - V_{Ci2} - V_o)D = V_o(1-D). \tag{2.13}$$

Phase 3 gives:

$$\Delta I_{L3+} = \frac{V_{Ci2} - V_{Ci3} - V_o}{L_3} DT_s \tag{2. 14}$$

$$\Delta I_{L3-} = -\frac{V_o}{L_3}(1-D)T_s. \tag{2.15}$$

And its volt-second balance relation is:

$$(V_{Ci2} - V_{Ci3} - V_o)D = V_o(1-D). \tag{2. 16}$$

Phase 4 gives:

$$\Delta I_{L4+} = \frac{V_{Ci3} - V_o}{L_4} DT_s \tag{2.17}$$

$$\Delta I_{L4-} = -\frac{V_o}{L_4}(1-D)T_s. \tag{2.18}$$

Which provides the last volt-second balance equation:

$$(V_{Ci3} - V_o)D = V_o(1-D). \tag{2.19}$$

Combining equations 2.10, 2.13, 2.16, 2.19 we have the set:

$$\begin{cases} (V_i - V_{Ci1} - V_o)D = V_o(1-D) \\ (V_{Ci1} - V_{Ci2} - V_o)D = V_o(1-D) \\ (V_{Ci2} - V_{Ci3} - V_o)D = V_o(1-D) \\ (V_{Ci3} - V_o)D = V_o(1-D) \end{cases} \tag{2.20}$$

which can be simplified as:

$$\begin{cases} (V_i - V_{Ci1})D = V_o \\ (V_{Ci1} - V_{Ci2})D = V_o \\ (V_{Ci2} - V_{Ci3})D = V_o \\ V_{Ci3}D = V_o \end{cases} \tag{2.21}$$

and is easily solvable, giving:

$$V_{Ci1} = \frac{3}{4}V_i; \tag{2.22}$$

$$V_{Ci2} = \frac{2}{4}V_i; \tag{2.23}$$

$$V_{Ci3} = \frac{1}{4}V_i. \tag{2.24}$$

At steady state the flying capacitors are charged at a constant voltage which are fractions of V_i proportional to the number of phases. It also follows that the conversion ratio of the converter is:

$$\frac{V_o}{V_i} = \frac{D}{4} \quad with \quad D < \frac{1}{4}. \tag{2.25}$$

It is interesting to notice that, as for the conventional buck operated in CCM, the conversion ratios are completely independent from the values of the inductors. Additionally to that, also the capacitors' voltages remain independent from inductors' values. However, inductance values influence the current ripples, which depend on inductance value at their denominator. For simplicity we assume that inductors are all equal thus $L_1 = L_2 = L_3 = L_4 = L$. The positive and negative slopes m_{+x} and m_{-x} (with $x = 1, 2, 3, 4$) of the inductors' currents become all equal among the phases and can be rewritten in the form:

$$m_+ = \frac{\frac{V_i}{4} - V_o}{L}, \tag{2.26}$$

$$m_- = -\frac{V_o}{L}. \tag{2.27}$$

From this follows that the inductors' current ripples are all equal to:

$$\Delta I_L = \frac{V_o}{L}(1-D)T_s. \tag{2.28}$$

In order to compare with a multiphase buck we should express D as expressed by equation 2.25 which gives:

$$\Delta I_L = \frac{V_o}{L}\left(1-4\frac{V_o}{V_i}\right)T_s. \tag{2.29}$$

For a multiphase buck we have that $D = V_o/V_i$ so inductor's current ripple is:

$$\Delta I_{Lmb} = \frac{V_o}{L}\left(1-\frac{V_o}{V_i}\right)T_s. \tag{2.30}$$

This shows how there is a ripple reduction on each phase with respect to the multiphase buck.

If we consider the output current going to the capacitor I_{Co}, this will be:

$$I_{Co} = I_{L1} + I_{L2} + I_{L3} + I_{L4}. \tag{2.31}$$

Its ripple is the output capacitor ripple ΔI_{Co} while the DC value is the current flowing to the load I_o. The capacitor current ripple can be evaluated by considering that, at steady state, it will have a period of $T_s/4$. From Fig. 2.3 it is easy to notice that with $DT_s \leq t < T_s/4$ the currents on the four phases have the same slope m_-, thus:

$$\Delta I_{Co} = 4|m_-|\left(\frac{1}{4}-D\right)T_s = \frac{V_o}{L}(1-4D)T_s. \tag{2.32}$$

Still considering the substitution of D we have:

$$\Delta I_{Co} = \frac{V_o}{L}\left(1-16\frac{V_o}{V_i}\right)T_s. \tag{2.33}$$

While a four phases multiphase buck with the same interleaving would have:

$$\Delta I_{Co\ mb} = \frac{V_o}{L}\left(1-4\frac{V_o}{V_i}\right)T_s. \tag{2.34}$$

The $k = 1$ switching scheme provides a very high step-down from input to output. The duty cycle of the switches is extended with respect to the standard multiphase buck by a factor of four. However this imposes a limit on the maximum output voltage which is obtained for $D_{max} = 1/4$ and is:

$$V_{o\ max} = \frac{V_i}{16}. \tag{2.35}$$

With $V_i = [10, 16]$ V, it provides $V_{o\ max} = [0.625, 1]$ V which is quite low for actual power supply values. For this reason $k = 2$ has been analyzed, too.

2.2.2 Two-by-two high side switches turn-on: k=2 switching scheme

This scheme provides an additional duty cycle extension with respect to standard multiphase buck and also with respect to the *k = 1* switching scheme. In this case the HS switches are turned on in couples, HS1 and HS3 together, then the other two. Fig. 2.4 shows the required logic signals.
In this case, the constraint on the duty is relaxed to:

$$D < \frac{1}{2}. \tag{2.36}$$

The steady state waveforms of each of the switching nodes and currents are shown in Fig. 2.5.

Following a steady state analysis similar to the one treated in subsection 2.2.1 it is possible to obtain the same flying capacitors' voltages of equations 2.22, 2.23, 2.24 also for this switching scheme. The conversion ratio is the same, but with the relaxed constraint on duty:

$$\frac{V_o}{V_i} = \frac{D}{4} \quad with \quad D < \frac{1}{2}. \tag{2.37}$$

Under the same assumptions, we obtain m_+ and m_- equal to the *k = 1* analysis. The current ripples on each inductor are still equal to equation 2.29. However, with respect to the output capacitor ripple there are some differences related to the different interleaving of the currents.

Considering the interval of I_{Co} in Fig. 2.5, with $DT_s \leq t < T_s/2$ all the inductor currents are assuming a negative slope, thus:

$$\Delta I_{Co} = 4|m_-|\left(\frac{1}{2} - D\right)T_s = \frac{V_o}{L}(2 - 4D)T_s. \tag{2.38}$$

Which, with the substitution of *D* comes out to be:

$$\Delta I_{Co} = \frac{V_o}{L}\left(2 - 16\frac{V_o}{V_i}\right)T_s. \tag{2.39}$$

A multiphase buck with same interleaving would have:

$$\Delta I_{Co\ mb} = \frac{V_o}{L}\left(2 - 4\frac{V_o}{V_i}\right)T_s. \tag{2.40}$$

So there is still a reduction of the capacitor ripple, but less than for the *k = 1* case. Nevertheless, this time the maximum output voltage is:

$$V_{o\ max} = \frac{V_i}{8} \tag{2.41}$$

giving $V_{o\ max}$ = [*1.25, 2*] *V* with V_i = [*10, 16*] *V*.

This switching scheme sacrifices part of the ripple reduction in order to obtain an additional duty cycle extension and higher $V_{o\ max}$ which can be more useful in practical applications.

2.3 Comparison with multiphase buck

Different characteristics need to be evaluated in order to define a comparison between high step-down multiphase buck and standard multiphase buck. These different aspects have already been presented in the cited literature describing discrete implementations of the high step-down topology. Table 2.1 collects these aspects considering also the two possible switching schemes. Due to the similarity of these topologies with the single phase buck architecture, we will report the same parameters evaluated also for the buck. This gives an easily understandable comparison with a widely known topology. Each parameter is presented considering a generic number *n* of phases.

The conversion ratio V_o/V_i proves the duty cycle extension between the high step-down topology and the standard buck topologies. This advantage, as we already introduced, is mostly based on the reduced voltage swing of the inductors.

Additionally, this provides a reduced blocking voltage of the switches, reported in Table 2.1 as $V_{ds\ max}$. Both HS and LS switches are blocking reduced voltages with respect to the single and multiphase buck's switches. The $V_{ds\ max}$ of each switch can be obtained from Fig. 2.3 and Fig. 2.5 considering the differential voltages on each switch. The resulting waveforms are shown in Fig.2.6. As it is possible to notice, even if the HS switches have $V_{ds\ max} = V_i/2$, each switch is turned on and off on a $V_{ds\ on/off} = V_i/4$. This allows to reduce the switching losses with the high step-down topology.

The reduced inductor's voltage swing provides also a reduction of inductor's current ripple ΔI_L with the high step-down topology. A smaller inductance value, thus a smaller inductor, can be used in order to obtain the same requirement on ripple or the same inductor can be used with a lower current ripple, providing reduced core losses.

An additional benefit of inductor ripple reduction can be seen on output capacitor ripple ΔI_{Co}. In this case, also the multiphase buck can provide an advantage on the single phase buck due to phase interleaving. Nevertheless, the high step-down topology provides an even increased ripple reduction. This reduction, as we already demonstrated above, is maximized with $k = 1$ switching scheme. A reduction of the output capacitor's current ripple allows to obtain an output voltage ripple inside the requirements using a smaller capacitance value which often implies using a smaller sized capacitor.

An interesting advantage of the high step-down topology is related to the automatic balance of the inductors' currents. This is directly related to the presence of the capacitors C_{ix}. Fig. 2.7 shows the three C_{ix} capacitors' currents over a switching period. Assuming different duty cycles for each of the phases, the steady state charge balance of C_{ix} capacitors over a switching period must be zero. Thus:

$$Q_{1\,avg} = (D_1 I_{L1} - D_2 I_{L2}) T_s = 0 \tag{2.42}$$

$$Q_{2\,avg} = (D_2 I_{L2} - D_3 I_{L3}) T_s = 0 \tag{2.43}$$

$$Q_{3\,avg} = (D_3 I_{L3} - D_4 I_{L4}) T_s = 0 \tag{2.44}$$

These equations can be combined to obtain the relation shown in Table 2.1:

$$I_{L1} D_1 = I_{L2} D_2 = I_{L3} D_3 = I_{L4} D_4. \tag{2.45}$$

This means that the imbalance of currents is almost removed without any additional sensing requirements. To the extent that each phase is controlled with the same duty cycle, the four currents are equal.

The inductor's current maximum slew rate, max di_L/dt, is a parameter which directly helps to compare the transient response of the topologies when a load current step occurs. In this case, on a heavy to light load step, the high step-down topology has the same slew rate as the buck ones as shown in Table 2.1.
However, when a light to heavy load step occurs, the reduced voltage excursion applied to the inductor and the limited maximum duty cycle of the high step-down converter, limit its maximum slew rate to the values shown in Table 2.1. These values can be obtained considering that the maximum duty cycle D_{max} limit allows to have a maximum slew rate over a switching period which is limited to:

$$\max \left. \frac{di_L}{dt} \right|_{L \to H} = \frac{\frac{\frac{V_i}{n} - V_o}{L} D_{max} T_s - \frac{V_o}{L} (1 - D_{max}) T_s}{T_s} = \frac{\frac{V_i}{n} D_{max} - V_o}{L}. \tag{2.46}$$

This comparison seems to be quite unfavourable for the high step-down. However, we have to consider that it is done assuming the same inductance value and switching period. As explained above, the advantages given by reduced switching losses and ripple reduction allow to relieve this condition by increasing the switching frequency and at the same time reduce the inductance value. This solution is the one followed in this work. An additional way to improve the transient response is by using coupled inductors as shown in [47]. This way the leakage inductance of the coupled inductors determines the slew rate during load variations, while the ripple reduction is determined by the coupled inductance. A detailed study on the benefit of coupling the inductors in multiphase buck is presented in Appendix A.

Another trade-off is set by the conduction losses related to the switches. If we consider the multiphase buck, this will have *n* times the conduction losses of the buck, as reported in table 2.1. However, if we consider the high step-down buck, we have an additional contribution of loss. This is related to the fact that the LS switches of the first *n-1* phases are conducting also on next phase's HS on time. This is sketched in Fig. 2.8.

Table 2.1 Comparison of different aspects between buck, multiphase buck and high step-down multiphase buck circuital topologies.

	Buck	Multiphase Buck		High step-down multiphase buck	
		$k=1$	$k=2$	$k=1$	$k=2$
$\frac{V_o}{V_i}$	D	D		$\frac{D}{n}, D<\frac{1}{n}$	$\frac{D}{n}, D<\frac{1}{2}$
$V_{ds\ max}$	V_i	V_i		$HS: \frac{2V_i}{n}, LS: \frac{V_i}{n}$	
$V_{ds\ on/off}$	V_i	V_i		$\frac{V_i}{n}$	
ΔI_L	$\frac{V_o}{L}\left(1-\frac{V_o}{V_i}\right)T_s$	$\frac{V_o}{L}\left(1-\frac{V_o}{V_i}\right)T_s$		$\frac{V_o}{L}\left(1-n\frac{V_o}{V_i}\right)T_s$	
ΔI_{C_o}	$\frac{V_o}{L}\left(1-\frac{V_o}{V_i}\right)T_s$	$\frac{V_o}{L}\left(1-n\frac{V_o}{V_i}\right)T_s$	$\frac{V_o}{L}\left(\frac{n}{2}-n\frac{V_o}{V_i}\right)T_s$	$\frac{V_o}{L}\left(1-n^2\frac{V_o}{V_i}\right)T_s$	$\frac{V_o}{L}\left(\frac{n}{2}-n^2\frac{V_o}{V_i}\right)T_s$
Phases' currents auto-balance	-	No		Yes, with: $I_{L1}D_1 = I_{L2}D_2 = I_{L3}D_3 = I_{L4}D_4$	
$\max\frac{di_L}{dt}\Big\vert_{H\to L}$	$-\frac{V_o}{L}$	$-\frac{V_o}{L}$		$-\frac{V_o}{L}$	
$\max\frac{di_L}{dt}\Big\vert_{L\to H}$	$\frac{V_i-V_o}{L}$	$\frac{V_i-V_o}{L}$		$\frac{\frac{V_i}{n^2}-V_o}{L}$	$\frac{\frac{V_i}{2n}-V_o}{L}$
Switches' conduction losses	$R_{HS}I^2_{HS\,rms} + R_{LS}I^2_{LS\,rms}$	$n(R_{HS}I^2_{HS\,rms} + R_{LS}I^2_{LS\,rms})$		$n(R_{HS}I^2_{HS\,rms} + R_{LS}I^2_{LS\,rms}) + (n-1)R_{LS}I^2_{HS\,rms}$	
Additional constraints	-	-		$f_s \gg \frac{1}{2\pi\sqrt{L_x C_{ix}}}$	
Passive components	L, C_o	nL, nC_o		$nL, nC_o, (n-1)C_{ix}$	

In [46] the conduction losses of the switches have been estimated approximating the inductor ripple to zero. However, this approximation is very strong, especially in our case where the output power and inductance values will assume much lower values. For this reason, we can estimate RMS current over the switches considering their effective current waveform shape which is similar to the trapezoidal pulse shown in Fig. 2.9. From this we can generically obtain that:

$$i|_{RMS} = \lim_{T_s\to\infty}\sqrt{\frac{1}{T_s}\int_0^{T_s} i^2(t)dt} = \sqrt{D}\sqrt{\frac{(b-a)^2}{3} + a(b-a) + a^2}. \tag{2.47}$$

This formula can be generalized to both HS and LS currents contributions. In fact we write it as:

$$I_{x\,RMS} = \sqrt{\delta}\sqrt{\frac{\Delta I_L{}^2}{3} + I_{L\,min}\,\Delta I_L + I_{L\,min}{}^2} \tag{2.48}$$

where $\delta = D$ for the HS switches and $\delta = 1\text{-}D$ for LS ones.

Exploiting the voltage stress reduction of the high step-down switches with lower breakdown voltage can be used. These are generally providing a better $R_{ds\,on}{\cdot}Q_g$ figure of merit so the increased conduction losses can be minimized. Considering an integrated implementation this effect can also be optimized by a proper sizing of the switches, in order to trade-off their conduction and switching losses.

An additional constraint which should be verified with the high step-down converter is related to the constant voltage on the flying capacitors. In order to maintain this assumption it is important that the resonance frequency between flying capacitor and power inductor is at a frequency much lower that the switching one, thus:

$$f_s \gg \frac{1}{2\pi\sqrt{L_x C_{ix}}}. \tag{2.49}$$

In conclusion, in terms of part count, the high step-down requires *n-1* additional capacitors with respect to the multiphase. Compared to other high step-down solutions proposed which involved multi-tap inductors, transformers or additional switched capacitors pre-regulators stages, this doesn't seem to be a major issue.

2.4 Functional overview of the implemented converter

The requirements for the designed converter have been obtained aiming to an improvement of existing commercial solutions for low power point-of-load regulators supplying loads under *2 V* with a power under *10 W* by converting directly from voltages in *12 V* rail range. Generally speaking, actual solutions are single-chip modules with external passives or PwrSiP based on single or multiphase buck topologies which are used with a small duty cycle in order to achieve the low output voltage. This operating condition is not in their optimal working point. As it can be noticed from the efficiency curves in their datasheets, these solutions present the lower efficiency when working with low output voltages. This is related to the fact that they are subject to the same switching losses they have when working with higher output voltages, but transferring lower output power. In order to provide a reasonable amount of switching losses, their switching frequency is usually in between *250 kHz* and *1 MHz*. This frequency range often requires inductors ranging in *2.2 ÷ 10 μH* which are usually the bulkier component of the converter. For this reason they can achieve overall footprints around *10 × 15 mm* but with thicknesses severely limited by the inductors and ranging around *3 ÷ 6 mm*. As an example, low profile applications (e.g. servers and rack modules) can potentially tolerate quite larger PCB area (i.e. one smaller inductor plus 2 to 4 more capacitors) but may have a

hard stop in terms of maximum height, which is meant to comply with the use of bulky inductors.

Following these considerations, the high step-down multiphase buck seems a good candidate for the improvement. The choice of a four phases architecture, together with maintaining the two possible switching schemes, gives a trade-off between the desired high step-down conversion ratios and the duty cycle extension. As far as the author knows, at the time of writing, this is the first attempt to completely integrate a four phases version of the high step-down multiphase buck. For this reason, we have decided to focus on an implementation which could provide both a demonstration in terms of power density increment within this specific application but also a testing of custom design solutions required for various functions. The requirements followed for the converter design are reported in Table 2.2.

Table 2.2 Implemented converter requirements.

Parameter	Requirement
V_i	[*10.8*, *16*] *V*
V_o	*1.2 V* nominal, range [*0.6*, *2*] *V*
I_o	*2 A* maximum
f_s	*10 MHz* nominal, up to *15 MHz*

The increment of switching frequency by an order of magnitude allows a reduction of the inductance and capacitors values. Moreover, by using a multiphase approach, conduction losses are divided among the four phases which can be rated for a quarter of the output current. This allows to use switches which are both smaller and rated for a smaller voltage.

Fig. 2.10 shows the architecture which has been implemented. All the active components, including power stage switches, drive architecture and logic are integrated on the same silicon die providing maximum flexibility in terms of placement, sizing, interconnection of blocks and parasitics reduction. The converter is implemented in open loop and without an internal clock generator. This choice has been adopted in order to simplify the design and to provide maximum test flexibility (i.e. multiple switching frequencies) without having to design a wide band oscillator on chip. For these reasons it requires the following four signals as external inputs:

- Clock: an AC coupled analog signal which is used as timing reference to generate the switches' control signals;
- Mode: a digital flag signal which is used to select among the two different switching schemes;

- Duty: a DC coupled analog signal which serves as duty cycle ratio value input;
- PWM slope: a current bias which is used to adjust the slope of the voltage ramp used in the internal PWM generator. The ramp slope must be varied depending on the switching scheme.

The logic block is composed by a start-up logic and a steady state logic. The start-up logic manages the start-up pre-charge of the power stage flying capacitors C_{ix}, with a procedure based on the sensing of the power stage nodes. The steady state logic provides the proper switching signals depending on the selected mode and duty cycle.

The silicon die has been designed in a Texas Instruments BCD proprietary Si technology process designed for analog, mixed signal and power applications which includes: Power MOSFETs or various voltage ratings realized both with Drain-Extended (DE) technology and Lateral Diffusion (LD) technology, BJTs and a $0.7\ \mu m$ 5 V CMOS logic family. Fig. 2.11 shows the IC layout with functional areas highlighted. The overall die area is $3.4mm \times 2.4mm$.

The die is packaged in a 24 pins Leadless Leadframe Package (LLP) [48] which has been selected in order to minimize bonding and lead inductance. Moreover, this package has a ground referenced thermal pad which allows reduced thermal resistance for heat dissipation. The package sizes are shown in Fig. 2.12.

Fig. 2.13 shows a micro-photography done after the wire bonding of the die to the lead frame. Double bonding has been applied to pins requiring low parasitic resistance and inductance like the power stage nodes, V_i and GND connections. The wire bonding has been done using copper wire which provides a better conductivity than gold wire bonding. The top-level metal, which has been used to route the supplies and power signals has also been realized with thick copper technology to minimize parasitic resistance.

The passive components required for completing the converter topology are placed externally. The additional components required are: input capacitor C_i, four inductors L_x, three capacitors C_{ix}, output capacitor C_o.

2.4.1 Passive components sizing

The sizing of passive components underlines the reduction of their values introduced by the high switching frequency. The sizing of power inductors has been done considering a single inductor size not exceeding a maximum size of $6 \times 6\ mm^2$ footprint and a thickness below $5\ mm$. For this reason we have decided to keep $L \leq 1\ \mu H$ which is an achievable result with common technologies for miniaturized inductors. Minimum inductance has been set to $L \geq 100nH$ thus limiting the current ripple per each phase to a maximum of $1\ A$ peak to peak.

Input and output capacitors are sized following a specification of less than $5\ \%$ voltage ripple respectively with minimum $V_i = 10.8\ V$ and $V_o = 0.9V$ giving $C_{in} \geq 1\ \mu F$ and $C_{out} \geq 150\ nF$. With respect to output capacitor, we can add a constraint considering the additional output capacitance necessary to limit the output transient over-voltage due to a current step on the load. Considering a maximum inductance per phase of $L = 1\ \mu H$ with a $10\ \%$ over-voltage on minimum V_o we obtain $C_{out} \geq 47$

μF. Due to the fact that the actual converter is not provided of a feedback control, this constraint could initially be omitted. However, we decided to take it into account for a more realistic analysis of converter start-up.

With respect to the additional capacitors C_{i1}, C_{i2} and C_{i3}, the sizing is obtained considering that at regime switching they must charge to constant voltages which are respectively $¾\ V_i$, $½\ V_i$ and $¼\ V_i$. This condition is verified if the switching frequency f_s is much higher than the resonant frequency $f_r = 1/2\pi\sqrt{LC_i}$ between each C_i and the inductor L. Then, with $f_s = 10\ MHz$, we can assume a maximum $f_r = 2\ MHz$. Assuming $L = 100\ nH$, we obtain $C_i \geq 63\ nF$. This minimum value, together with the fact that the capacitors must withstand a voltage of at least 12 V (i.e. $¾\ V_i$ with $V_i = 16\ V$), makes their integration on silicon unfeasible for actual design technology used.

2.5 Power stage

As already explained, with both switching schemes HS and LS switches V_{ds} are respectively subject to the same voltage excursions. With four phases topology, HS switches must only block up to $V_i/2$, while LS only up to $V_i/4$. Thus, with respect to a multiphase buck converter, where both HS and LS switches must block up to V_i, the blocking voltages are reduced and switches with lower voltage rating can be used. In this case a $9\ V$ rating LDMOS N-type switch has been chosen, among the ones available within the selected process, both for HS and LS design. This choice gives a good margin on the $16\ V$ upper limit on V_i. It also allows a more compact layout of the power stage switches with respect to a $16\ V$ rated switch which has a larger layout required to provide higher voltage insulation. For the LS implementation a switch with a lower voltage rating could be used (e.g. a $5\ V$ NMOS). However, within the chosen technology, the $9\ V$ LDMOS is the power switch with the lowest voltage rating. An alternative solution could have been the $5\ V$ NMOS device but it is not specifically designed for power applications.

Using only N-type switches, instead of complementary solutions, allows to spare area on the HS switches while achieving the same on resistance R_{DSon}. Another advantage comes from a reduction of gate charge Q_g needed to turn on the switch.

The sizes of the HS and LS switches have been chosen aiming at the optimization of overall efficiency for an operating condition centered on nominal requirements and $k = 2$. The procedure followed is explained in subsection 2.9.2. The result obtained has shown an optimum with LS area three times the HS one, or $R_{DSonLS} = R_{DSonHS}/3$. For instance, with a $V_{GS} = 3\ V$, the simulated results of the channel resistances are: $R_{DSonLS} = 66\ m\Omega$, $R_{DSonHS} = 198\ m\Omega$. This result is in accordance with the fact that with this topology LS switches are subject to increased conduction losses with respect to HS ones.

2.5.1 Layout

The layout of the power stage switches has been designed with the effort of minimizing the parasitic series resistance and inductance added by top metal layer

interconnections and bonding wires. In order to maintain the external passive components of the power stage the closest possible to the power stage pins (VN1, VN2, VN3, VL1, VL2, VL3, VL4), these are all placed on the same side of the package. Fig. 2.14 shows a close-up on the power stage layout area. The power switches are highlighted in order to show the peculiar HS and LS switches arrangement. The interconnection between the power switches is realized with the 5th metal layer (which is white colored in the layout) with the HS switches located closer to the die border and LS switches strictly behind them. This way, the connections between different HS (i.e. VN1, VN2, VN3) are close to the pad ring of the chip. At the same time, LS have sources connected to a common ground distribution path and drains (i.e. VL1, VL2, VL3, VL4) are brought to the pad ring by passing over the HS switches. The remaining gap areas are used to place the gate drivers' final sections as close as possible to the switch they need to drive. More details on the drive architecture layout are explained in section 2.6.

2.5.2 High side's switches source and drain connections design

As the HS switches have the LS drain connection routed on top of them, there is little overlap to realize their drain and source contacts in top metal. This has a detrimental effect on the increment of the drain to source resistance due to layout. Moreover, due to the arrangement of the fingers composing the switch, it is necessary to have a transition from an horizontal interconnection to a vertical one. Fig. 15 shows the tapering of the different metal layers, highlighting the source and drain connections. This structure has been designed following the results of a 3D simulation of the distribution of currents.

A previous solution, with MET3 and MET4 simply replying the MET2 pattern showed that the current density crossing MET3 and MET4 layers tended to be maximum in the areas directly overlapped (and thus contacted) by the MET5 while the rest of the length was conducting very small current but subtracting contact area useful to the other connection.

This layout solution provided an $R_{DSonHS}|_{layout} = 226.4\ m\Omega$ with $V_{GS} = 3\ V$ obtained with parasitic extractor simulation. This layout had an increment of *14.3 %* with respect to channel resistance R_{DSonHS}.

For this reason the structure gradually transitioning from MET5 to MET2 patterns, shown in Fig. 15.a has been adopted. In this case $R_{DSonHS}|_{layout} = 215.2\ m\Omega$ with an increment of *8.7 %* on channel resistance. This has also provided the current distributions shown in Fig. 15.b which tend to be uniform on each metal layer.

2.6 Drive architecture

The implemented power stage is a full LDMOS N-type switches architecture. With respect to P-type HS switches, these are smaller for the same R_{DSon} so less drive power is needed, less area is occupied on chip and they present less parasitic capacitance. However, this makes the drive architecture requirements more complicated, due to the fact that the turn-on of a N-MOS type HS1 needs a gate voltage

higher than V_i. Moreover, the high step-down topology has a particular configuration of the HS switches which are all working on different voltage domains as it is possible to notice from Fig. 2.3 and Fig. 2.5 observing their drain and source voltage waveforms (i.e. proper *VNx* and *VLx* nodes).

A possible solution for the HS drive architecture has been introduced in [46] for the three phases high step-down converter and it is shown in Fig. 2.16. It exploits a cascading of bootstrap stages with source-referenced HS drivers.

This solution, which is meant to be realized with discrete components, presents some main limitations. First of all, it requires an independent supply, V_{dr} at a voltage lower than V_i which is used to recharge the bootstrap capacitors. In case of an autonomous voltage conversion system, V_{dr} must be obtained from V_i (e.g. using a linear regulator) which is a quite inefficient solution. Additionally, the diodes cause a forward voltage V_f drop which sums up through the bootstrap drivers such that the higher their voltage domain is lifted from ground, the less they are recharged. More precisely, C_3 will be recharged at V_{dr} - V_f, while C_2 can only be recharged at V_{dr} - $2V_f$ and so on. It is easy to notice how the problem is even worse with a four phases solution. Lastly, the diodes must have a breakdown voltage higher than $2V_i/n$.

Exploiting the flexibility given by integration, there is room for improving this solution following some general requirements. These are:

- avoid the use of a linearly regulated V_{dr} source at a voltage lower than V_i;
- exploit the possibility of doing charge recycling among the different turn on and turn off events;
- integrate on-chip all the components required for the drive architecture (e.g. bootstrap capacitors).

The following subsections will describe the designed solution focusing on its behaviour and sub-parts description.

2.6.1 Architecture overview

The introduced drive architecture is shown in Fig. 2.17. It has been implemented using only $0.7\ \mu m$ 5V CMOS devices. It receives as inputs the logic signals which control the turn-on and turn-off of HS and LS switches. More precisely, "VHSx_logic" are the logic control signals of HS switches, while "VLSx_logic" are the logic control signals of LS ones.

The capacitive voltage divider formed by the four C_{div} capacitors provides four constant voltages used as references to generate the different drive signals. At steady state, the voltage divider values are $V_{driveLS} = ¼V_i$, $V_3 = ½V_i$ and $V_2 = ¾V_i$. The capacitive divider works as a charge storage system which supplies the charge required from a certain voltage domain for a switch turn-on. It also recovers the turn-off charge which is stored back at a lower voltage. This way the charge can be recycled for multiple turn-on events before it reaches ground. The drive power required for each turn-on is absorbed from V_i and from each capacitor divider's node without the need of any additional linear voltage regulation. Due to the fact that the power absorptions from the different divider voltages are different, even with charge recov-

ery, the voltages would drift from being quarters of V_i. To avoid this drift and keep the voltages stable a refresh architecture has been designed as explained in subsection 2.6.4. The capacitive divider's voltage nodes are available outside of the chip for inspection purposes as it can be seen from Fig. 2.11. However, four $C_{div} = 2.4\ nF$ capacitors, realized by stacking MOS and Metal-Insulator-Metal (MIM) capacitances in order to increase the capacitance density over area, are directly integrated on-chip providing the necessary amount of capacitance.

In order to explain the behavior of the drive architecture, let's start analyzing the HS drivers. The VHS2, VHS3 and VHS4 gate voltages are generated using subsections of the drive architecture composed by three dedicated drive chains each. The tapering of these chains and additional details on the drive subsections are described in subsection 2.6.2. The drive chains of a specific subsection receive as input the same logic signal. The simultaneous commutation of the chains in a drive subsection allows an equivalent voltage excursion of $½V_i$ on the gate nodes of the HS switches. The theoretical gate voltage waveforms, referenced to ground potential, provided by the drive architecture are shown in Fig. 2.18 for $k = 1$ and in Fig. 2.19 for $k = 2$.

As shown in Fig. 2.17, the gate voltages are not source referenced. For this reason, in order to obtain the equivalent V_{gs} applied to the HS switches, the difference between the *VHSx* gate node voltage and *VNx* (or *VLx* for switch HS4) source node voltage must be considered. Considering the power stage waveforms of Fig. 2.3 and Fig. 2.5 it can be derived the following relationship:

$$V_{gs\ HSx} = VHSx - VNx = \begin{cases} 0 & for\ VHSx\_logic = '0' \\ \dfrac{V_i}{4} & for\ VHSx\_logic = '1' \end{cases} \tag{2.50}$$

while for HS4 it becomes:

$$V_{gs\ HS4} = VHS4 - VL4 = \begin{cases} 0 & for\ VHS4\_logic = '0' \\ \dfrac{V_i}{4} & for\ VHS4\_logic = '1' \end{cases}. \tag{2.51}$$

These excursions of $V_{gs} = V_i/4$ allow the correct turn-on and turn-off of the corresponding HS switches. With respect to VHS1, a bootstrap architecture is needed to respect equation 2.50 and allow a proper turn-on. In this case, the on-chip bootstrap capacitor $C_b = 1\ nF$ is recharged through a PMOS switch which is turned on following the corresponding LS switch logic signal. This way, a proper disoverlap between bootstrap recharge and drive operation is ensured.

LS drivers are standard source-referenced drivers. They are supplied by the node $V_{driveLS}$ which is also used as supply voltage for the logic blocks. This solution allows to avoid draining power from an auxiliary internal linear voltage regulator which has a less efficient power conversion. As an additional advantage, being the

logic and the different subsections of the drive architecture supplied by equal fractions of the input voltage, as the input voltage changes the voltage supply of every section changes proportionally, allowing the propagation delays to drift uniformly.

As a drawback, the switches' V_{gs} are proportional to V_i, too. This causes a higher R_{dson} for lower input voltages. However, the switching losses move in the opposite direction, being lower for lower input voltages and are balancing this effect. A custom level shifter architecture, introduced in subsection 2.6.3, is used to provide a proper voltage translation of the logic signals from the $[0, V_{driveLS}]$ voltage domain to the domain corresponding to the supply rails of each drive chain. As shown in Fig. 2.17, the level shifters have been placed also on LS drive chains. Here the voltage translation is not required, but their inclusion allows to equalize the delays with respect to HS drivers. This helps in preserving the disoverlaps between the logic signals set by the logic block.

2.6.2 Driver sections "selective" tapering

Considering Fig. 2.17, each of the drive chains is tapered in size following a "fan-out of four" (FO4) tapering rule [49] which starts from a technology minimum sized inverter with balanced high-to-low and low-to-high drive strengths. The chains directly connected to the gates of power switches are inverters with a size increasing by four times per each stage from the minimum sized inverter up to the optimal buffer size required to switch the power transistor. They are referred to as "Balanced High" (BH) and "Balanced Low" (BL) labels in Fig. 2.17, depending on whether they are driving an HS switch or a LS switch. The optimal size of BH and BL drive chains has been evaluated with a Cadence Analog Design Environment (ADE) multi-parametric analysis taking into account a maximization of converter efficiency as a function of the size of the drive chains as multiples of the minimum inverter. This optimization is explained in subsection 2.9.2. The remaining drive chains present in the HS drive architecture (i.e. the ones labeled as SP and SN in Fig. 2.17) could simply be instances of the BH type. However, this would cause a non-optimal usage of the available silicon area making them larger than what it is actually required. In fact, depending on the topology of the drive architecture, it is possible to "selectively" reduce the drive strength of some of the drive chains by properly reducing the sizes of their inverters. This ultimately reduces their area occupation.

The evaluation of drive strength reduction has been done considering the average flow of currents during operation. This has been done with a steady state simulation over few switching periods of the HS drive architecture section including HS2 and HS4 drivers. This has been done to assume a regular topological pattern and to exclude the bootstrap from computation. All the instanced drive chains are of the BH type. Using nominal conditions of $k = 2$, $V_i = 12\ V$, $C_{div} = 2.4\ nF$ and $f_s = 10\ MHz$ the currents at each instance terminal have been evaluated as an average over a switching period. Fig. 2.20 shows the obtained values per each terminal.

Moreover, the sinked (i_p) and sourced (i_n) currents from the supply terminals of the BH drivers connected to the gates of the power switches are balanced as expected. Conversely, there is a strong imbalance between the terminals of each of the drive chains directly connected to the capacitive divider. For this reason we assumed

the lowest average current ratio among each drive chain supplying BH drivers connected to the HS switches. The selected ratios are $\alpha_4 = i_{p4}/i_{n4} \approx 3.4$ for top side drive chains and $\beta_6 = i_{p6}/i_{n6} \approx 0.23$ for bottom side drive chains. The top side drive chains, referred as "Strong P" (SP) in Fig. 2.17, have the width of the N-MOS transistor of the final inverter divided by a factor α_4 with respect to the same transistor of BH buffer while the P-MOS maintains the same size of the BH one. Consequently, the load seen by the previous inverters of the chain is reduced and they can be re-sized still maintaining an FO4 tapering. With respect to the bottom side chain, referred as "Strong N" (SN) in Fig. 2.17, the P-MOS transistor width is multiplied by a factor β_6 maintaining N-MOS sized as in BH buffer. The four tapered buffer types BH, BL, SP, SN have an equal number of stages (i.e. 6) each to minimize the propagation delay discrepancies and ensure the conservation of disoverlaps provided by the logic block. A test bench of the "all-BH" type chains versus the one obtained as explained has shown comparable delays in ranges of hundreds of picoseconds, which we assumed negligible, so the re-sized drive chains have been preferred.

With respect to the HS1 bootstrap, we used two BH type buffers as shown in Fig. 2.17. In fact the buffer connected to the capacitive divider must source and sink the whole gate current of HS1.

The drive chains of low side switches are of BL type. The only difference with the BH type is that due to the fact that LS switches are sized to be three times bigger than the HS switches, the BL buffer is obtained by simply connecting three BH type buffers in parallel.

2.6.3 Level shifter

As shown in Fig. 2.21 many of the drive chains are working on a specific voltage domain. For this reason, the proposed architecture requires a significant number of level shifters which are highlighted in the figure. The function of each level shifter is to translate a logic signal from the input voltage domain $[0, V_i/4]$ to an output voltage domain $[mV_i/4, (m+1)V_i/4]$ with $m = 0, 1, 2, 3, 4$ depending on how the specific level shifter instance is connected. As already mentioned, level shifters are also placed on the inputs of LS drivers in order to provide proper time delay matching.

The proposed solution has been obtained after an iterative design focusing on the minimization of:

- power consumption: as there are several level shifters, these structures should consume a minimum amount of power during the voltage translation of the input signal transition from low-to-high or high-to-low, while they should have close to zero power consumption when no transition is occurring;
- propagation delay: the delay required to translate the control signal from input to output should be minimized in order to avoid a possible limitation on maximum control speed of the overall converter due to level shifters;
- propagation delay spread: as there are several instances of the level shifter, many of them working on a different output voltage domain, it is essential

that the propagation delay is independent from the voltage translation required to the specific level shifter instance.

Following these general requirements the principle scheme of Fig. 2.22, which shows the implemented functions, has been obtained.

The variation of the control signal logic level in the input voltage domain is transmitted to the output voltage domain where it is latched and provided to output. The presence of the memory element in the output voltage domain allows to switch off the transmission from the input voltage domain once the variation has been latched. This allows to reduce the static power consumption. For this purpose a feedback transmission is used together with a latch that stores the feedback and disables the main transmission. In addition, this process causes the level shifter input to become sensible to an opposite level variation on the input signal.

In order to understand how these functions have been implemented on silicon, Fig. 2.23 shows the transistor level schematic of the level shifter where the different functional areas have been highlighted. The circuit is split between the set and reset functions on the output memory element. For this reason, from the input signal IN, the "set" and "reset" commands are obtained and alternatively activated depending on the input signal's voltage level. The "set" command works on Low-to-High transitions of the input signal, "reset" on High-to-Low ones. As an example, the "set" operation will be described.

When IN goes from low to high, the lower NMOS of the transmitter (TX) is turned on and a current is sinked from the receiver (RX). This current causes the voltage on node "R_set" to drop. The higher is the magnitude of the current, the faster is the "R_set" voltage transition. However, higher currents require transistors with an higher W/L ratio thus with higher C_{iss} and C_{oss} capacitances. Moreover, they cause an higher power consumption. In order to maintain small sized transistors, limit the power consumption and most of all equalize the current's magnitudes in all the level shifters, the current is limited by a Cascode transistor with the gate biased by "LEVELSHIFTER_BIAS". This voltage bias is generated from a unique block and distributed to all the level shifters on chip.

The voltage difference between input and output voltage domain can be up to $5V_{imax}/4 = 20\ V$ with $m = 4$ voltage translations. A proper voltage blocking is obtained by adding four series Cascode connected 5V NMOS transistors biased at voltages "Vcas1", "Vcas2", "Vcas3" and "Vcas4". These have proven to be the faster among the solutions evaluated. In fact, the "R_set" node sees a parasitic capacitance which is greatly reduced with respect to solutions implementing the voltage blocking using HV transistors which have higher C_{oss} than 5 V devices. Moreover, the smaller parasitic capacitances of the 5 V devices are more immune to a capacitance value modulation imposed by the output voltage domain variation allowing a smaller delay spread between voltage translations with different m.

The bias voltages "Vcasx" are connected to the capacitive divider's nodes which offer the required voltage divisions. The bias voltages are differently connected depending on the voltage translation required for the specific level shifter instance. For example, LS driver's "dummy" level shifters have the bias voltages all connected

together to $V_{driveLS}$. Conversely, the level shifter used together with HS1 final driver, has Vcas1 connected to $V_{driveLS}$, Vcas2 to V_3, Vcas3 to V_2 and Vcas4 to V_i.

As "R_set" voltage drops, a modified inverter with an NMOS providing a weaker transconductance (realized with *W/L = 1/10*) is easily toggled to a logic "1" exploiting the high resistivity towards VSS_out provided by the NMOS itself. This event provides a falling edge to the output flip-flop which samples a logic "1" and pulls up the OUT signal. During the "R_set" voltage drop, the RX and Feedback TX transistors, of the set circuital section, are configured in such a way that "R_set" can be easily pulled down by the transmitter. Once that OUT has gone high, two operations are performed. The set RX transistors are configured in a way that prevents the "R_set" from being pulled down again making the set RX immune from spurious set current pulses. At the same time, the reset RX is enabled such that if "R_reset" node is pulled down by a reset current pulse, this can be detected. Moreover, the set 30 V Drain Extended (DE) PMOS is turned on and a feedback current pulse is sent down to the Feedback RX. In this case, the timing and especially the delay matching among different *m* cases, is not as relevant as in transmission so the DE PMOS can be used for the voltage blocking. This allows to spare some layout area.

The feedback pulse is used to clock the feedback memory element which pulls up Q_fb. Once this is achieved, the set signal is toggled to "0" and its TX is switched off, while the reset signal gate is enabled. Additionally, the set feedback resistive transistor is shorted to make the Feedback RX immune to any additional spurious feedback pulses. At the same time, the reset Feedback receiver is enabled.

The circuit is now configured to receive a reset which is associated with the High-to-Low transition of IN. Most of its DC currents are zeroed and its sensitive nodes are configured to provide immunity to spurious commands which could be generated by noise or unpredicted drifts.

A CLEAR structure implements a slower level shifter which is required to provide an asynchronous clear of the memory elements. This structure is used at start up to ensure that the level shifters are all cleared and starting from OUT = "0" configuration.

Fig. 2.24 shows the simulated output waveforms for different values of *m* with $f_s = 10\ MHz$, $V_i = 16\ V$. The different level shifter instances must ensure similar propagation delays to maintain disoverlaps and proper switching schemes. The delay spread between the logic fronts associated to outputs in different voltage domains must be minimized. Fig. 2.25 shows the simulation results still at $f_s = 10\ MHz$, $V_i = 16\ V$ of the spread between outputs with different *m* values. These signals are obtained considering only the differential voltage at the level shifters' outputs for each voltage translation case. The case $m = 4$ is the faster one, being supplied with an higher voltage difference between input and output voltage domain. However, the delay spread among all the cases is around *390 ps* which is more than tolerable on a switching period $T_s = 100\ ns$.

2.6.4 Refresh architecture

As previously introduced, the capacitive divider has different power absorptions from its nodes which would cause an uncontrolled voltage drift from the nominal

voltages. The first obvious reason is related to the $V_{driveLS}$ node which has many additional loads with respect to the V_2 and V_3 points. A solution to this problem can be a ladder of linear regulators which would regulate the capacitor voltages. This solution has a quite inefficient approach and can present problems during the start-up.

The solution adopted comes from the following consideration. Observing power stage nodes voltage levels during a switching period in Fig. 2.3 and Fig. 2.5 we have that:

$$VN2 = V_2 = \frac{3}{4}V_i \quad for\ VHS2\_logic = '1'; \tag{2.52}$$

$$VN3 = V_3 = \frac{1}{2}V_i \quad for\ VHS3\_logic = '1'; \tag{2.53}$$

$$VLx = V_{driveLS} = \frac{1}{4}V_i \quad for\ VHSx\_logic = '1'. \tag{2.54}$$

This means that connecting the *VN2*, *VN3* and each of the four *VLx* nodes with the proper capacitive divider node during the time intervals described by equations 2.52, 2.53 and 2.54 allows to regulate the capacitive divider values to the proper fraction of V_i. This type of regulation does not imply a dissipation of energy to obtain the proper value. In fact, it is based on the V_i partitioning imposed by the power stage and on the availability of the flying capacitors as charge reservoirs. In case the capacitive divider's node that needs to be refreshed is at a lower voltage than the target one, the amount of charge required is directly drained from the flying capacitor in the main power conversion path. Conversely, in case the divider's node is charged at a higher value with respect to the required, the energy is not dissipated but sent back to the flying capacitors. Assuming that the size of the flying capacitors is greater than the size of the C_{div} capacitors, the voltage drop caused on them by the regulation is negligible and is re-balanced by the automatic current balance property of the topology.

Fig. 2.26 shows the circuital blocks which form the refresh architecture. Each section is connected to a specific power stage node. During operation, the PMOS switches of the specific sections are turned on and the voltage is refreshed without the needs of any additional voltage conversion. In order to ensure that the refresh operation is done when the power stage node's voltage level is already settled, the PMOS switches are controlled with logic signals *VHSx_ref* that are timing windowed as shown in Fig. 2.26 with respect to the logic signals.

The four *VLx* nodes commuting at $V_i/4$ are connected to refresh $V_{driveLS}$. *VN2* and *VN3* provide the refresh of V_2 and V_3 nodes respectively. In order to test the refresh architecture functionality, the *VHSx_ref* signals are connected to the level shifters' inputs through pass-gate switches. These provide minimum additional propagation delay and allow to disable the refresh architecture by means of a logic signal named "Refresh" available on an external pin, as shown in Fig. 2.11.

In order to demonstrate the behavior of the refresh architecture, two transient simulations on *600 μs* have been run with Cadence ADE on the complete converter's

schematic monitoring the voltage nodes of the capacitive divider, output voltage and converter's efficiency. The first one has been done without the refresh architecture activated and its result is shown in Fig. 2.27. The time axis has been set to logarithmic scale in order to better appreciate the voltage drift which affects the capacitive divider nodes. The second simulation has been done under the same conditions but with the refresh architecture activated. Fig. 2.28 shows how, in this case, the voltages are stable and much closer to the required fractions of V_i.

In order to measure the behaviour of the capacitive divider, four *12 kΩ* SMD resistors have been placed in parallel with each C_{div} externally of the IC. This auxiliary divider is required to ensure a proper start-up using the available instrumentation. In fact, the chip has been designed and simulated for start-up transients of tens of microseconds, while the power supply used for this measurement (model EX354T by TTi) is only capable of ramping up the converter's V_i in few milliseconds. Fig. 2.29 shows the measured voltages of the divider's nodes. When the converter has no clock provided, the power stage flying capacitors (i.e. Ci1, Ci2 and Ci3) are pre-charged as explained in section 2.7 and then the converter idles. The capacitive divider voltages are able to drift depending on the different static absorptions present on each node. If the clock is provided, as soon as the flying capacitors pre-charging is accomplished, the converter starts to switch and the drive chains action tend to diminish the drifts but a dynamic imbalance between each node's power absorption is still present. The last measure, on the right of Fig. 2.29, shows the case when the refresh block is also activated and the drifts are minimized.

2.6.5 Layout

The drive architecture occupies the bigger area on the chip. Fig. 2.30 shows the distribution on silicon of the different functional blocks composing it. Everything is laid out following a generic rule, where the higher the current derivative can be on a certain path, the shorter the path itself should be, in order to minimize the parasitic inductance and resistance. For this reason, the drive chains are placed as close as possible to the gates of the switches they drive. The same with respect to the refresh blocks which need to interconnect the power stage nodes to the capacitive divider.

2.7 Start-up logic

Since power switches are rated for 9 V of V_{dsmax}, which is lower than $V_{imin} = 10.8\ V$, it is important to guarantee a controlled pre-charge of the flying capacitors C_{i1}, C_{i2} and C_{i3} at the converter start-up to avoid over-voltages of their V_{ds}. For this reason, the logic signals required at start-up are managed by a dedicated 5 V CMOS logic section, the start-up logic, whose scheme is shown in Fig. 2.31. The basic idea behind the start-up logic behavior is to exploit the ramp of the input voltage V_i, to pre-charge the flying capacitors to predefined voltage values and then start the steady-state logic as soon as V_i is high enough. The pre-charge is done directly through the power switches without the need of any additional dedicated switch.

To ensure that this logic is ready to work as soon as V_i is high enough, it is supplied by an auxiliary linearly regulated supply $V_{startup} = 4\ V$ which is present as soon as V_i reaches that value. The start-up voltage supply will be described in detail in subsection 2.7.2.

2.7.1 Start-up sequence

As it can be seen from Fig. 2.31, the start-up logic is divided in three sections. The first section senses the required node voltages and scales them down in order to obtain a voltage comparable with a *1.2 V* voltage threshold. This threshold is obtained from an on-chip bandgap reference generator. The second section evaluates the proper thresholds and consequently acts on the power switches' logic signals which are identified as "VHSx_start" or "VLSx_start" to differentiate them from the steady-state logic signals. These are buffered by the third section and connected to the multiplexer shown in Fig. 2.10.

In order to explain the behavior of the start-up logic, Fig. 2.32 shows the theoretical power stage's waveforms at start-up and the V_{gs} of the power switches obtained with the start-up logic signals. Each relevant event has been numbered for a better description of the start-up sequence.

As soon as $V_{startup}$ is high enough to supply logic cells, the signal "lvshf_clear" goes high providing the "clear" signal to each level shifter present on-chip (see Fig. 2.23). As the R-C divider voltage rises, the "lvshf_clear" is sent back to low. Conversely, the LS switches are turned on to keep a terminal of the flying capacitors to GND (event 1 in Fig. 2.32). The same signal is used to clear the flip-flop. As V_i reaches 7.5V (2), there is enough voltage to supply each drive section and HS switches can be turned on. Comparator U5 toggles and HS1, HS2 and HS3 logic signals are asserted. The three HS switches are turned on and used to respectively pre-charge the capacitor on their phase. The three capacitors are charged in parallel, as it can be noticed from the slopes of VNx nodes between (2) and (3). As soon as VN3 reaches 2.5V (3), U1 toggles and HS3 is turned off. The same then happens for HS2 when VN2 reaches 5V (4) and for HS1 when VN1 reaches 7.5V (5). Finally, with the capacitors all pre-charged, when V_i becomes greater than 9V (6) U4 toggles and "SS EN" signal is asserted. This signal is the steady-state enable, it enables the steady-state logic and toggles the multiplexer of Fig. 2.10 such that the switches are now controlled by the steady state logic. After (6) the converter starts to switch following V_i as it finishes ramping and settles. The "SS EN" signal is also used to disable the comparators reducing the regime power consumption of the start-up logic. The logic has been designed to work with a slew rate of V_i as fast as $1\ V/\mu s$.

Fig. 2.33 shows a measured start-up sequence done on the realized chip which shows a good agreement with the theoretical behaviour. The V_i ramp has been achieved using a programmable voltage ramp from an Agilent 33120A arbitrary waveform generator (AWG). In order to achieve the capability of driving the converter's input capacitance C_{in}, the AWG output has been amplified with a voltage power amplifier [50]. It has been possible to achieve a ramp with a slope as fast as $10\ V/15\ \mu s$ as it can be noticed from Fig. 2.33 in (a). During the rise of V_i, before the turn-on of the three HS switches, the VNx nodes have significant leakage pre-charge

probably due to the fact that the HS switches are not completely kept off in this time interval. However, this pre-charge doesn't cause any negative consequence. Fig. 2.33 (b) shows a close-up on the instant when HS switches are turned on. The three VNx nodes settle at evenly spaced voltage values leaving the three flying capacitors properly pre-charged. Fig. 2.33 (c) shows how there is some bouncing associated with the comparators' control of the VNx nodes' thresholds. These bounces doesn't cause any issue and the settling voltages are properly achieved. These voltages remain stable until steady-state condition is enabled. After the switching starts, there is an initial transient on each VNx voltage, which can be appreciated in (b) from *6 μs* to *15 μs*, but the steady-state switching condition eventually re-balances the voltages which assume the proper steady-state dynamics as shown in Fig. 2.33 (d).

2.7.2 Start-up voltage supply

The start-up voltage supply is a linearly regulated voltage supply which provides $V_{startup} \approx 3.5\ V$ used to supply the start-up logic, disable the ESD protections on the pad ring and supply the *1.2 V* band-gap voltage reference generator and the PTAT bias currents generator. After the start-up operation is completed, the bandgap and current generators are the only loads connected under this linearly regulated supply with a negligible current absorption. Fig. 2.34 shows the schematic of the start-up voltage supply, including the bandgap voltage and bias currents generators.

The diode-connected 5V NMOS transistors (shown directly as diodes in the schematic), provide a gate voltage for the 20 V LD NMOS of approximately $V_g \approx 7 \cdot 0.7V = 4.9V$. Thus $V_{startup} \approx V_g - V_{th} = 4.9\ V - 1.4\ V = 3.5\ V$. As it is possible to notice, the main goal of the start-up supply is not precision but rather speed at turn-on, which has to be achieved following the V_i ramp.

2.8 Steady-state operation

Once the start-up phase is finished and the “SS EN” signal is activated and the steady-state mode of operation starts. This mode is managed by the steady-state logic of Fig. 2.10 which takes as input a clock signal, a digital flag and two analog programming signals and uses them to generate PWM logic signals to control the power stage switches and the drive architecture's refresh. As already said, this logic is supplied by $V_{driveLS}$ node of the capacitive divider, thus no additional linear regulator is required for its operation.

2.8.1 Steady-state logic

In order to implement the most of the functionality inside the chip, the steady-state logic has been designed to be externally programmable in terms of switching mode and duty cycle using a minimum amount of inputs, still preserving the flexibility required to adjust eventual discrepancies with simulated waveforms. Table 2.3

lists this input pins required to control the behavior of the steady-state logic and describes their functionality in terms of logic configuration.

Table 2.3 Input pins used to program the steady-state logic behaviour and their functional description.

Pin name	Type	Functional description	Values	
			$k = 1$	$k = 2$
Clock	Analog, AC	Timing reference used to generate the control signals	$f_s = \frac{f_{clock}}{4}$	$f_s = \frac{f_{clock}}{2}$
Mode	Digital	Sets the switching mode	Mode = '0'	Mode = '1'
V_{reg}	Analog, DC	Sets the duty cycle ratio D value on a range $V_{reg} = [0, 1.2]\ V$	$D = \frac{V_{reg}}{4 \cdot 1.2\ V}$	$D = \frac{V_{reg}}{2 \cdot 1.2\ V}$
I_{pwm}	Analog, DC	Current bias used to adjust the slope of the PWM ramp generator depending on the switching mode	$I_{pwm} = 1.2\ V \cdot \frac{4C_P}{T_s}$ $I_{pwm}\big\vert_{10MHz} \approx 6.3\ \mu A$	$I_{pwm} = 1.2\ V \cdot \frac{2C_P}{T_s}$ $I_{pwm}\big\vert_{10MHz} \approx 12.6\ \mu A$

Using the parameters in Table 2.3 the steady-state logic generates the proper signals depending on the switching mode selected. The clock signal is used to generated the timing slots required by the switching schemes of Fig. 2.2 and Fig. 2.4. In order to simplify the design of the chip, no internal PLL circuitry has been designed so it is not possible to internally multiply the frequency and achieve $T_s/4$ and $T_s/2$ time bases. Instead, the external clock must be provided with a frequency at a proper multiple of f_s.

The duty cycle D is linearly proportional to the analog voltage $V_{reg} = [0, 1.2]\ V$. A better control on the PWM signal generation, consequently on the D value, is achieved by providing with the external pin I_{pwm} a bias current. This current is internally used for the ramp generator of the PWM modulator block which will be explained further on. It is important to note that adjusting the V_{reg} and I_{pwm} values allows to test a precise duty cycle getting rid of eventual discrepancies related to the

variation of integrated components values with respect to nominal (e.g. the value of C_P the capacitor used inside the ramp generator).

The steady state logic schematic is shown in Fig. 2.35. On the "SS EN" signal assertion, the "ClockGen" block starts working, transforming the AC coupled Clock input in a digital clock signal with *50 %* duty cycle. The close-up in the upper left corner of the figure shows its circuitry.

By means of a type T flip-flop, the clock signal frequency is halved and two identical PWM modulator blocks (i.e. "PWM Mod" in the schematic) are activated alternatively. The choice of using two PWM modulators in parallel has been adopted to relax the timing constraints on modulator reset time, thus allowing proper operation at maximum switching frequency (i.e. 15 MHz). In fact, the modulator structure works as shown in the lower left side close-up of Fig. 2.35. As a low-to-high transition of "clock" occurs the latch is set and PWM_out goes high. At the same time the capacitor C_P is charged with a constant current I_{pwm} generating a linear ramp on the negative input of the comparator. As soon as the ramp reaches the V_{reg} voltage value the comparator toggles and PWM_out goes low. This provides a relationship between the PWM_out duty cycle δ and V_{reg} value which can be described as:

$$V_{reg} = \frac{I_{pwm}}{C_P}\delta T_{pwm}\,. \tag{2.55}$$

The PWM period T_{pwm} is only a fraction of the converter's switching period T_s and more precisely:

$$T_{pwm} = \begin{cases} \frac{T_s}{4} & for\ k = 1 \\ \frac{T_s}{2} & for\ k = 2 \end{cases}. \tag{2.56}$$

Equation 2.55, can be expressed in terms of D as:

$$V_{reg} = \begin{cases} \frac{I_{pwm}}{C_P} DT_s & with\ D < \frac{1}{4} \quad for\ k = 1 \\ \frac{I_{pwm}}{C_P} DT_s & with\ D < \frac{1}{2} \quad for\ k = 2 \end{cases}. \tag{2.57}$$

I_{pwm} must be set to achieve D_{max} with $V_{reg\,max}$. We obtain:

$$I_{pwm} = \begin{cases} V_{reg} \cdot \frac{4C_P}{T_s} & for\ k = 1 \\ V_{reg} \cdot \frac{2C_P}{T_s} & for\ k = 2 \end{cases}. \tag{2.58}$$

In our case we have chosen $V_{reg\ max} = 1.2\ V$ in order to use the same comparator circuitry which has been used for the start-up logic. This gives the formulas shown in Table 2.3 for I_{pwm}. The capacitor C_P has been implemented using MIM capacitor in order to ensure better linearity of capacitance against applied voltage with respect to MOS capacitors. The value implemented is $C_P = 262.5\ pF$ taking into account also the parasitic input capacitance of the comparator and switches. With $T_s = 100\ ns$ the I_{pwm} values shown in table are obtained.

With these settings there is a linear relationship between the value set at V_{reg} and D, as shown in table.

The "PWM_out" signal is routed to a 2-to-1 multiplexer (MUX) and the proper PWM output is selected depending on which PWM Mod has been clocked last. The MUX selection is properly delayed with a τ_p delay chain.

A programmable circular shift register is initialized at start-up with the "lvshf_clear" signal and configured with "Mode" depending on switching scheme used. This block loads an initial binary configuration as '1000'. The '1' is then circularly cycled on each clock rising edge inside the various positions. With $k = 1$ all OUT1 to OUT4 are used, while with $k = 2$ the circulation is limited to OUT1 and OUT2.

This block, used together with the "1 to 4 deMUX" and "Mode-conditional routing" realizes the logic signals of the four different phases each with duty cycle D. The deMUX operates with the transfer function shown in Fig. 2.35. The routing has "dummy" MUXes on paths 1 and 2 to achieve delay matching among all the phases.

As it is possible to notice, this logic structure doesn't allow to control the duty cycle of the single power switch but each switch is provided with the same duty.

The four phases' logic signals are sent to two different types of disoverlap generators. The one shown in the lower right corner close-up of the figure, achieves the disoverlaps needed between HS and LS switches of the same phase. The one shown in the upper right corner close-up, achieves the disoverlap required for the refresh blocks, as shown in Fig. 2.26. The disoverlaps provided between the outputs VHSx_logic, VHSx_logic, VHSx_ref are shown in the timing diagram of Fig. 2.36. In our case, the delay blocks implement a time delay $\tau = 1\ ns$ which gives a disoverlap between HS and LS logic signals of $t_{dis} = 2\ ns$. This value has been selected with a parametric analysis of logic disoverlap time in range $t_{dis} = [300\ ps, 3\ ns]$ evaluating the variation of the output efficiency on the overall converter's architecture. More details on this analysis are provided in subsection 2.9.3.

2.9 Simulation results

The design of an IC relies almost exclusively on the circuital simulation results obtained with dedicated design tools (e.g. the Cadence Virtuoso suite) using physical models of the devices available in a specific technology process of interest. When it comes down to design a single-chip DC-DC converter, as in our case, this allows to exploit the simulation results in order to optimize the circuit behaviour to meet requirements and maximize power efficiency. The most important optimizations that have been achieved with the help of simulation results are the sizing of the

power switches and drivers as described in subsection 2.9.2, the current distribution of power switches to reduce their contact resistance as it has been presented in subsection 2.5.2, the disoverlap time between HS and LS logic signals. The possibility of simulating the different blocks and overall architecture in various process corners is also relevant. This aspect is treated in subsection 2.9.4 with respect to the start-up transient behaviour.

2.9.1 Parasitics modeling in circuital simulations

In order to improve the reliability of the circuital simulation's results, a fundamental point is the correct modeling of the components and parasitics that are present both "on-chip" and "off-chip". With respect to the parasitics "on-chip" the schematic simulation can only take into account the parasitics modeled inside the physical device models and strictly related to the single device inner layout (e.g. the gate-drain capacitance of a MOSFET) as if the device has ideal contacts and interconnections. The additional parasitics generated by the physical layout of each specific instance of the device cannot be included. These are included in post-layout simulations by RLC parasitic extractors. The parasitics related to the components outside of the chip are those related to the real behavior of the components soldered on PCB and PCB layout itself, but also those related to wire bonding and packaging of the die in general. All these "off-chip" additional parasitics must be taken into account and modeled by the designer with nets combining various ideal RLC components which model the real behaviour of parts like the wire bonding, the power inductors, the capacitors, etc...

Following this purpose, the external power stage's parasitics have been modeled in the circuital simulations as shown in Fig. 2.37. The modeling includes the parasitics which provide the most relevant contributions to power loss, thus directly influence converter's efficiency.

The inductors have an high impact on the overall converter size so we have modeled three different inductors following a trade-off between power density and efficiency. In fact, smaller inductors provide higher power density of the overall converter but present higher series resistance and, due to the presence of magnetic cores they suffer of core losses. The inductor L_a with $L = 110\ nH$ and $DCR = 90\ m\Omega$ models values associated with a 0603 SMD inductor used as reference case to maximize power density. The second value, L_b models an inductor with bigger sizes and thus reduced series resistance. The last inductor value, L_c is an air-core inductor, thus no core loss is modeled. These models' values refer to real inductors which are presented in subsection 2.10.2. The rest of the passives (i.e. C_{in}, C_i and C_o capacitors, wire bonding) have been modeled with their additional parasitics to provide an estimation of their power losses. Also in this case, their parasitics are related to real components' values.

2.9.2 Optimization of power switches sizing

The integrated realization allows an optimization of power switches' sizes in function of maximum efficiency. The operating condition for which we have opti-

mized the efficiency is aiming at the maximum output power density of the converter. For this reason we have chosen as optimization case: $k = 2$, $f_s = 10\ MHz$, $V_i = 12\ V$, $V_o = 1.2\ V$, $I_o = 2\ A$. The $k = 2$ has been chosen due to the higher output ranges achievable.

The efficiency has been optimized with Cadence Virtuoso Analog Design Environment (ADE) simulations using the schematic shown in Fig. 2.37 to model the parasitics configured with the 0603 SMD inductor. A VerilogA PID controller block has been implemented in the simulation to ensure that the duty cycle is regulated to maintain $V_o = 1.2V$, $I_o = 2\ A$. The optimization process has been done following three steps.

As starting point, the sizes of power switches have been evaluated with an iterative design trading-off between the power switches' overall sizes and maximum achievable efficiency. In doing this analysis an equal size of HS and LS switches has been considered and the driver has been adapted following the FO4 rule with respect to the switches' sizes. The result of this preliminary analysis has given an efficiency $\eta = 77.3\ \%$ and the sizing in terms of W/L ratio of the switches has been $W/L = 26400/0.8$.

With respect to the buffers used in the drive architecture, they have initially been assumed all of the balanced type (see subsection 2.6.2) and simplified in simulation, still preserving the FO4 tapering, with parallels of multiple instances of the "BUF16" logic block. This logic component is a CMOS logic buffer, available with the logic family of the technological process used, with a drive strength sixteen times higher than the minimum inverter achievable with the technological process. After the evaluation of the optimal sizing has been accomplished, this "BUF16" blocks have been converted to equivalent inverters to optimize layout area. Moreover, the "selective" tapering of the driver chains has been done as explained in subsection 2.6.2.

Going back to the preliminary analysis result, the number of buffers "BUF16" in the final drivers' stages has been $N_{BUF16} = 50$.

The second step of optimization has been to use this preliminary results to run a parametric analysis over the HS and LS switches sizes with a proportional variation of the drivers' final stages.

The used parameters are:

$$\left.\frac{W}{L}\right|_{HS} = HS_{fingers} \cdot \frac{2640}{0.8} \tag{2.59}$$

$$\left.\frac{W}{L}\right|_{LS} = LS_{fingers} \cdot \frac{2640}{0.8} \tag{2.60}$$

$$N_{BUF16\,HS} = 5 \cdot HS_{fingers} \tag{2.61}$$

$$N_{BUF16\,LS} = 5 \cdot LS_{fingers} \tag{2.62}$$

The parameters $HS_{fingers}$ and $LS_{fingers}$ have been used to set a multi-parametric transient simulation in ADE with ranges $HS_{fingers} = [2, 12]$ and $LS_{fingers} = [8, 22]$. The steady-state is controlled by the VerilogA controller in order to maintain the optimization output power equal for all the different simulation runs. For each run, when the steady-state is reached, output efficiency, drive power, V_o and I_o are saved. The results are shown in Fig. 2.38.

The graphs are obtained with $LS_{fingers}$ on x-axis while different curves are plotted for different values of $HS_{fingers}$. As shown in the efficiency graph, the starting point with $HS_{fingers} = LS_{fingers} = 10$ gives an efficiency which can be increased by increasing the sizes of the switches. The curve which seems to maintain the best efficiency is the one associated to $HS_{fingers} = 5$. The value of $LS_{fingers}$ has been limited to $LS_{fingers} = 15$ in order to limit the overall size of the power stage on silicon. In fact, this choice allows to maintain the same layout area as the initial case but it increases efficiency from *77.3 %* to *80.5 %*. A bigger LS switch (i.e. with $LS_{fingers} = 22$) gives only a *0.5 %* increment which doesn't justify the additional area required.

The third step of the optimization is related to the size of the driver's final stages. In order to demonstrate that the values obtained from previous analysis allow the best efficiency result in terms of drive, an additional multi-parametric simulation is done. This time, the power switches' sizes are fixed to their final values which are:

$$\left.\frac{W}{L}\right|_{HS} = HS_{fingers} \cdot \frac{2640}{0.8} = \frac{13200}{0.8} \tag{2.63}$$

$$\left.\frac{W}{L}\right|_{LS} = LS_{fingers} \cdot \frac{2640}{0.8} = \frac{39600}{0.8} \tag{2.64}$$

while the driver's sizes in terms of “BUF16” instances are still varied in the same range as above. The results of this second analysis are shown in Fig. 2.39. It is possible to notice how the driver sizes were already very close to their optimal value as $LS_{fingers} = 15$ gives the peak of efficiency. However, with respect to the HS number of fingers $HS_{fingers} = 4$ gives a slight increment on efficiency. Thus, the final sizes of drivers are:

$$N_{BUF16\,HS} = 20 \tag{2.65}$$

$$N_{BUF16\,LS} = 75 \tag{2.66}$$

which have been used to size the drive architecture and each stage's tapering.

2.9.3 Optimal disoverlap analysis

In order to evaluate the best disoverlap time between the logic signals controlling HS and LS switches turn-ons, a parametric simulation with a variable disoverlap time has been set for the same nominal operating condition used in previous subsection. The disoverlap time has been varied in an interval t_{dis} = [*300 ps*, *3 ns*] keeping all the other values constant. The rise and fall times of logic signals are set to $t_r = t_f = 300\ ps$. Steady-state V_o, I_o, drive architecture power P_{drive} and efficiency are saved and plotted against t_{dis}. The result is shown in Fig. 2.40, where it is possible to notice how efficiency is almost constant for t_{dis} = [*500 ps*, *2 ns*]. In the sizing of the disoverlap generators a $t_{dis} = 2\ ns$ has been considered to minimize the drive power.

2.9.4 Start-up transient analysis in technological process corners

The start-up operation of the converter relies on the proper behaviour of several sub-blocks. These can have a variation of their time delays depending on the technological process variations, temperature variation and other design variables. In our case, a design variable of interest is the input voltage. For this reason the start-up transient of the overall converter schematic has been simulated in the corners shown in Table 2.4, which has been selected among the possible combinations trying to select the hardest operating cases. The technological process models have three different settings which model the variations of devices' performances from "weak" to "strong" which are associated to respectively more or less resistive devices with respect to nominal conditions. V_i corner values are chosen depending on requirements. Case "1" has been included as reference case. Fig. 2.41 shows the values of efficiency, V_i and V_o. It is important to underline that the converter is able to start-up for each different case. However, the efficiency drifts much from the nominal value.

Table 2.4 Parameters used for start-up transient corner analysis.

	Device models			V_i (V)			T (°C)		
Id.	Weak	Nominal	Strong	10.8	12	16	0	27	125
1		x			x			x	
2	x			x			x		
3	x			x					x
4	x					x			x
5			x	x					x
6			x			x			x

2.9.5 Power losses breakdown and efficiency evaluation

Table 2.5 shows the losses breakdown obtained from the simulation of the complete converter schematics after optimization. P_{HS} and P_{LS} estimate the drain to source losses of the power switches averaged over a steady-state switching period. These have been calculated from simulation considering the $V_{ds}(t)$ voltage across the specific power switch and $I_d(t)$ drain current.
Thus:

$$P_{HS/LS} = f_s \cdot \int_0^T V_{ds}(t) I_d(t) dt. \quad (2.67)$$

P_{ind} the inductor losses are estimated with RMS current and the simplified model shown in subsection 2.9.1. Thus:

$$P_{ind} = I_{ind\ RMS}^2 \cdot R_{ind}. \quad (2.68)$$

In this case the values of $L = 110\ nH$ and $R_{ind} = 90\ m\Omega$ have been used to model the smaller inductor.

P_{drive} includes the total drive losses. These have been measured with a dedicated VerilogA watt-meter which estimates the average power drained from V_i by the complete drive architecture and logic blocks.

The remaining losses P_{other} (i.e. passive components ESR, bonding resistance, parasitic diodes, etc...) are obtained as a subtraction from the total input power, thus:

$$P_{other} = P_{in} - P_{out} - P_{HS} - P_{LS} - P_{ind} - P_{drive}. \quad (2.69)$$

Fig. 2.42 shows the pie chart of the power losses from Table 2.5.

Table 2.5 Estimated power losses breakdown with $k = 2$, $f_s = 10\ MHz$, $V_i = 12\ V$, $V_o = 1.2\ V$, $I_o = 2\ A$, 0603 SMD inductor.

HS	mW	%	LS	mW	%	Ind	mW	%		mW	%
1	68.01	11.2	1	42.15	7.0	1	25.81	4.3	Drive	83.01	13.7
2	51.68	8.5	2	42.95	7.1	2	26.27	4.3	Other	45.85	7.6
3	68.08	11.2	3	37.49	6.2	3	26.08	4.3			
4	39.73	6.6	4	21.81	3.6	4	26.59	4.4	Total loss	605.51	mW
Total	227.50	37.6	Total	144.40	23.8	Total	104.75	17.3			

2.9.6 Efficiency

The inductors modeled in Fig. 2.37 have been also used to evaluate schematic efficiency versus the load current and input voltage for the different trade-offs. As before, the VerilogA controller has been used to maintain a constant output power condition. As an example, Fig 2.43 shows the efficiency versus V_i with $V_o = 1.2\ V$, $I_o = 2\ A$ and efficiency versus I_o with $V_i = 12\ V$, $V_o = 1.2\ V$ for inductors L_a and L_c. The maximum efficiency, depending on V_i, is achieved with $V_i = 13\ V$ for both inductors and is $\eta_a = 80\ \%$, $\eta_c = 85\ \%$. It is also relevant that with $V_i < 12\ V$ the converter cannot provide $I_o = 2\ A$ as the output voltage drops, too. Considering the effi-

ciency versus I_o, inductor L_a provides a maximum efficiency $\eta_{a\ max} = 82\ \%$ with $I_o = 1\ A$ while inductor L_c provides $\eta_{c\ max} = 85\ \%$ with $I_o = 1.4\ A$. As this comparison is done between two inductors with the same inductance, it is possible to notice how varying inductor's DCR only, influences much the total efficiency.

2.10 Board design and measurement results

Due to the sizes of the integrated circuit package and presence of the thermal pad, which required re-flow soldering, the realized converter has been tested adopting a modular PCB solution. Each chip has been re-flow soldered on a "daughter" board where the passives necessary to complete the converter topology have been soldered close to the chip to minimize parasitics and overall converter's area to achieve highest power density. Due to the fact that there is a need to test different inductors, the daughter board has been realized in five different versions which are identical, with exceptions made for the inductors' land patterns. The five different land patterns have been obtained by grouping together the land patterns of the possible inductors of interest trying to make a minimum number of boards capable to host many different inductors' values and packages.

A main board, the "mother" board, has been designed to host the daughter board with a custom socket. This board has the electronics needed to set the programming pins providing the switching scheme, PWM polarization, duty cycle and clock input. In case a daughter board is damaged or a comparison needs to be done among different daughter boards, it is simply a matter of replacing it, preserving exactly the same external settings on the chip. Fig. 2.44 shows a picture of the mother and one of the daughter boards assembled together as they are used for the testing.

Additional details on daughter and mother boards can be found in Appendix B.

The measurements presented in the following sections have all been done with this test PCBs. The measurement setup is shown in Fig. 2.45. The MATLAB instrumentation control toolbox has been used to control the digital multimeters and electronic load in order to automate the efficiency measurements. Voltage waveforms have been measured with a Tektronix 3054B digital oscilloscope. The test points on daughter board are shown in Fig. 2.46. It is possible to notice how the test points of switching nodes are the SMD contacts of passive components. In fact, test point structures have been limited to avoid both the additional parasitics and PCB area related to them.

2.10.1 Power stage voltage waveforms

Fig. 2.47 shows the measured voltages of the power switches nodes at steady-state for $k = 1, 2$, $V_i = 12\ V$, $f_s = 10\ MHz$ and maximum duty operation. These respect the voltage dynamics of the theoretical waveforms shown in Fig. 2.3 and Fig. 2.5.

Fig. 2.48 shows the measured output AC voltage ripple $V_{o\ ac}$ for $k = 1, 2$ with $V_i = 12\ V$, $I_o = 2\ A$. In Fig. 2.48b it is possible to appreciate how the ripple frequency $f_{rip} = 2\,f_s$. This is less evident for $k = 1$ where $f_{rip} = 4\,f_s$.

2.10.2 Efficiency

Fig. 2.49 shows three of the five different solutions for the daughter boar, equipped with the power inductors previously modeled in simulation. These are Coilcraft SMT inductors, with the specifications in Table 2.6. We decided to focus this initial analysis on inductors with inductance close to the minimum design value.

The three inductors have different trade-offs between power density and overall converter efficiency η. This can be appreciated from Fig. 2.50 where, from left to right, the first row shows the measured efficiencies with $V_i = [11, 16]\ V$ of the three solutions in Fig. 2.49. Due to the fact that the converter hasn't got a feedback control, the output power P_o, instead of load current, has been used to map efficiency. The second row shows the efficiency curves as $V_i = 12\ V$ with $f_s = [7.5, 15]\ MHz$. As it is possible to notice, the optimum switching frequency is close to *7.5 MHz*. Air core inductor, sample 3, results more efficient than sample 2 even if it has a three times higher DCR. This is related to the fact that sample 2 has additional losses related to the magnetic core. The measured results show efficiency curves that are below the simulated values. This can be seen comparing Fig. 2.50 with Fig. 2.43.

Table 2.6 Tested inductors.

Board No.	Part No.	Size (mm)	Core	L (nH)	I_{RMS} (A)	DCR (mΩ)
1	0603AF-111XJRU	1.8 x 1.12 x 0.91	Ferrite	110	1.6	60
2	XFL4012-121MEB	4 x 4 x 1.2	Ferrite	120	9.6	5.88
3	1812SMS-R12JLB	4.95 x 6.35 x 4.2	Air	120	1.5	17.3

Additional loss contributions are probably related to the fact that the dead time of the power switches is fixed in this implementation and cannot be adjusted to compensate for the load variation and the presence of additional parasitics and non idealities of the prototype. Among the non-modeled parasitics, it is possible to assume also the capacitance of PCB which subtracts energy from the various switching nodes. These assumptions are partially confirmed by the fact that decreasing the switching frequency to *7.5 MHz* shows higher efficiency. In fact, decreasing the switching frequency reduces the switching losses while the conduction ones are less dependent on frequency. However, the decrease to *7.5 MHz* is not sufficient to recover the total difference with respect to simulation meaning that some additional non-modeled losses contributions are present. Another hypothesis is related to the core losses which could be higher than the amount modeled with the simplistic assumption using a series resistor. In fact, these are dependent on inductors' current ripple amplitude, DC value and frequency as explained in Chapter 4. Nevertheless, despite the decreased efficiency with respect to simulation, it is still possible to appreciate the trade-off between maximum efficiency and power density. The coreless "Sample 3" has *3 %* higher efficiency with respect to the smallest 0603 inductor "Sample 1".

2.11 Power density comparison

The solution with the smaller inductors (i.e. number 1 in Fig. 2.49) has an increased power density with respect to previous solutions using the same topology. The implemented solution has a converter area $A_{conv} = 150\ mm^2$ with an output power $P_o \leq 3.8\ W$ as shown in Fig. 2.50. We can define a power density estimated over converter area of:

$$PD_A = \frac{P_o}{A_{conv}} = 25.3 \frac{mW}{mm^2}. \tag{2.70}$$

An initial comparison can be done in terms of equivalent topologies with the VRM proposed in [47]. The converter presented there has been implemented on a PCB area which can be estimated as approximately $A_{conv} = 3000\ mm^2$ of converter area with $P_o \leq 60W$. Thus, it has a power density $PD_{A1} = 20\ mW/mm^2$ for a $f_s = 1\ MHz$. The comparison shows how an increment of a decade in switching frequency causes an increment of roughly *25 %* in power density. However, the previous comparison is done between solutions which have completely different targets in terms of output power.

A better comparison for the performances of the proposed solution can be done by referring to the converter presented in [51], which is a merged two-stage approach converter. This comparison is shown in Table 2.7. The maximum power density has been estimated considering that the merged two-stage converter has a PCB converter area which can be estimated to roughly $A_{conv} = 300\ mm^2$. This is done without taking into account the presence of the capacitors of switched capacitor stage that have been soldered on the other side of the board. It is interesting to see how the proposed converter has an order of magnitude better performances in terms of power density and more than double voltage step-down, despite the fact that efficiency is a *5 %* lower.

Table 2.7 Performance comparison.

Reference	[51]	This work
Topology	Merged two-stage	High step-down / Extended duty
Technology	CMOS *0.18 µm*	CMOS *0.7 µm* + LDMOS
V_i	*4.0 – 5.5 V*	*10.8 – 16 V*
V_o	*0.8 – 1.3 V*	*0.675 – 2 V*
f_s	*10 MHz*	*10 MHz*
Max. η	*81 %*	*76 %*
Voltage step-down at max. η	*5.0 V : 1.3 V*	*13 V : 1.2 V*
Output power	*0.3 W to 0.8 W*	*0.5 W to 3.8 W*
Maximum estimated PD_A	*2.6 mW/mm²*	*25.3 mW/mm²*

2.12 Conclusion

An integrated high step-down four phase buck converter architecture has been presented. The advantages provided by the topology with respect to multiphase buck converters have been reviewed from literature and described in detail. These provide duty cycle extension, power switches voltage rating reduction and inductor voltage swing reduction leading to reduced switching losses and smaller output capacitance and inductor's values. The benefits can be enhanced exploiting also the integrated realization, which allows to increase the switching frequency of the converter up to 10 MHz with benefits in terms of dynamic response and additional passives' size reduction. Integration can be used to optimize the sizing of power switches and designing a custom drive architecture and other auxiliary blocks. For these reasons, the integration of power stage has been presented focusing on details like optimal sizing, placement on the layout and switches' interconnection resistance reduction. The custom drive architecture developed to control the eight power switches has been presented together with the most important sub-blocks. These allow to realize the drive without the need of any additional linear voltage regulator. The logic blocks implemented, comprising start-up and steady-state logic blocks have been described. The automatic start-up sequence including the pre-charging of the flying capacitors has been explained and analyzed with measured results. The steady-state logic operation has been described, too. Three different SMT inductors solutions have been simulated and measured to demonstrate the trade-off existing between the most power dense solution and the most efficient one. The overall converter power density shows an increment with respect to previous solutions using the same topology and with respect to solutions with different topology aiming at comparable output powers and performances.

The main purpose of this work was to demonstrate the feasibility of integration for the four phases high step-down buck. Moreover, the proper operation of several auxiliary blocks has been proven. Future work will focus on the development of a controller to additionally characterize the behavior in closed loop for various load conditions and load current transients. Additional tests with inductors, not focusing on minimum inductance value, will allow a better optimization of the efficiency of the converter. From physical layout point of view, the converter works with inductance and capacitance values which easily allow, with future design reviews, to move from a single chip solution with external passives to a “PwrSiP” possibly using custom inductors realized to fit directly on top of the die while capacitors are placed aside.

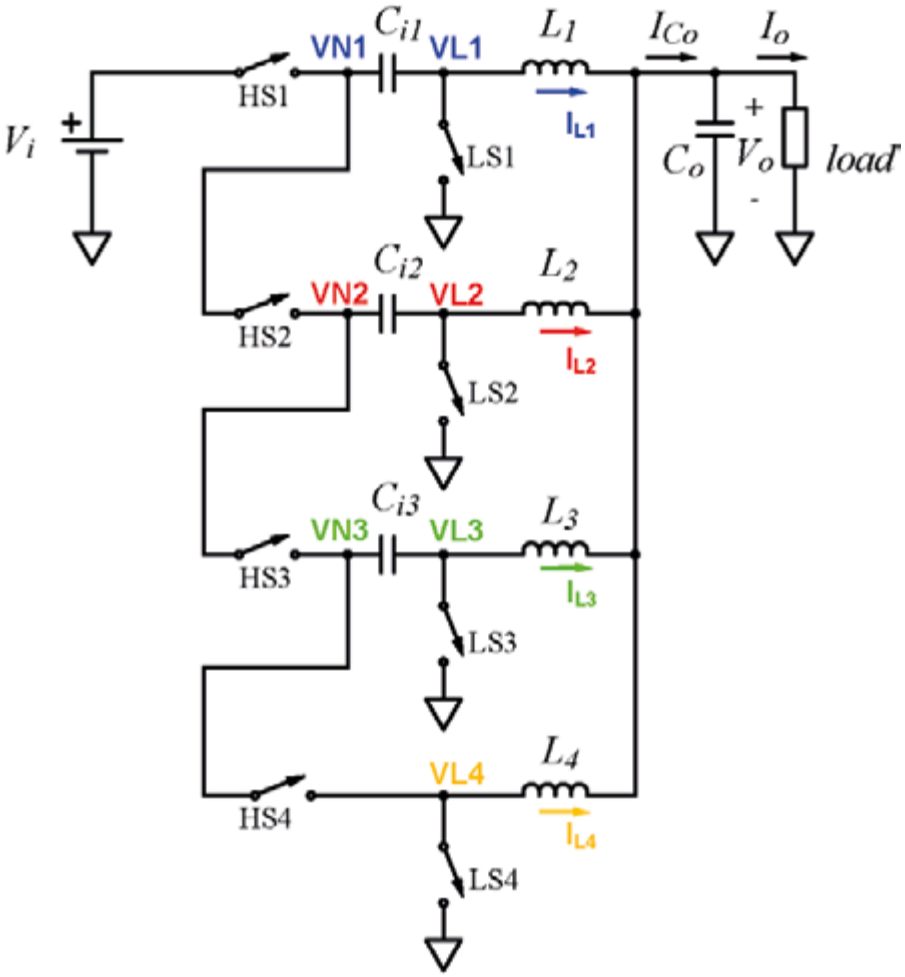


Fig. 2.1. Four phases high step-down buck ideal circuit.

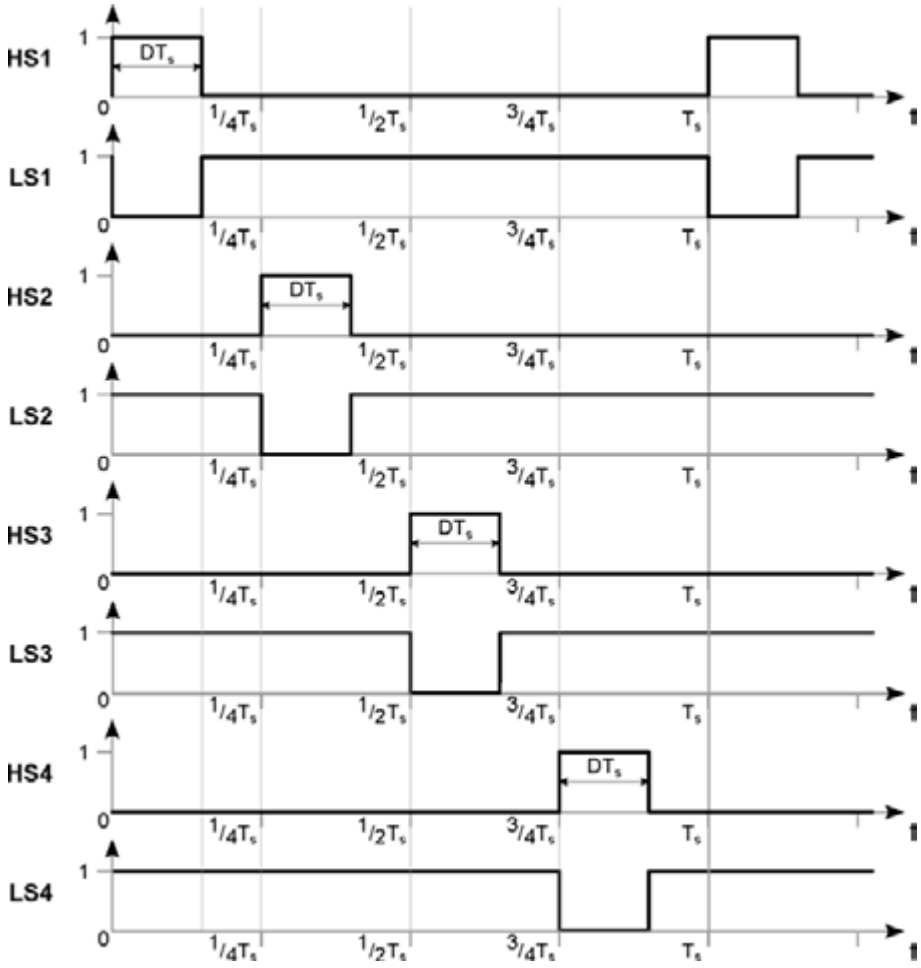


Fig. 2.2. *k=1* switching scheme logic signals.

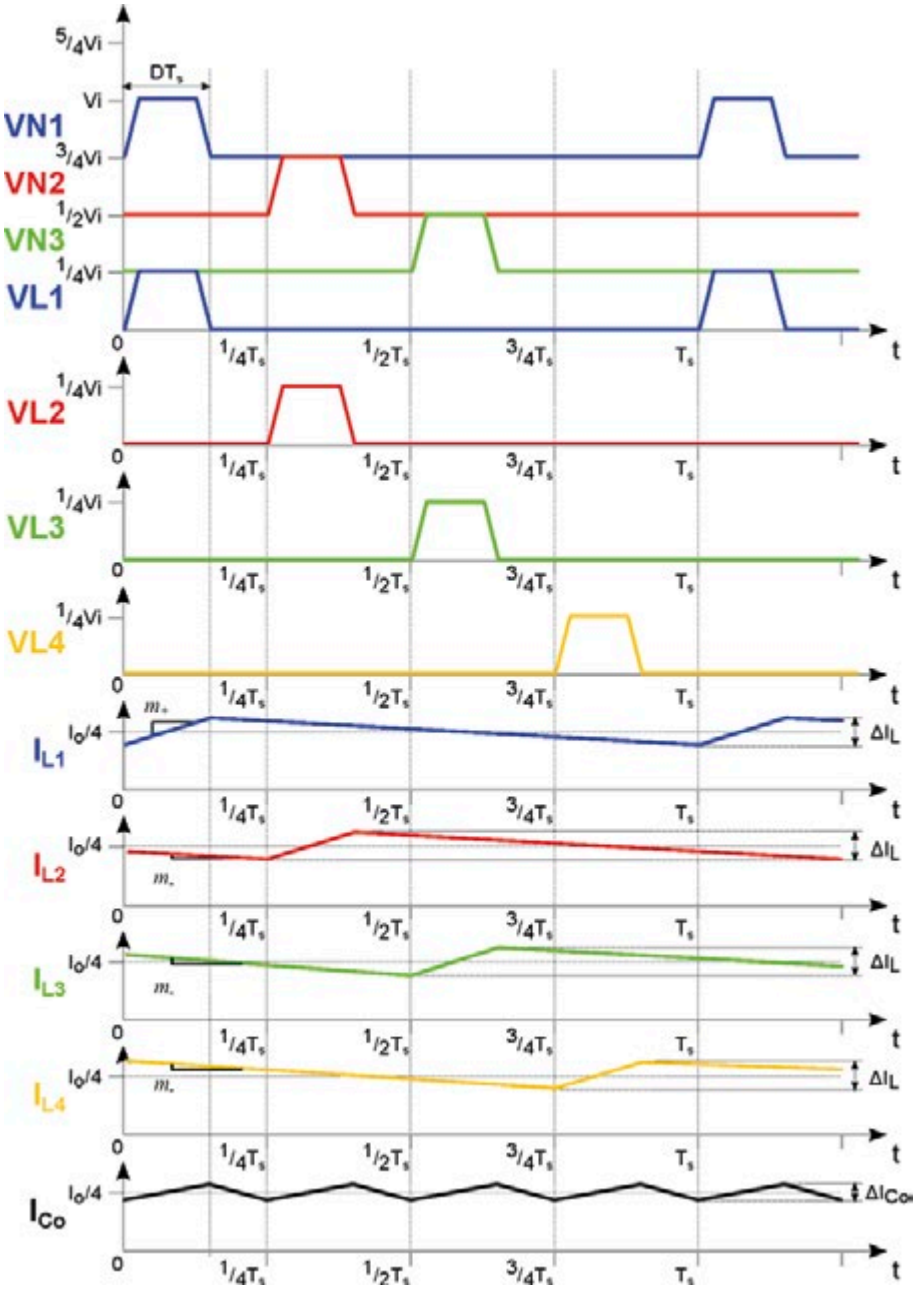


Fig. 2.3. *k=1* power stage voltage nodes and currents ideal waveforms.

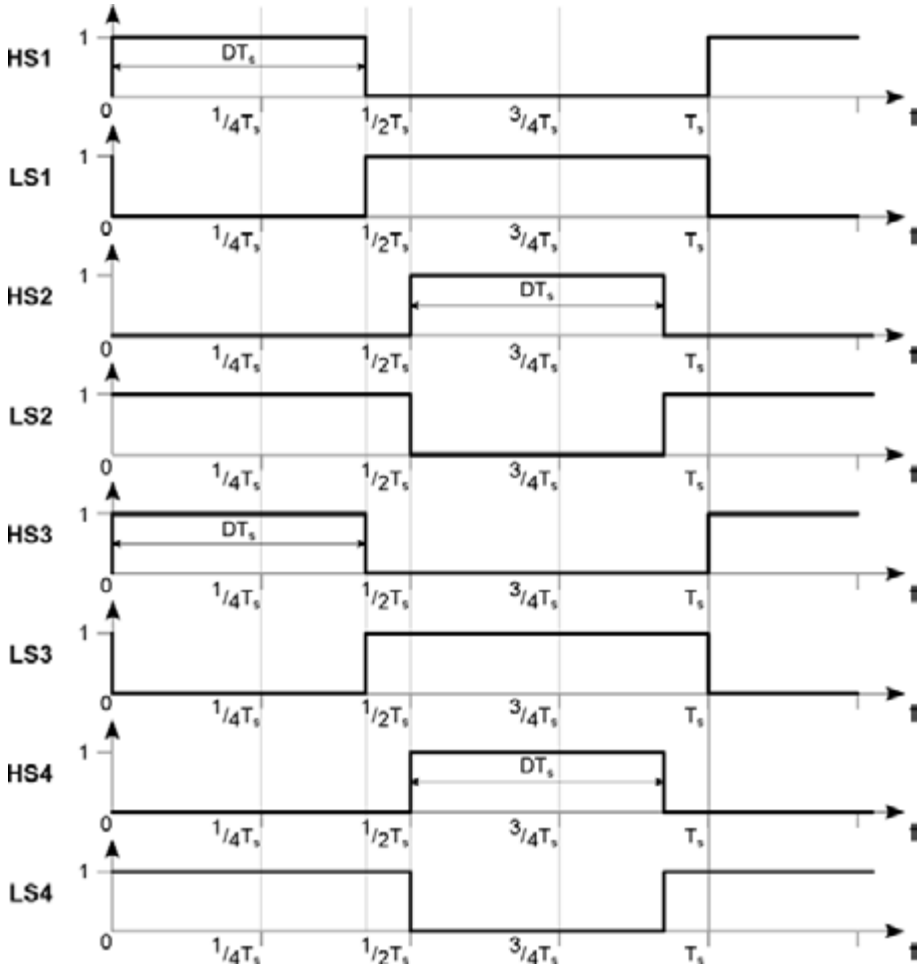


Fig. 2.4. *k=2* switching scheme logic signals.

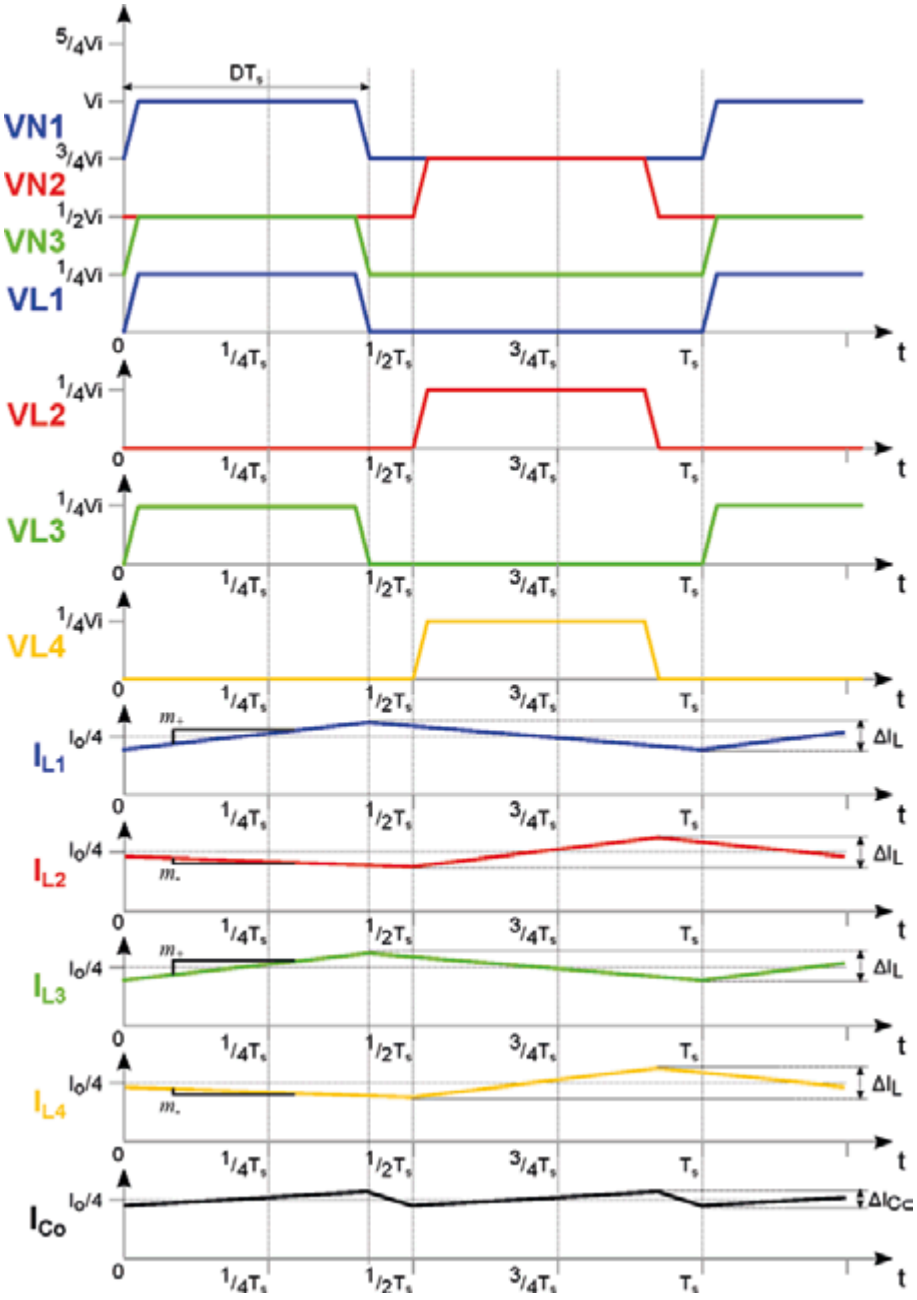


Fig. 2.5. *k=2* power stage voltage nodes and currents ideal waveforms.

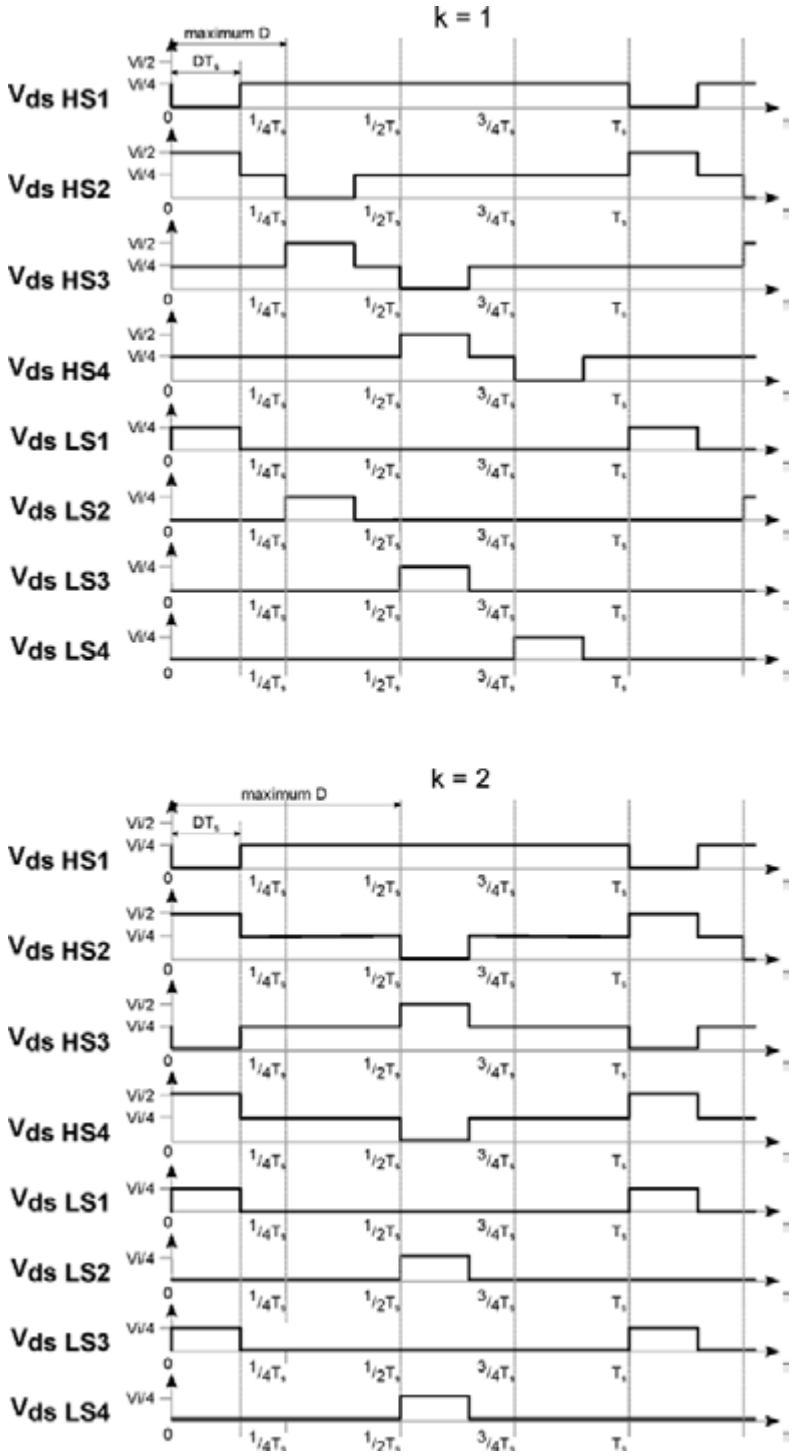


Fig. 2.6. Theoretical V_{ds} waveforms of HS and LS switches for $k = 1, 2$.

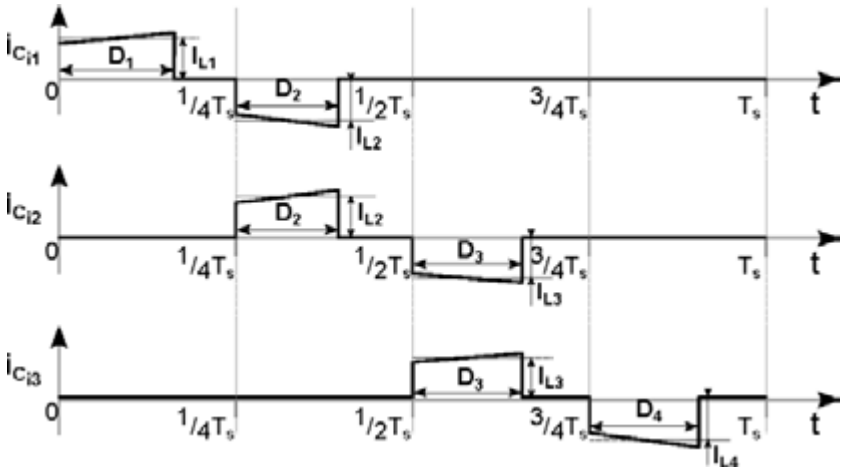


Fig. 2.7. Flying capacitor currents over a switching period.

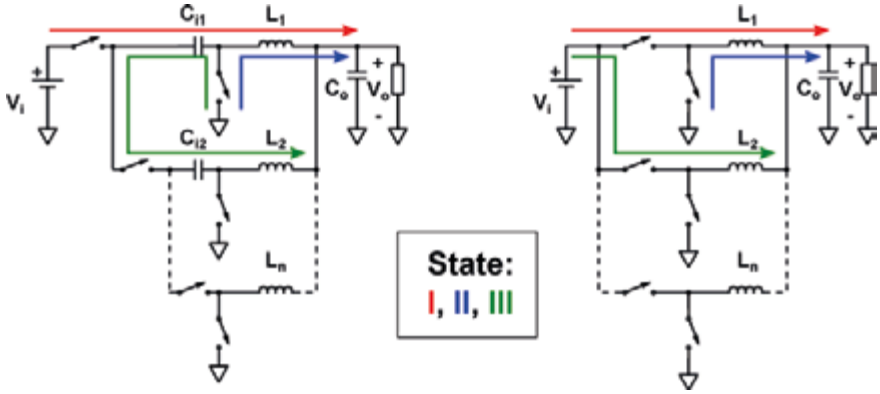


Fig. 2.8. Comparison of current paths for the first three switches states between generic multiphase buck (right) and high step-down (left).

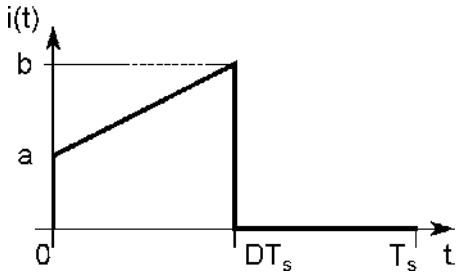


Fig. 2.9. Trapezoidal current pulse used to obtain RMS equivalent.

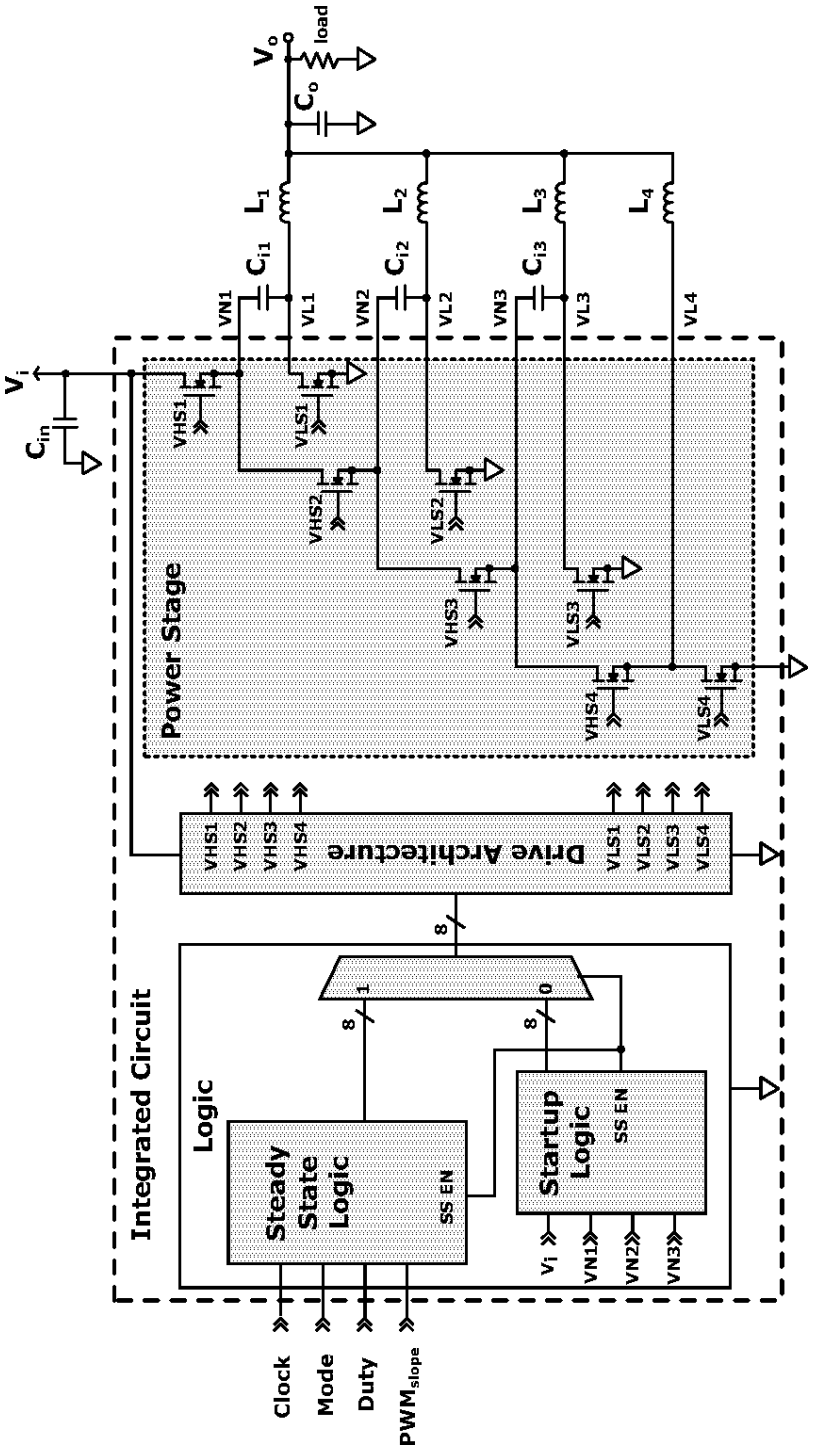


Fig. 2.10. Implemented High Step-down multiphase buck topology.

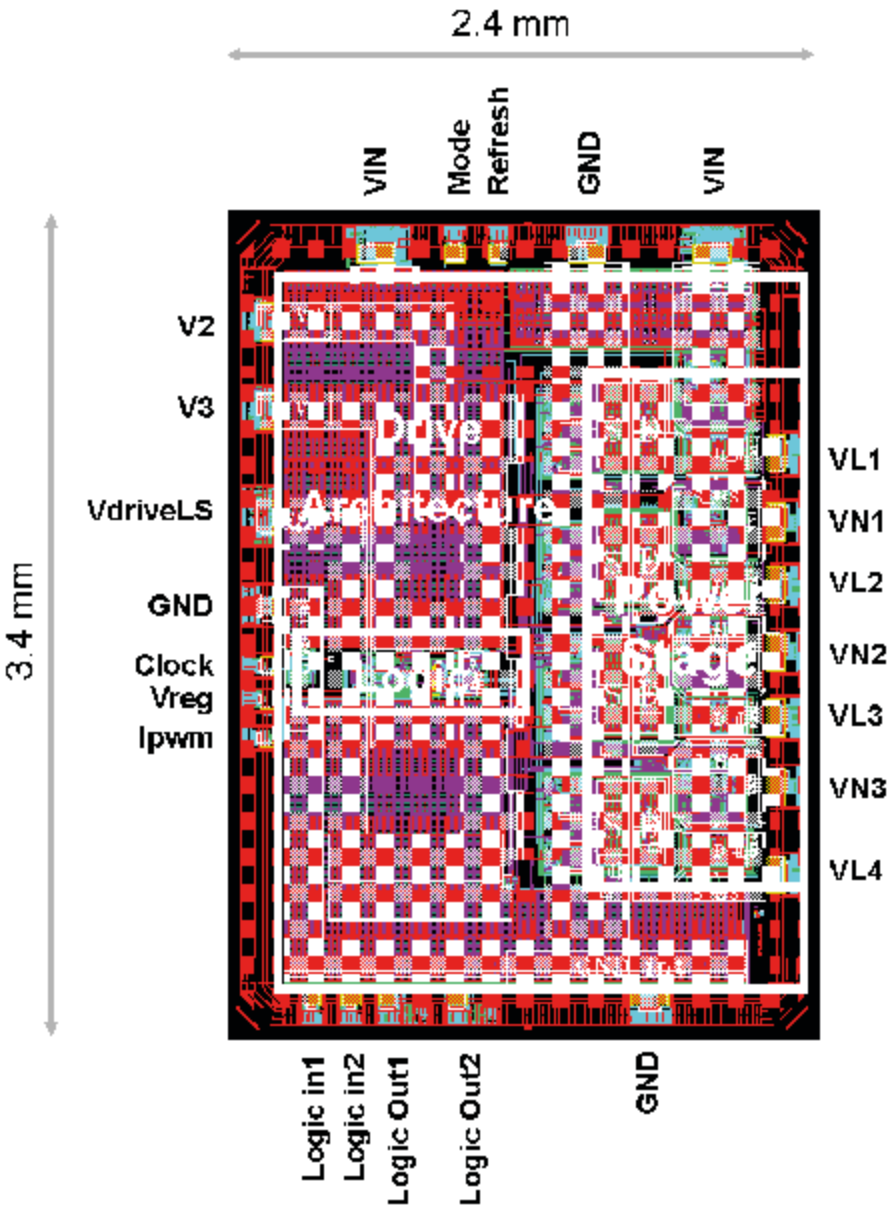


Fig. 2.11. Chip layout with areas highlighted by functionality.

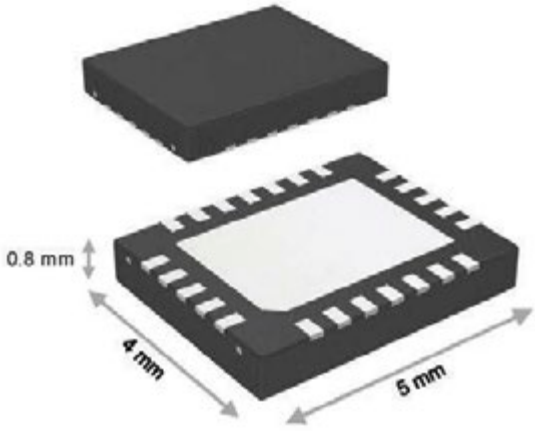


Fig. 2.12. 24 pin LLP package.

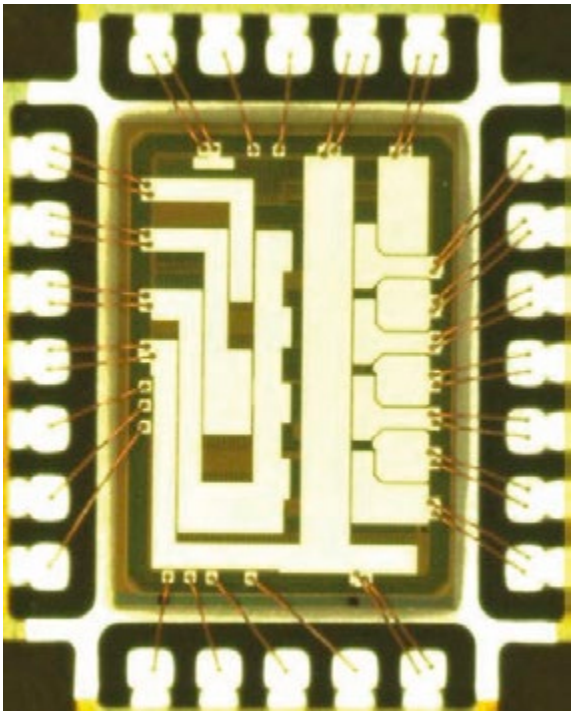


Fig. 2.13. Micro-photography of the die after wire bonding to the package leadframe.

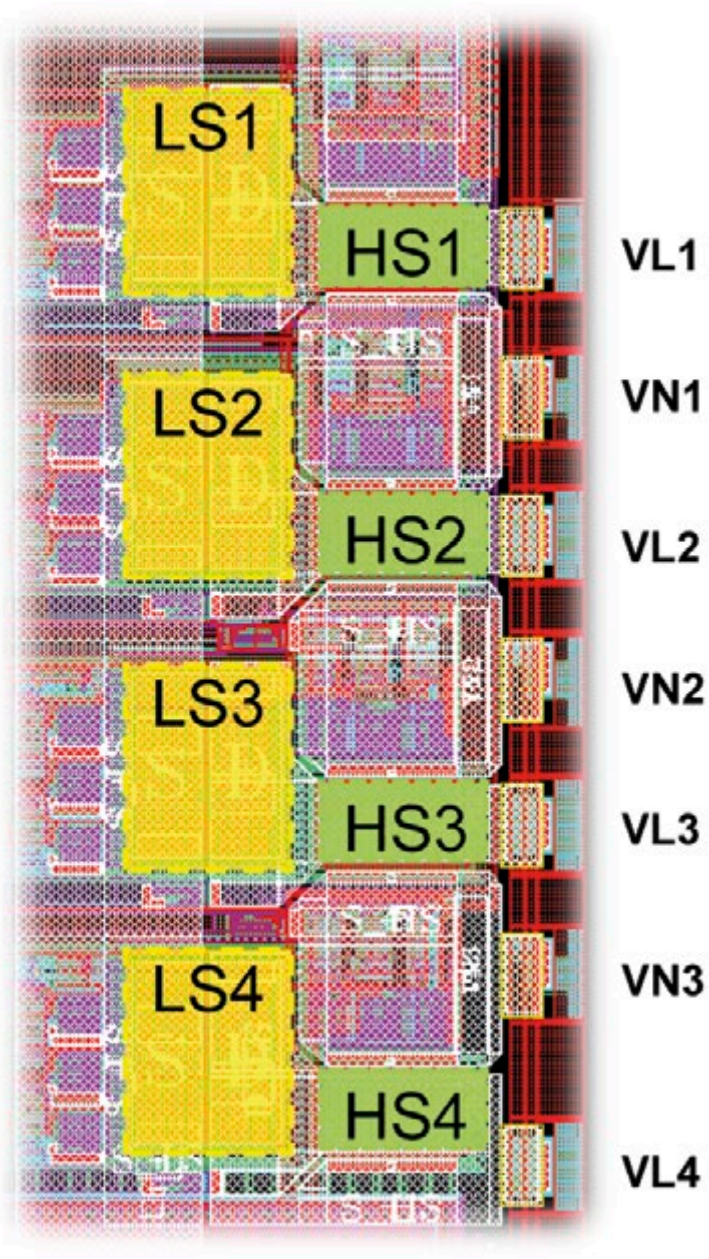
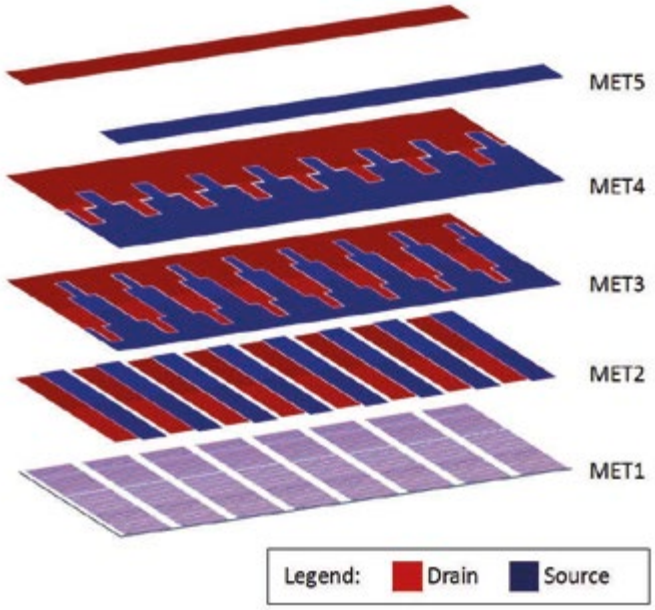
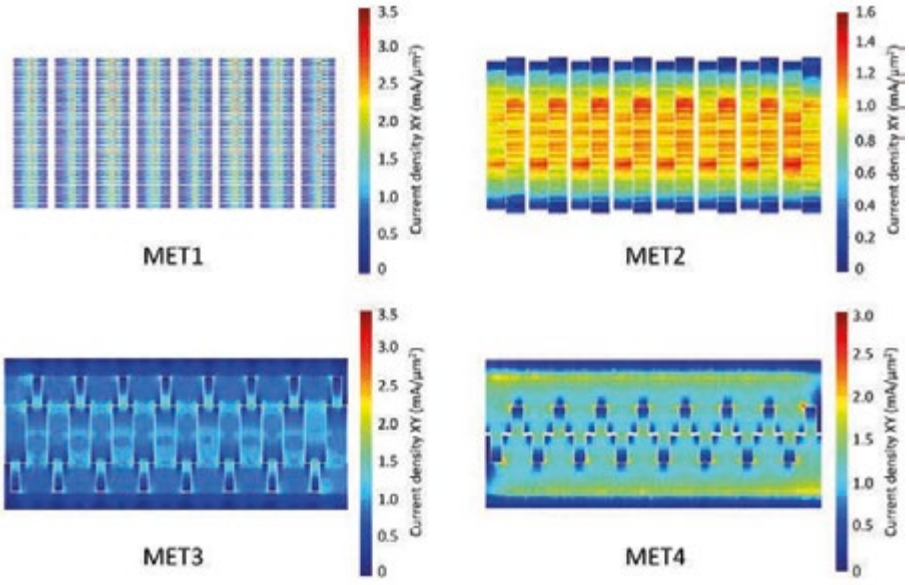


Fig. 2.14. Power stage layout with HS and LS switches highlighted to show their arrangement.



(a) Metal layers arrangement.



(b) Currents distributions [$mA/\mu m^2$].

Fig. 2.15. HS switch Drain and Source metal layers tapering and currents.

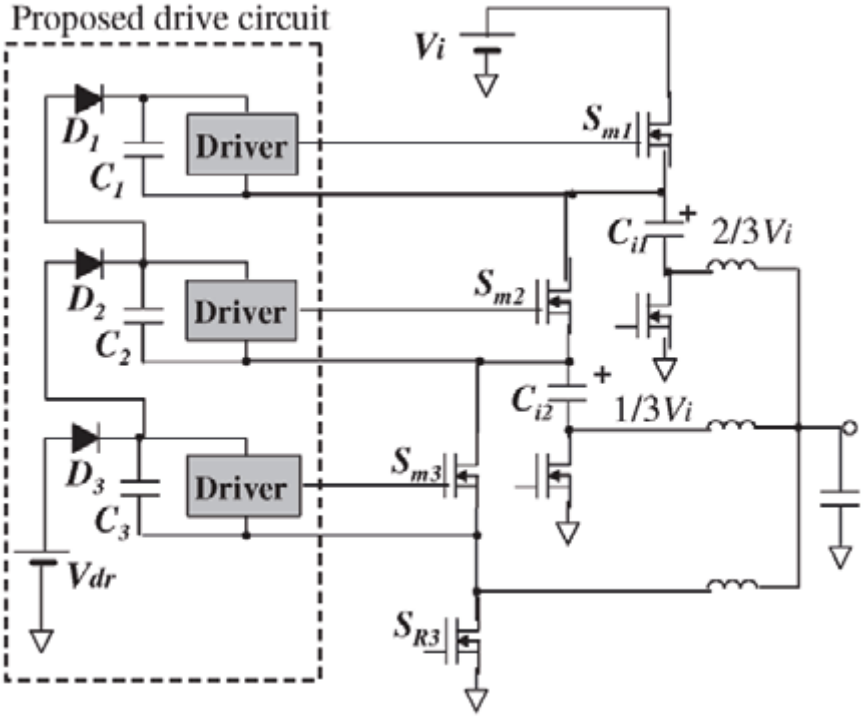


Fig. 2.16. HS drive architecture based on cascaded bootstrap stages proposed in [46].

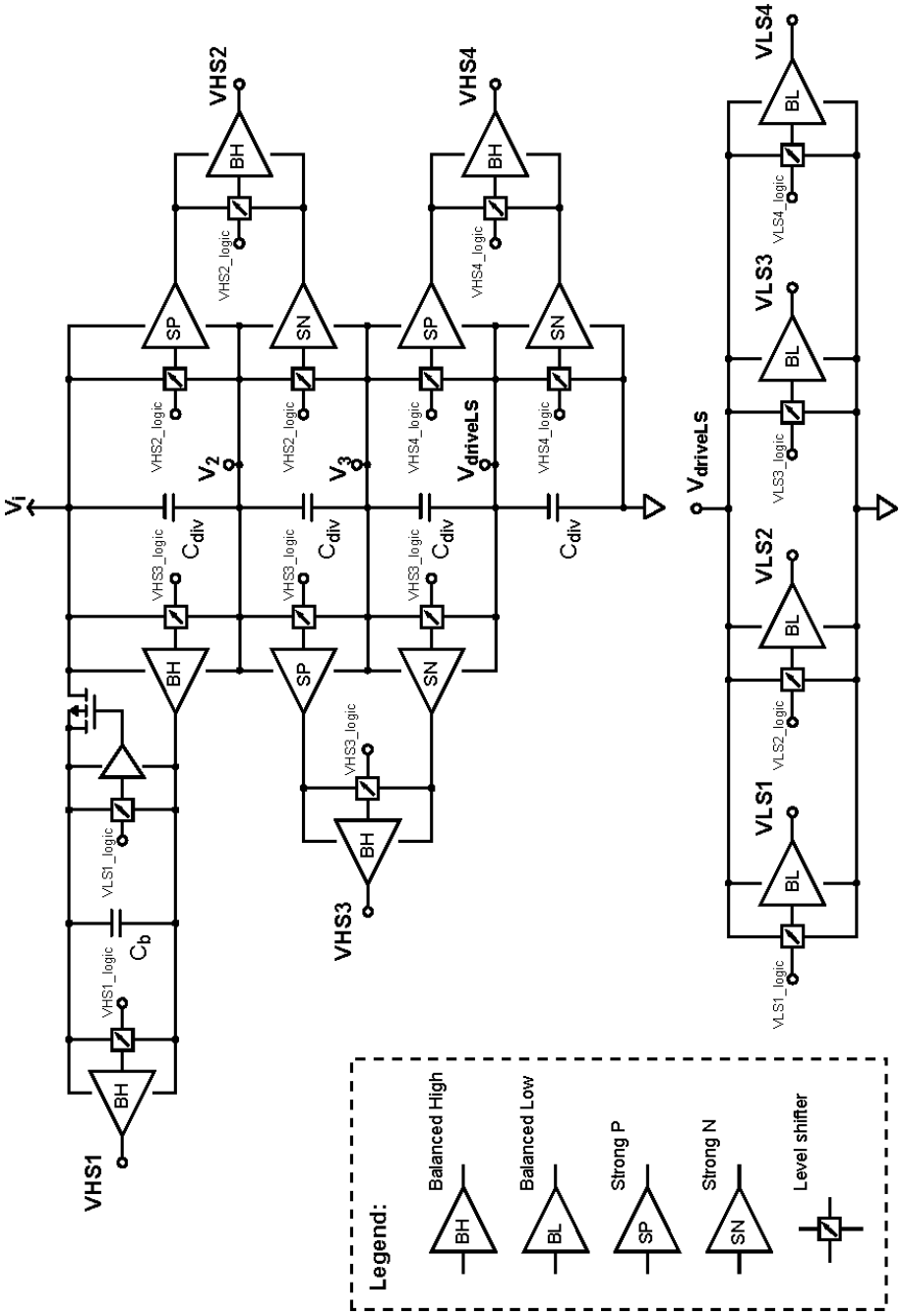


Fig. 2.17. Multi-voltage domain drive architecture scheme.

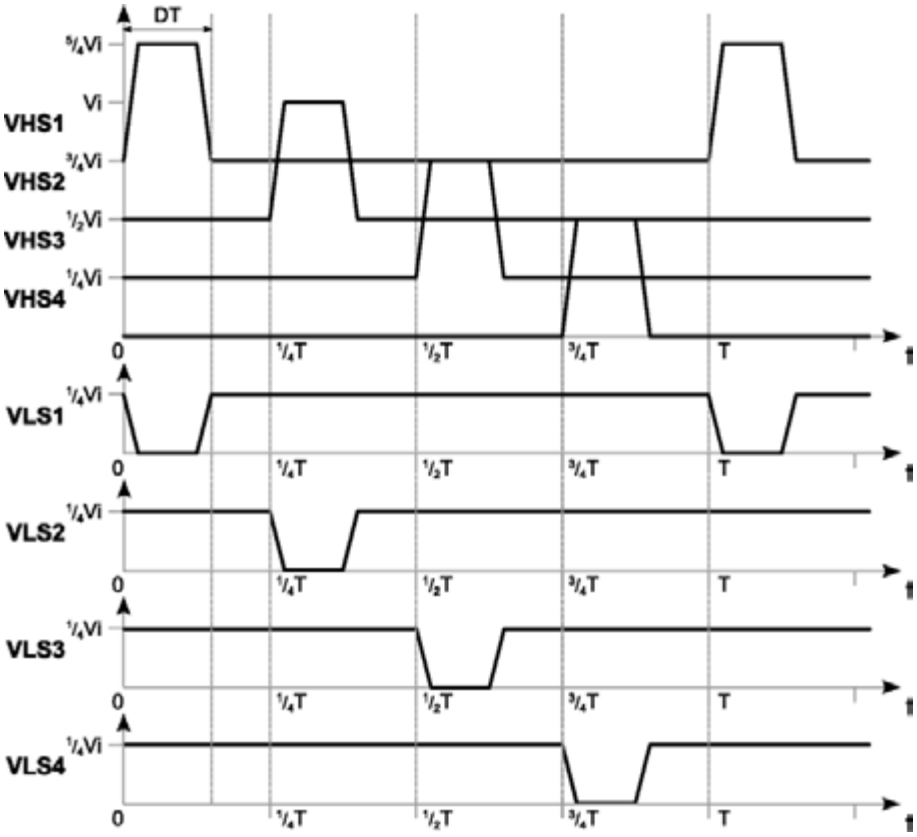


Fig. 2.18. Drive architecture theoretical output waveforms for *k = 1*.

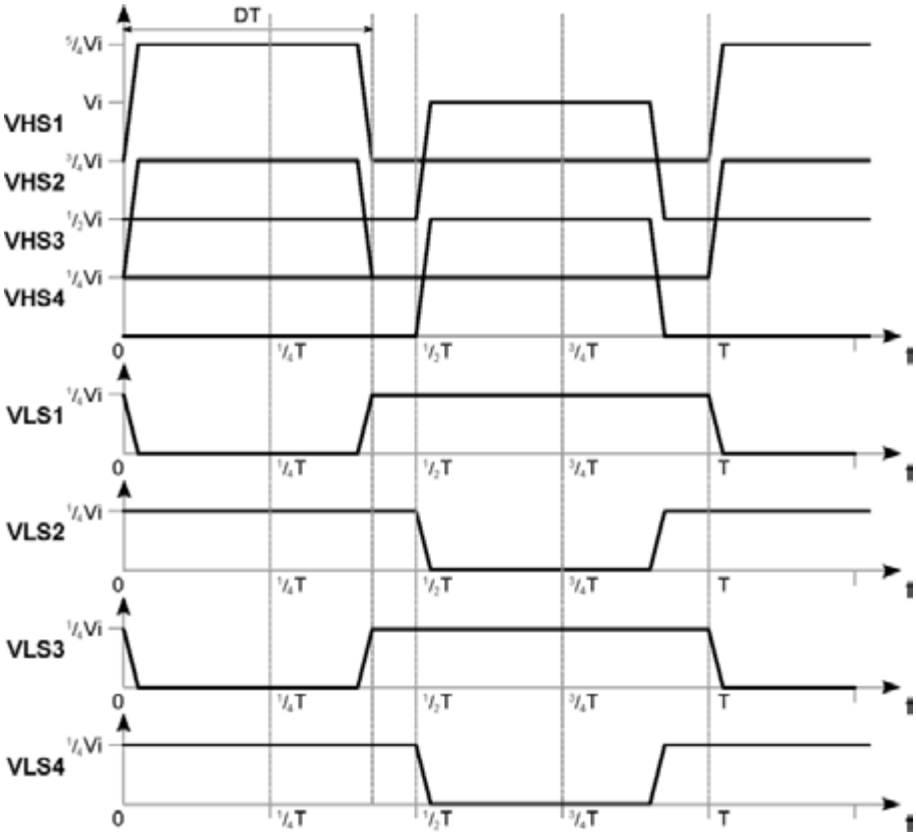


Fig. 2.19. Drive architecture theoretical output waveforms for $k = 2$.

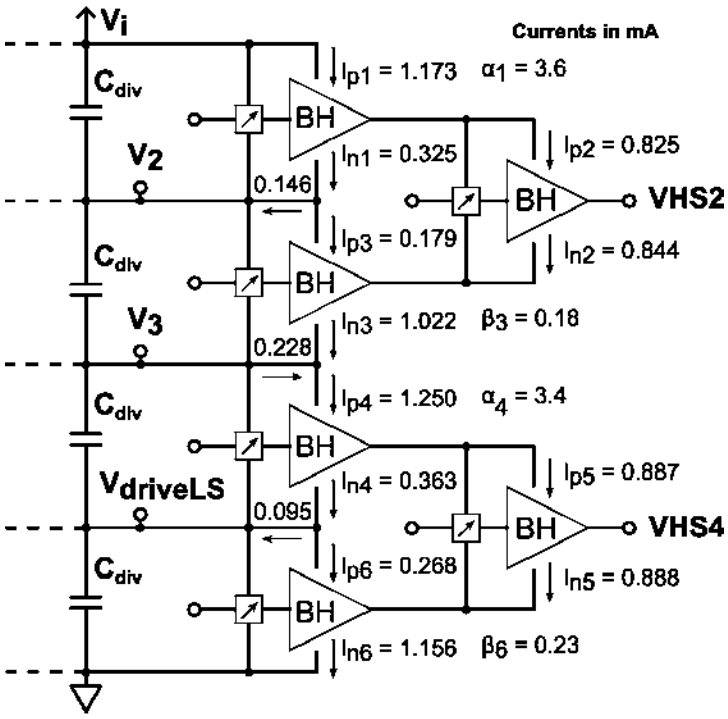


Fig. 2.20. Average currents over a switching period at HS drive architecture nodes.

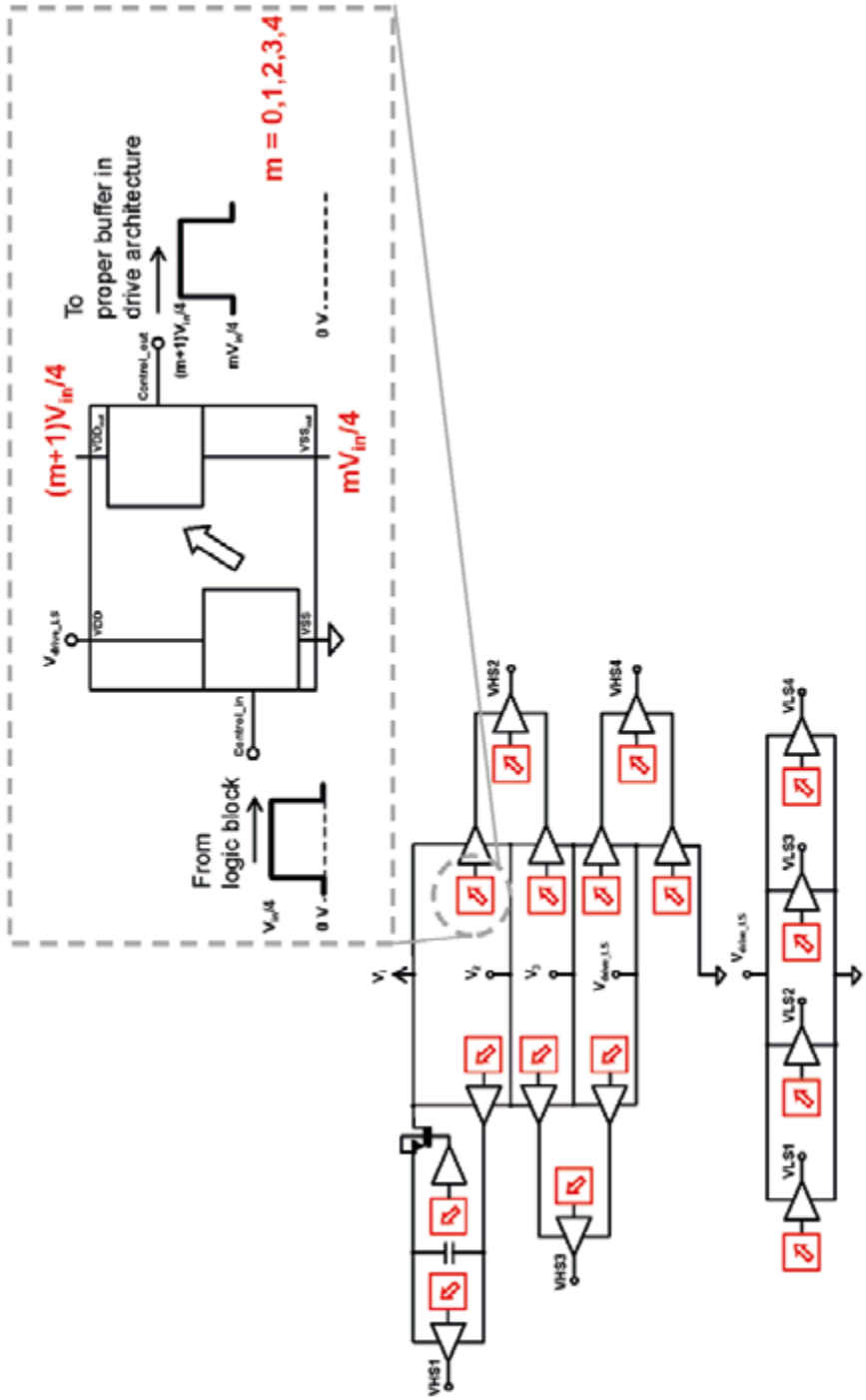


Fig. 2.21. Level shifter instances highlighted in the drive architecture and their generic functional scheme.

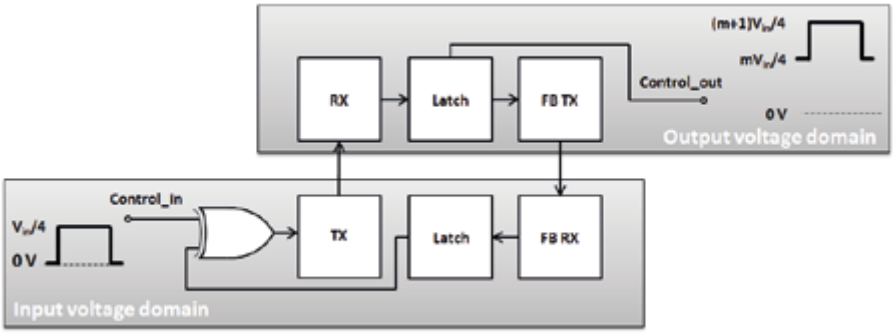


Fig. 2.22. Level shifter principle block scheme.

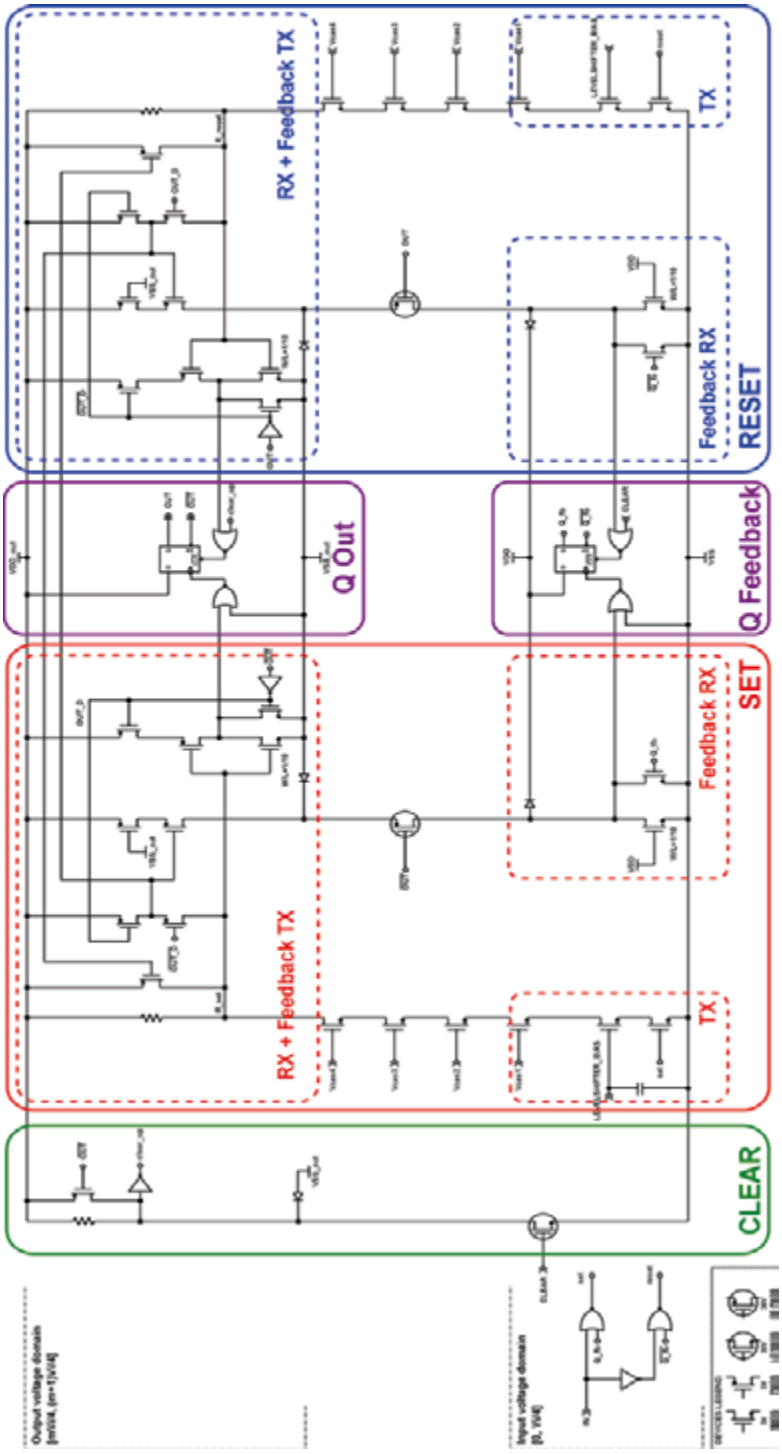


Fig. 2.23. Level shifter schematic with functional areas highlighted.

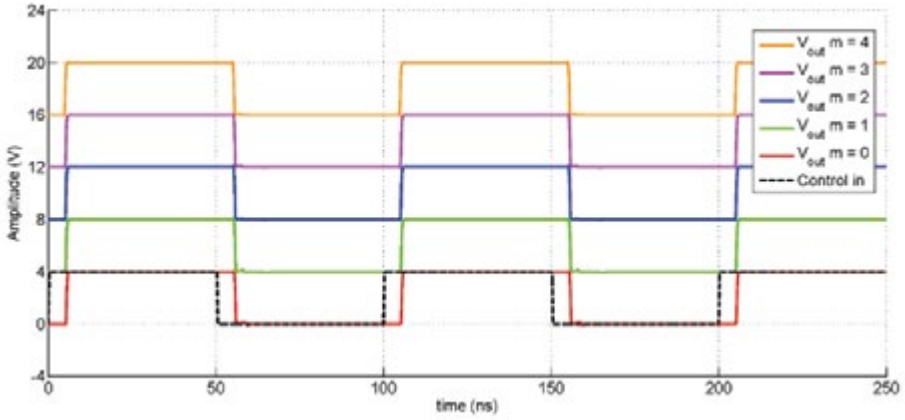


Fig. 2.24. Level shifter simulated output waveforms for different values of *m* with $f_s = 10\ MHz$, $V_i = 16\ V$.

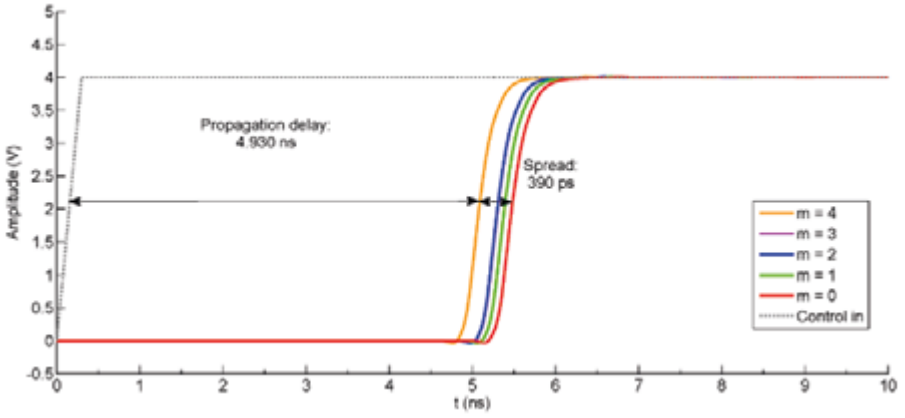


Fig. 2.25. Level shifter simulated output spread between translations with different *m* , $f_s = 10\ MHz$, $V_i = 16\ V$.

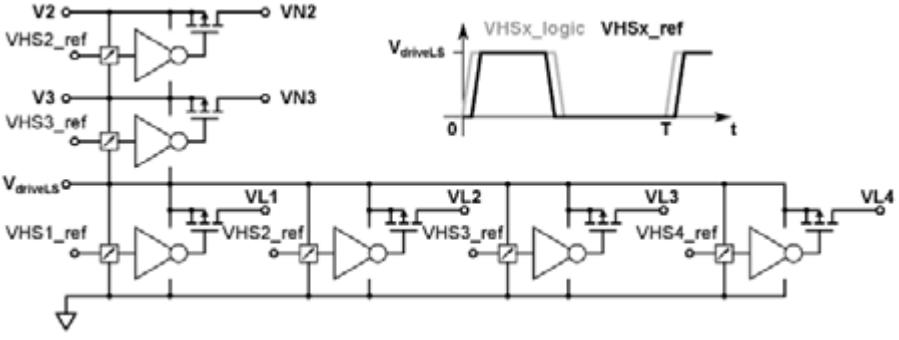


Fig. 2.26. Refresh architecture blocks.

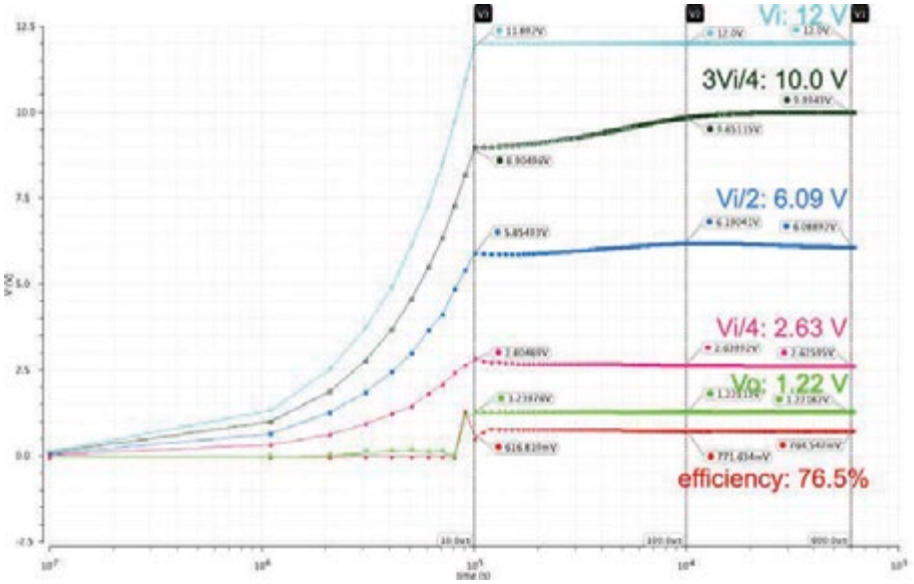


Fig. 2.27. Long-term transient simulation of capacitive divider voltages without refresh architecture. Waveforms report the final values after *600 μs*. Time axis is shown in log scale to emphasize variations.

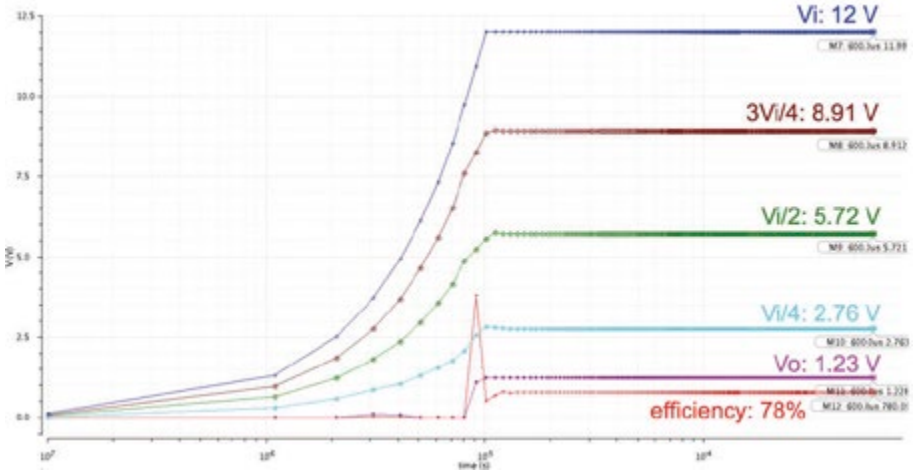


Fig. 2.28. Long-term transient of capacitive divider voltages with refresh architecture. Waveforms report the final values after *600 μs*. Time axis is shown in log scale to emphasize variations.

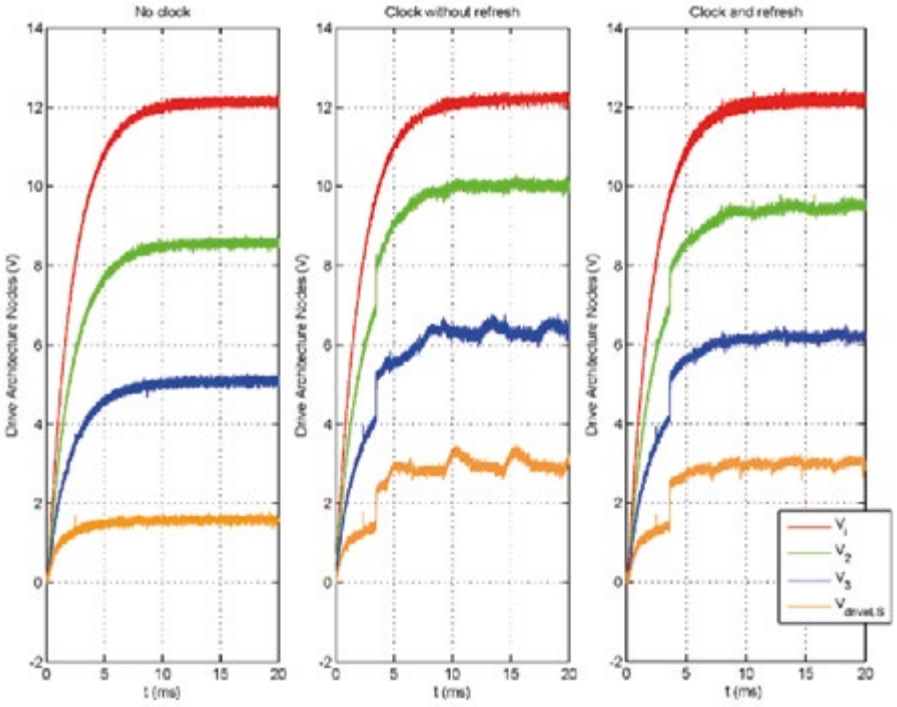


Fig. 2.29. Capacitive divider nodes' voltages at start-up. From left to right: no clock signal start-up showing the static drift of the nodes; clock signal allows the drivers to partially recover the voltage drifts; the activation of the refresh block additionally reduces the drift.

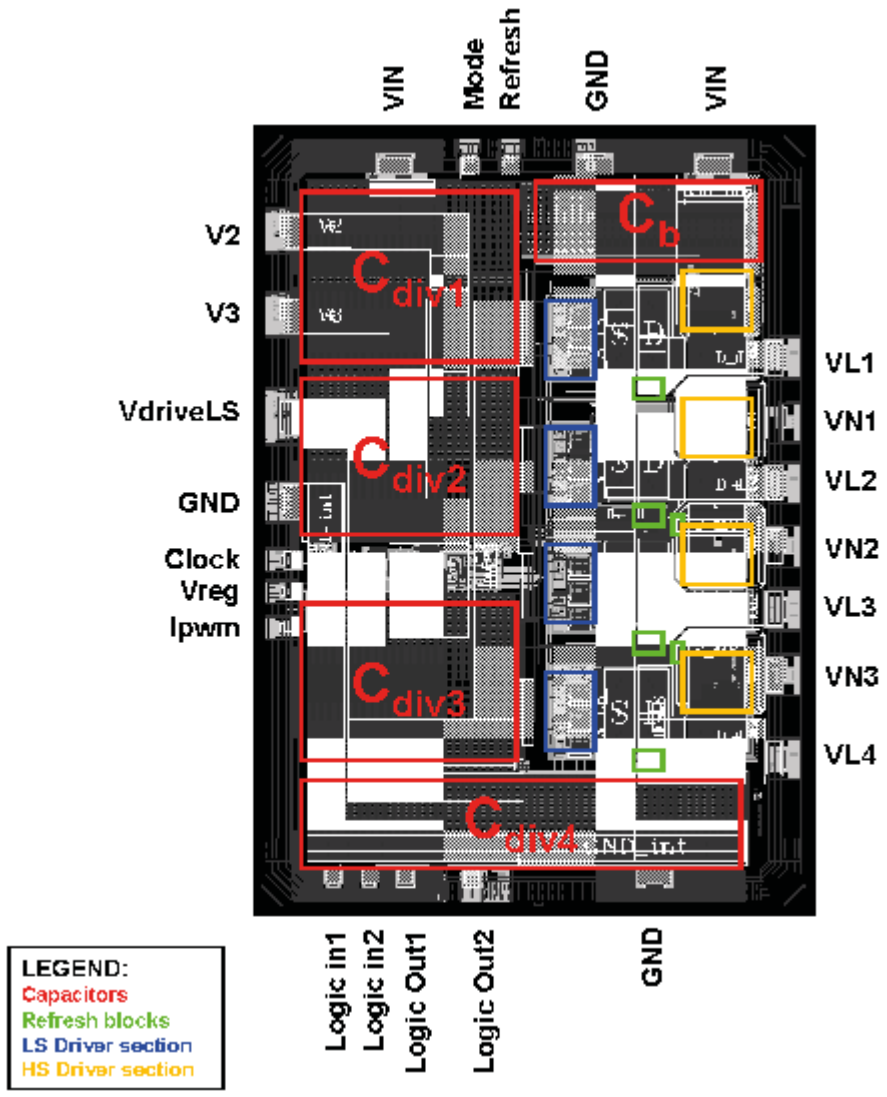


Fig. 2.30. Drive architecture blocks highlighted on chip layout.

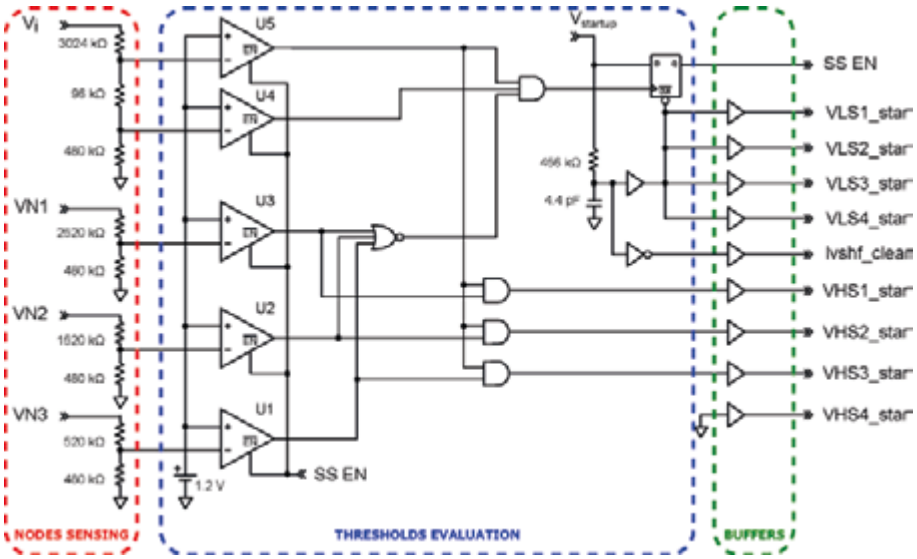


Fig. 2.31. Start-up logic principle scheme.

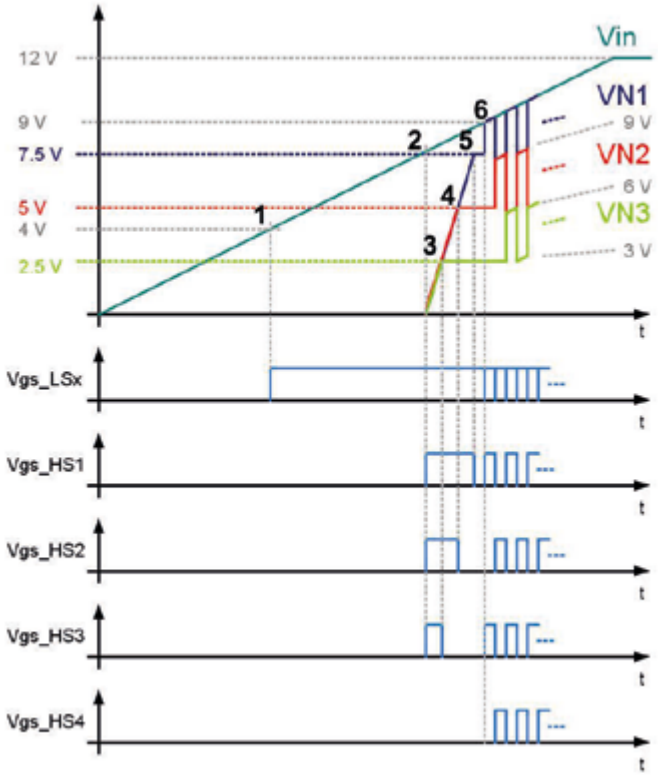


Fig. 2.32. Theoretical power stage's start-up waveforms and power switches' V_{gs}.

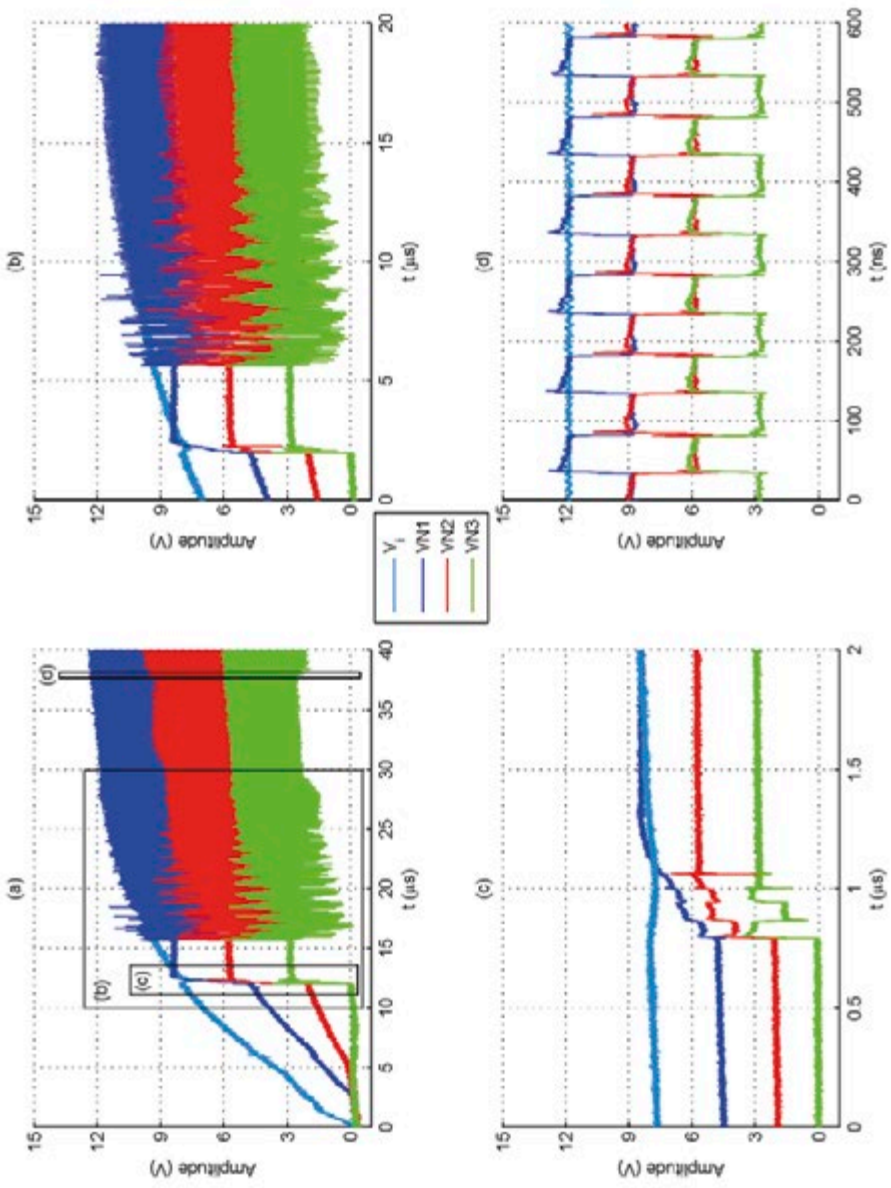


Fig. 2.33. Measured start-up with rise of V_i, VN1, VN2, VN3 nodes showing pre-charging of flying capacitors and steady-state switching.

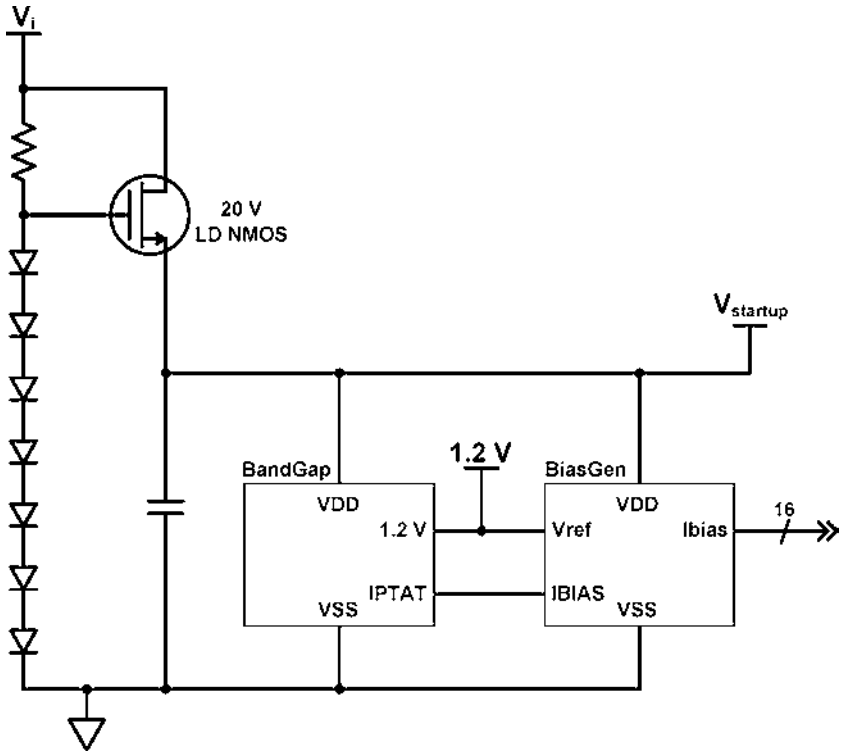


Fig. 2.34. Start-up voltage supply schematic with bandgap and bias current generators.

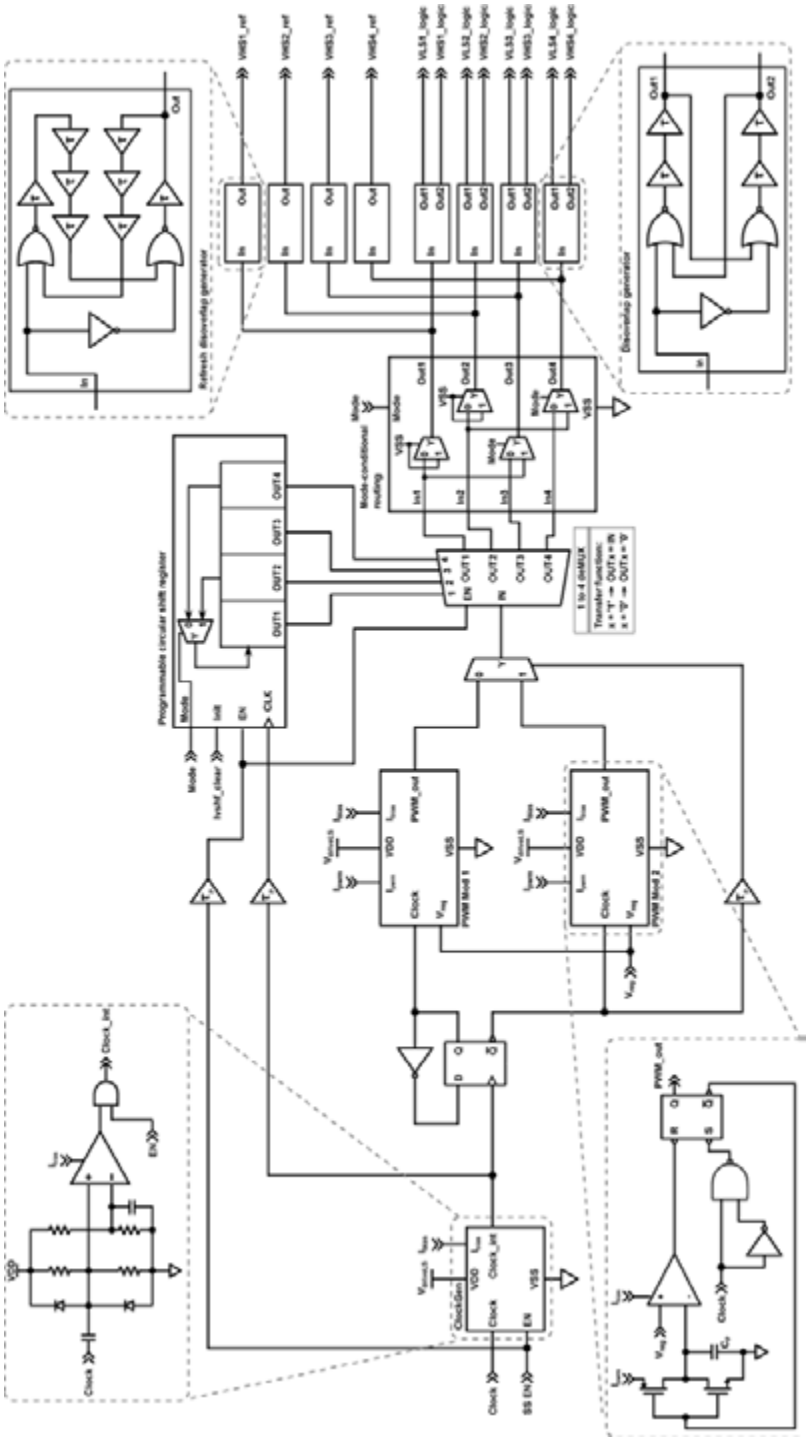


Fig. 2.35. Steady-state logic schematic.

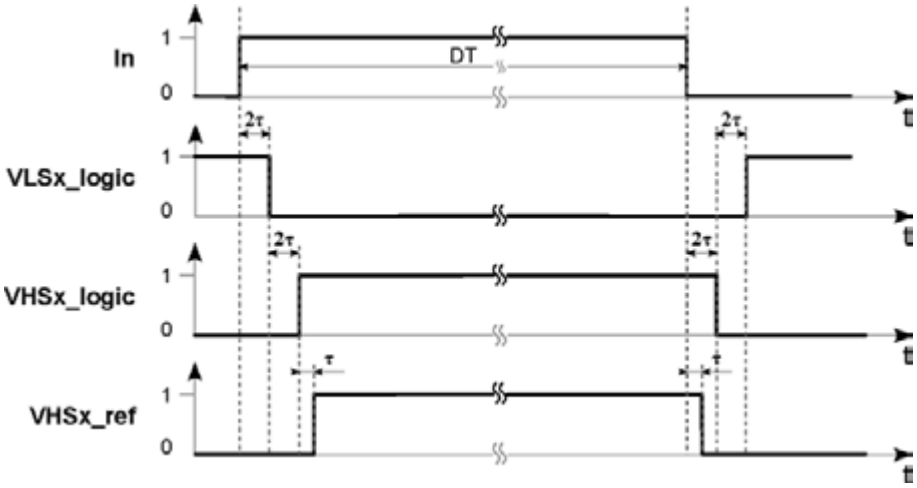


Fig. 2.36. Disoverlap generators outputs timing diagram.

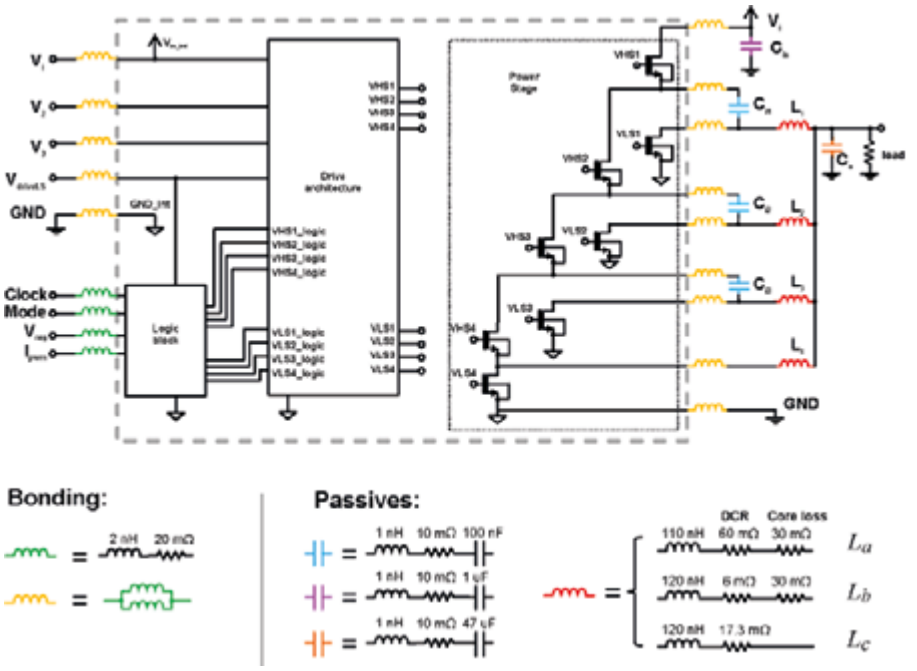


Fig. 2.37. Efficiency evaluation circuit including parasitics related to physical implementation.

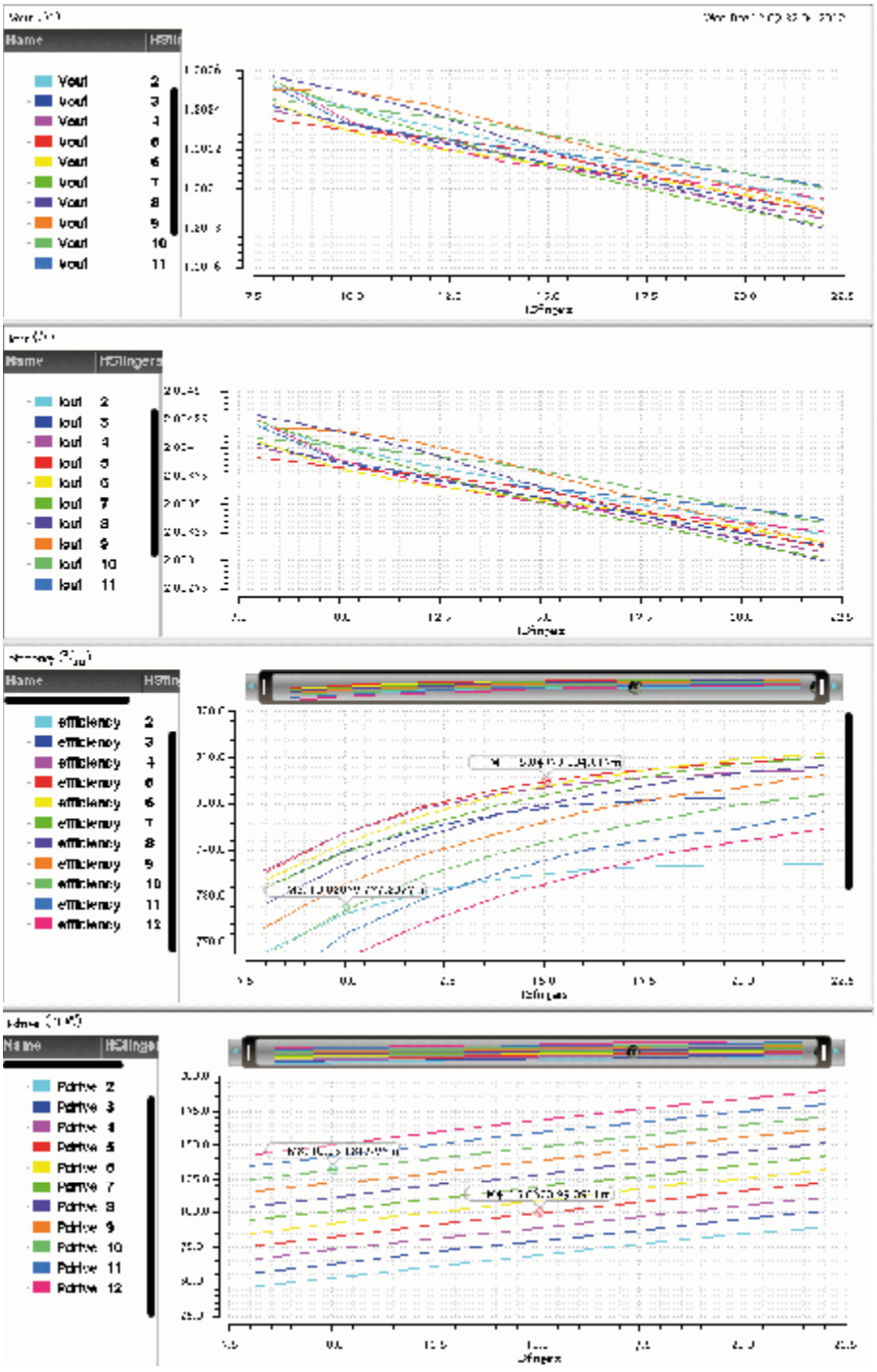


Fig. 2.38. Multi-parametric simulation results used to estimate power switches' optimal number of fingers.

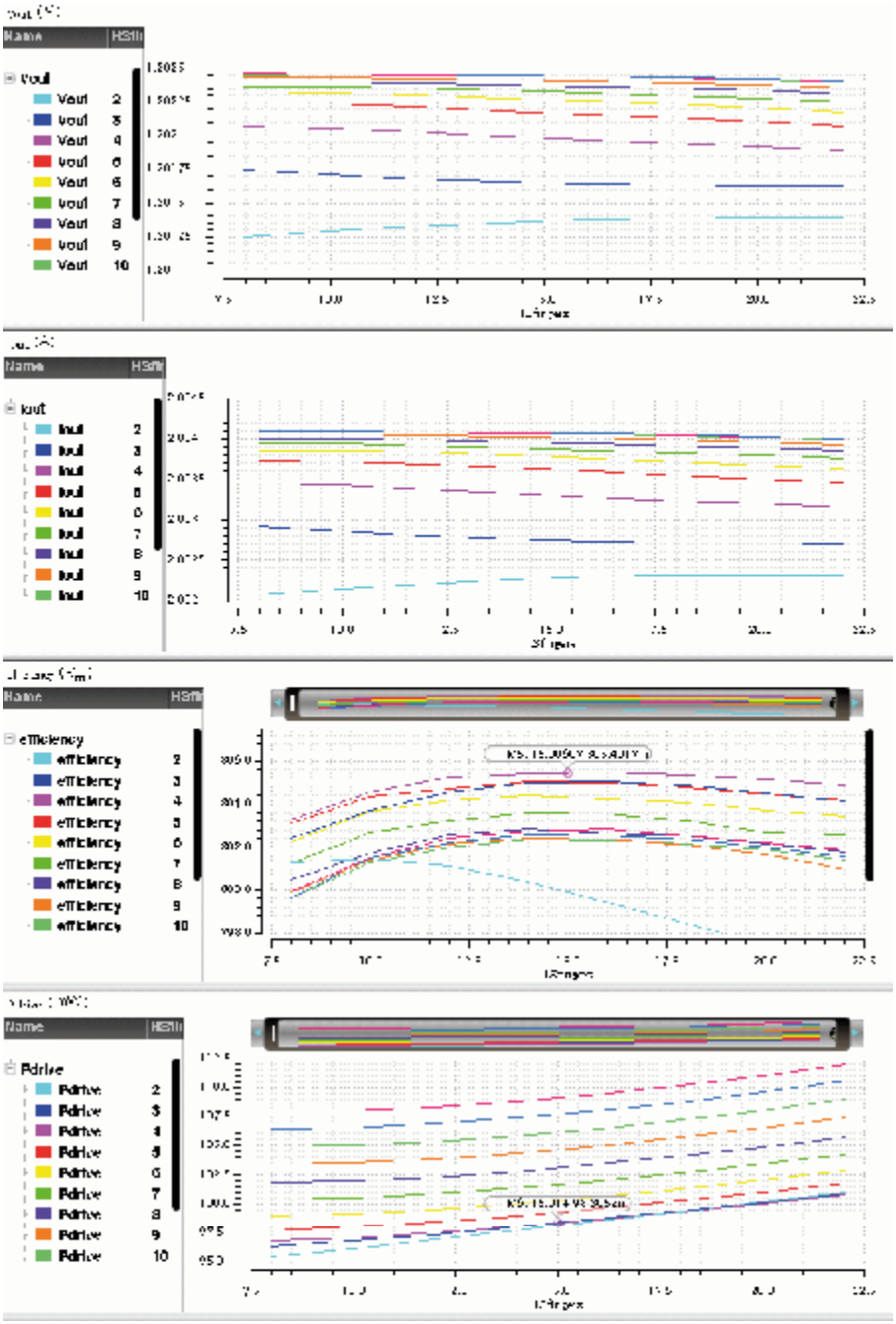


Fig. 2.39. Multi-parametric simulation results used to estimate optimal power switches' drivers sizes.

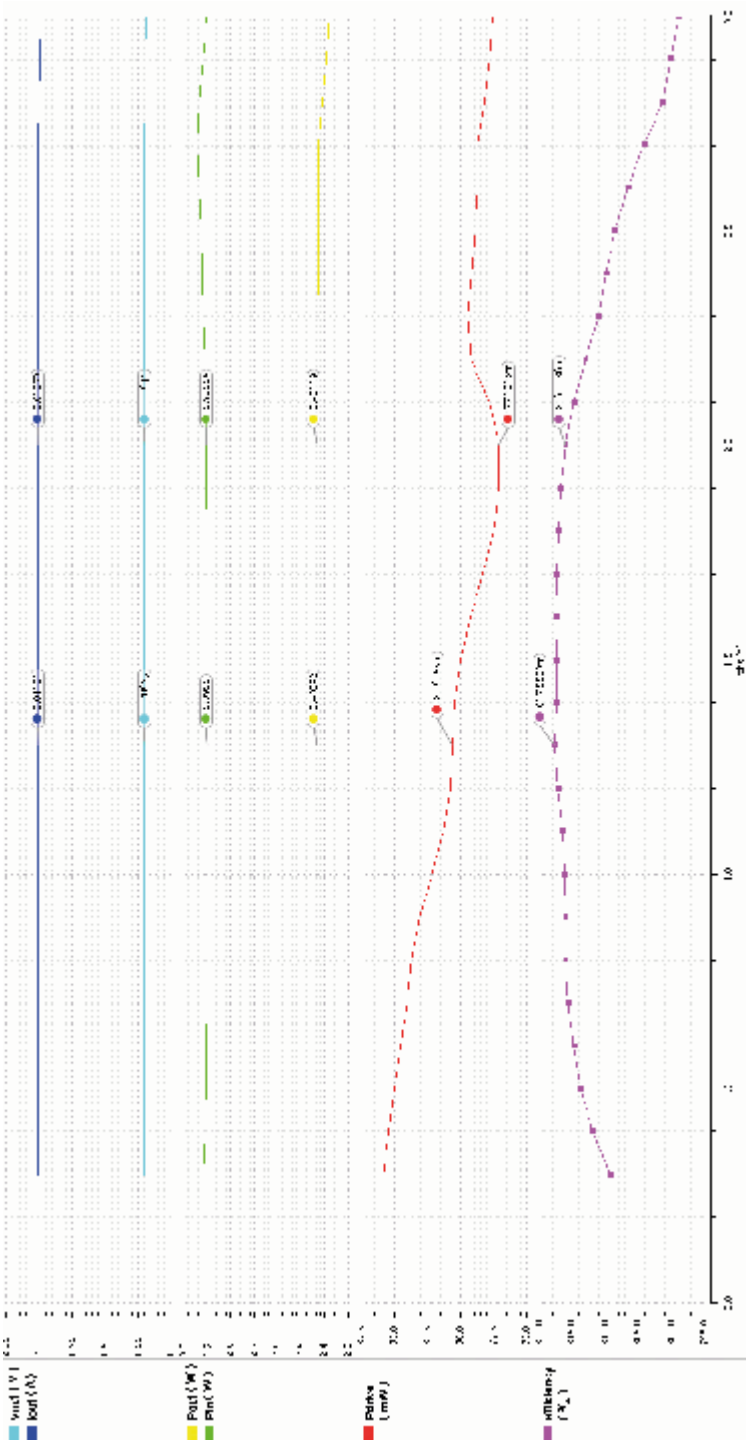


Fig. 2.40. Parametric simulation of disoverlap time t_{dis} versus efficiency.

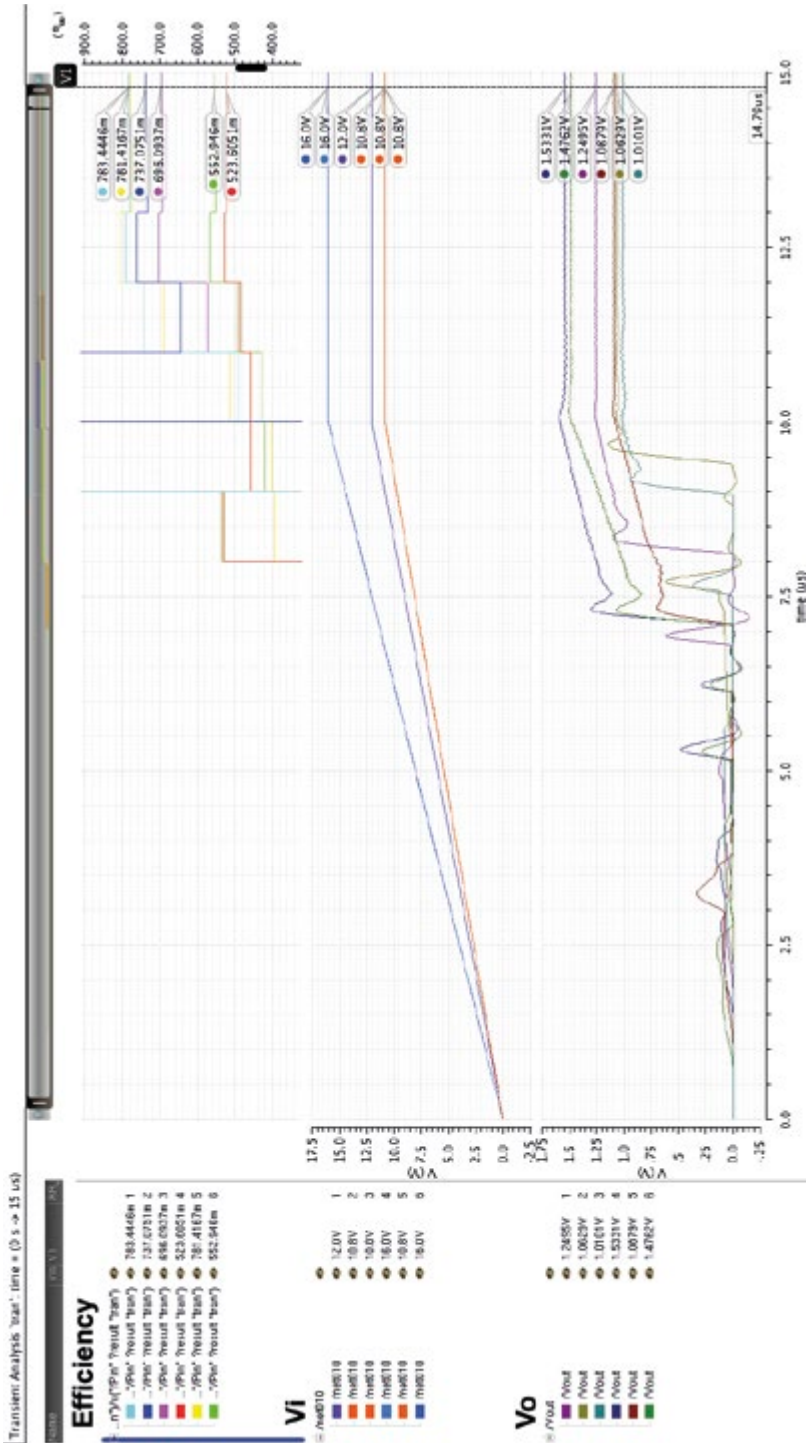


Fig. 2.41. Process' corners analysis done on start-up transient.

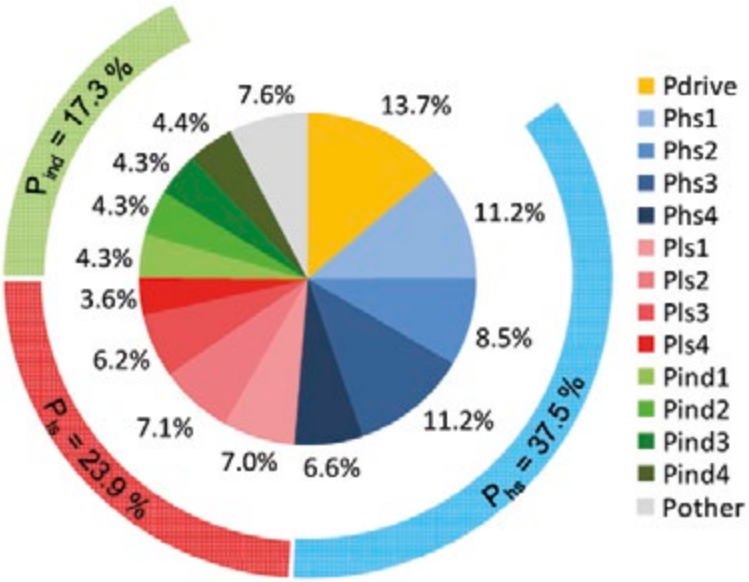


Fig. 2.42. Power losses pie chart.

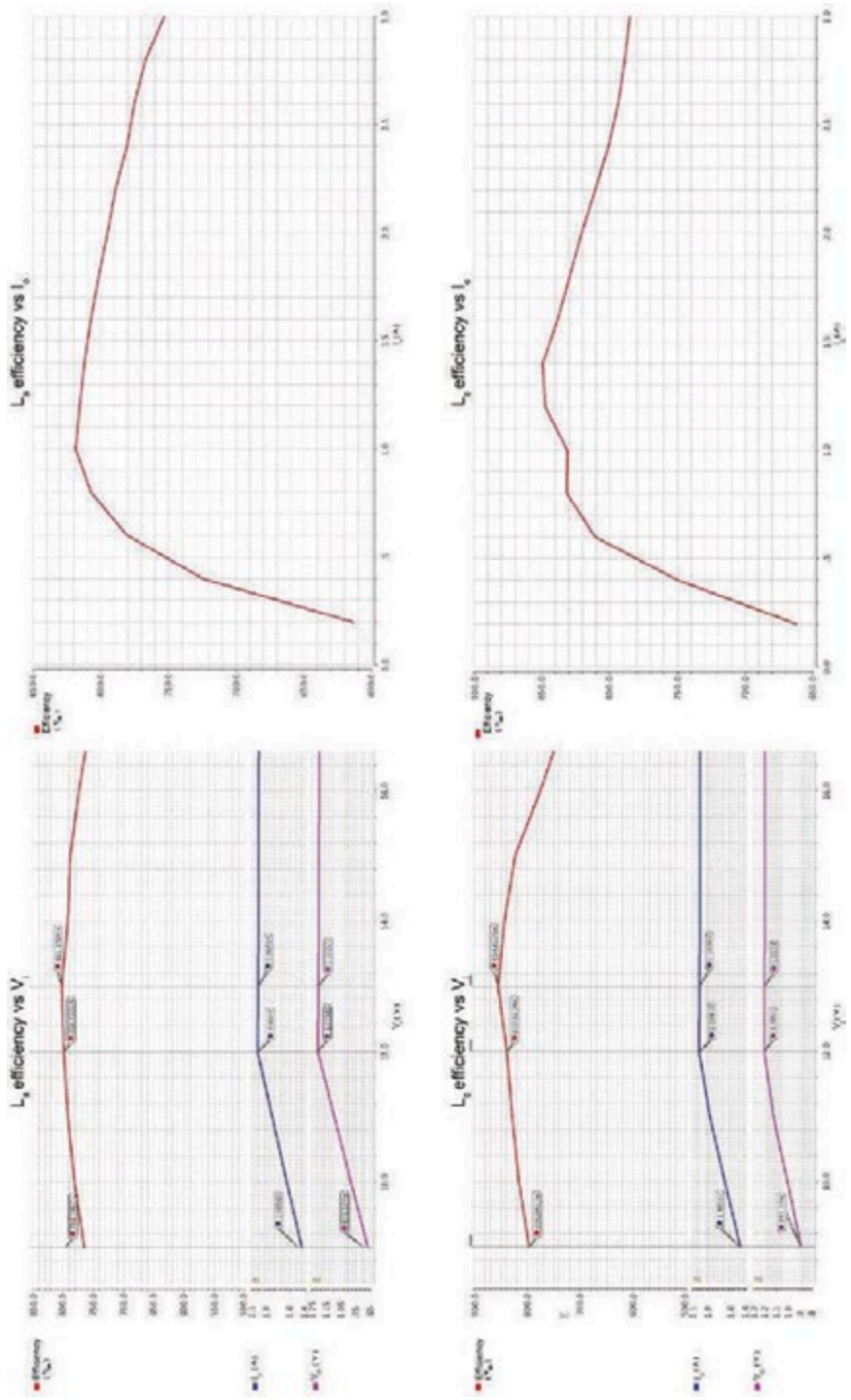


Fig. 2.43. Simulated efficiency versus V_i and efficiency versus I_o for inductors L_a and L_c.

Fig. 2.44. Mother and daughter PCBs designed to test the converter's performances.

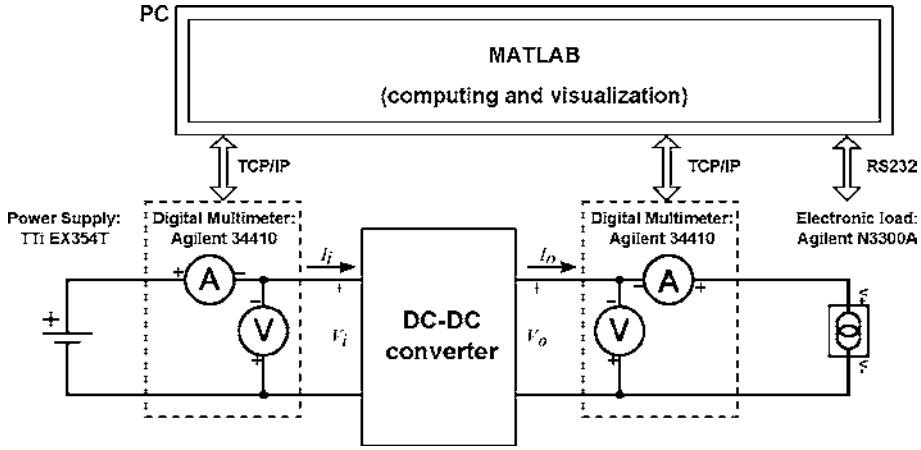


Fig. 2.45. Test chip measurement setup.

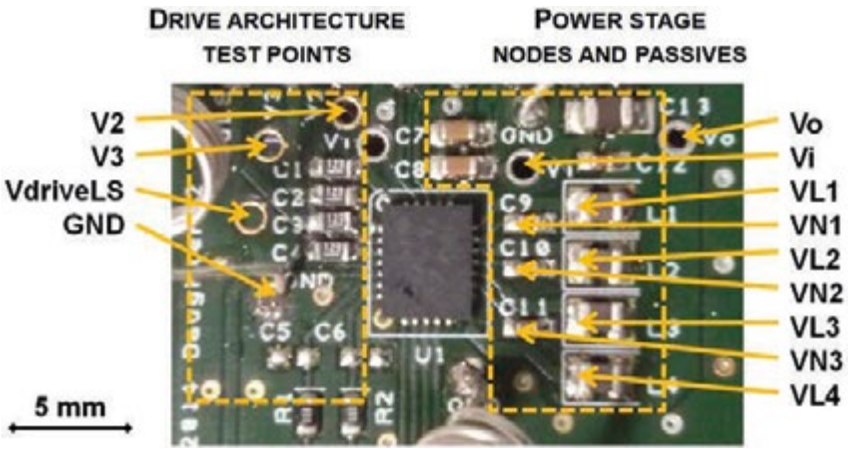
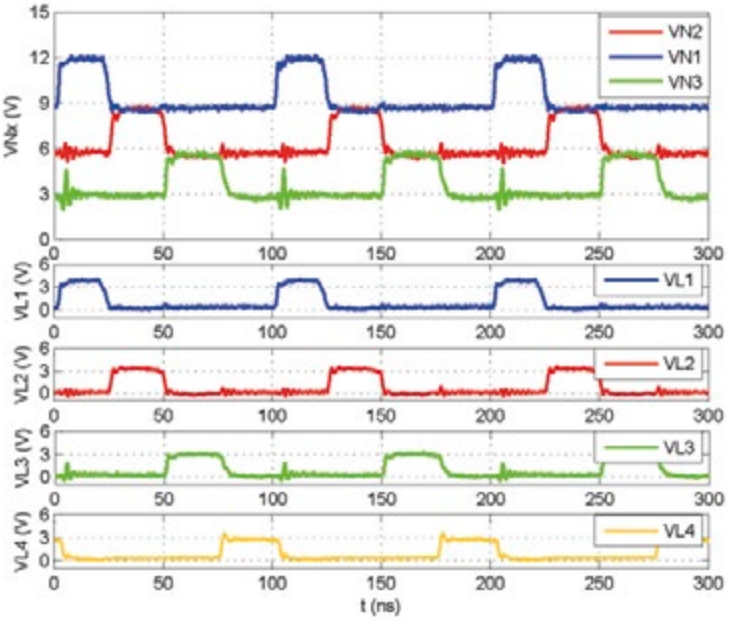
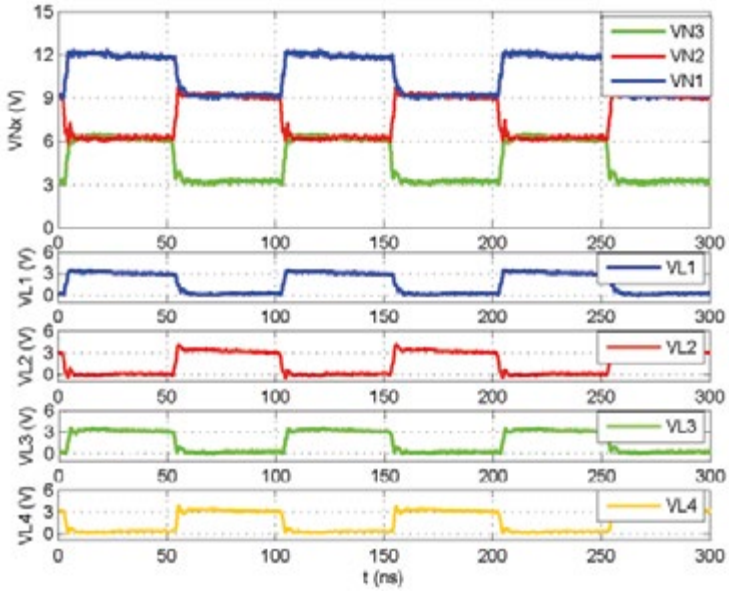


Fig. 2.46. Measurement test points highlighted on daughter board's PCB.

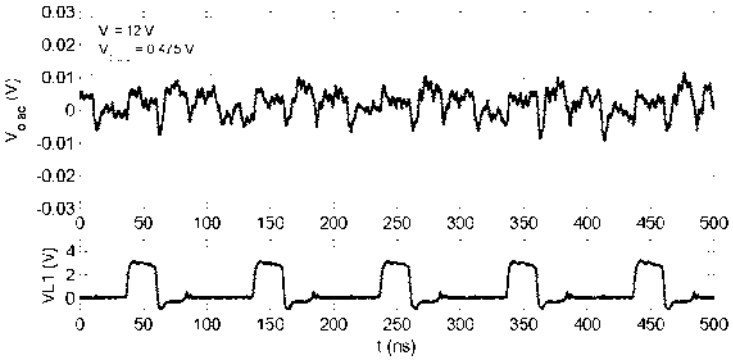


(a) $k = 1$ switching mode.

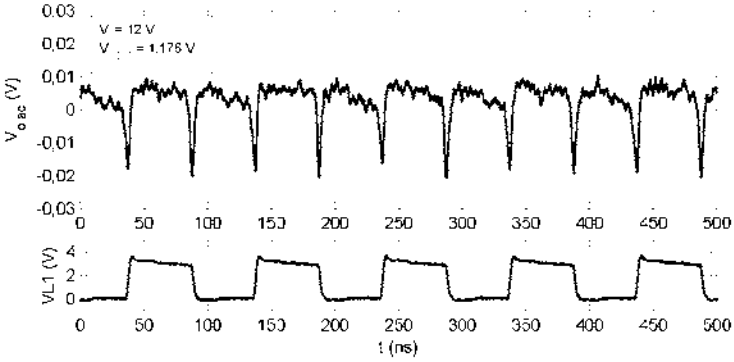


(b) $k = 2$ switching mode.

Fig. 2.47. Measured power stage nodes voltage waveforms for $V_i = 12\ V$. Node labels are referred to Fig. 2.10.



(a) Output AC voltage ripple with $k = 1$.



(b) Output AC voltage ripple with $k = 2$.

Fig. 2.48. Measured output voltage ripples for $V_i = 12\ V$, $I_o = 2\ A$. Oscilloscope bandwidth limited to *150 MHz*. VL1 node voltage is reported to demonstrate increment in ripple frequency with respect to f_s.

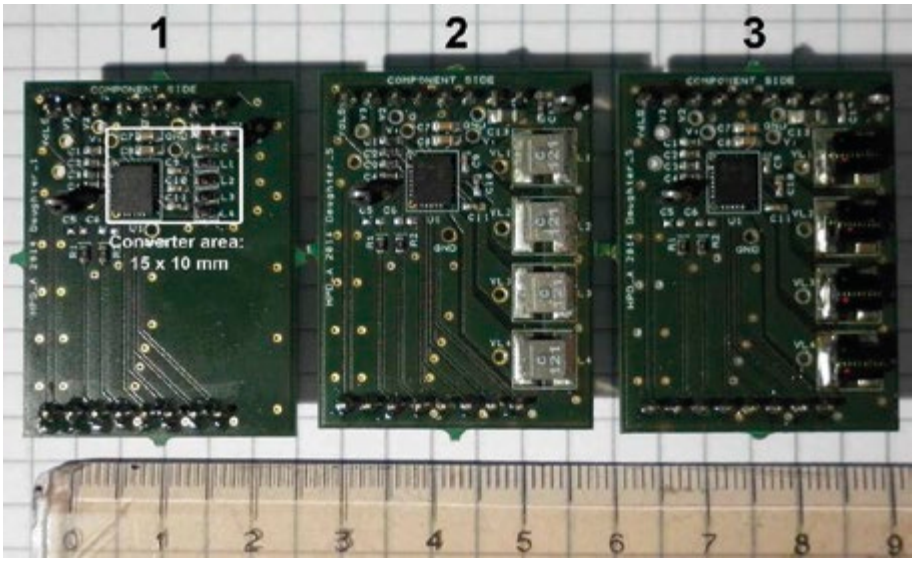


Fig. 2.49. Different solutions tested for inductors and PCB arrangements.

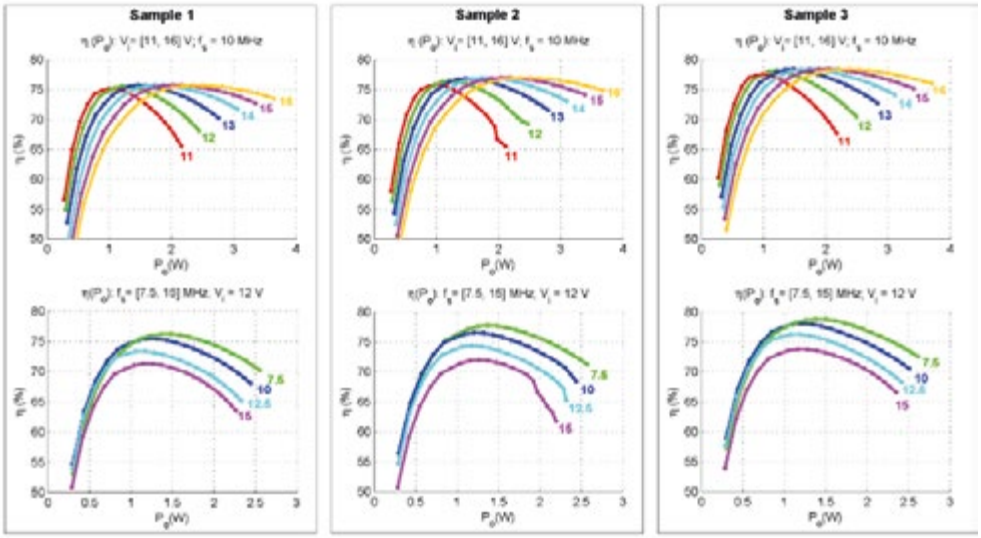


Fig. 2.50. Efficiency as function of output power P_o for the converters of Fig. 2.49. First row shows efficiency as V_i varies, second row as f_s varies.

Chapter 3
High power density stackable flyback architecture

Previous chapter has shown the increment in terms of power density obtained combining integration and a proper direct energy transfer topology aiming at high step-down conversion ratio. Main benefits with respect to a multiphase buck are the reduction of both voltage and current stress on the components allowing their size reduction. The same concepts can be applied to indirect energy transfer topologies. This chapter presents a preliminary study done on the design of a high frequency low-voltage stackable flyback architecture. Starting from considerations on actual solutions and the availability of integrated high frequency micro-transformers, a script which allows to define the requirements needed to design a custom micro-transformer is presented. The script has been used together with a simulation test-bench in order to do a preliminary evaluation towards the design of a discrete prototype. These results are applied to an evaluation of different solutions for the implementation of main switch.

3.1 Topology overview

The low-voltage stackable flyback (LVSF) converter, which is shown in Fig. 3.1, has been studied and designed at the University of Toronto. The results presented in [31] are obtained with a *12* to *1 V*, *4 A*, *500kHz* 2-cell stacked flyback converter prototype providing a *14 %* smaller output capacitor, up to *40 %* lower power losses, and *33 %* faster transient response when compared to an equivalent *12 V,* 2-phase conventional multiphase buck with approximately the same inductor volume. These volume reductions are provided exploiting two principal advantages. The first one is directly related to topology, which provides an input voltage sharing among the stacked cells (series connection at inductors' primary sides) and an output current sharing (parallel connection at inductors' secondary sides). This combination allows a reduction of the voltage and current stress of components minimizing also the inductors' voltage swing. The same considerations widely explained in the previous chapters are still valid, so switches with lower voltage rating can be used together with inductors with smaller inductance values. The second advantage is related to the sizing of the output capacitance, where a reduction is achieved when comparing with multiphase buck. This reduction is enabled exploiting a minimum deviation controller technique which relaxes the requirements on output capacitance value related to transient voltage deviations.

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3.1.1 Minimum deviation controller

This converter has a complementary mixed-signal controller designed following the minimum deviation method [33]. This control technique allows to enhance the transient response of the topology in terms of minimum deviation from the steady-state values of output voltage and current when a load transient is applied. By operating a two-steps method, the PID controller regulation is suspended when a transient is detected. A dedicated transient suppression logic is used to control the switches during the transient recovery in such a way that the overcurrent stress on the inductors is reduced with respect to the PID response. The output capacitor's current sign is used to evaluate value when the current value is close to the next steady-state. When this happens, the PID regulation is resumed.

3.2 Miniaturization of the stackable flyback

The converter topology has been implemented using discrete components for the power stage and a controller based on both FPGA and discrete components [31]. The switching frequency of *500 kHz* has allowed a reduced effort in terms of both discrete and controller implementation.

The aim of this study is to investigate the potential for increased level of integration, which would allow the use of this topology in mobile and other applications where the high power density and small dimensions are of a key importance. In order to achieve an increment in terms of power density with respect to the presented solution, an increment of switching frequency to reduce the sizes of required passives, together with a dedicated integrated implementation, can be evaluated.

The analysis starts from the possibility of using integrated micro-transformers capable of operating in a switching frequency range f_s = [*10*, *50*] *MHz* and providing a customizable turn ratio which can help in design optimization. These are introduced in section 3.3. The preliminary requirements shown in Table 3.1 have been considered in the analysis that follows.

Table 3.1 High power density stackable flyback preliminary requirements.

Parameter	Requirement
V_{in}	[*15*, 48] *V*
V_{out}	*1 V*
I_{out}	*1 A*
k	[*3, 5*]
f_s	[*10, 50*] *MHz*

These requirements aim at the development of a high step-down converter possibly working with input voltages up to *48 V* used in telecommunication and industrial applications. An output power around *1 W* is considered to ensure an increment in terms of miniaturization with respect to the existing high step-down solutions. This power level should allow limited concerns on packaging constraints regarding power dissipation. The number of stacked cells k is used as another degree of freedom.

With respect to power switches, the choice of such a transferred power level allows the use of small-sized switches. A rough approximation on switch sizing can be done considering their voltage and current rating requirements. With respect to voltage ratings, it is easy to notice that each cell behaves as a flyback converter. Regarding primary side switches, the input voltage sharing reduces their required voltage rating. Worst case is with $k = 3$ and $V_{in} = 48\ V$ which causes $V_{in\ k} = 16\ V$ per each cell. If we assume that the turn ratio between primary and secondary is not too high (e.g. from 1:1 to 5:1) the secondary voltage reflection is multiplied by the turn ratio with a worst case of $V_{sec\ ref} = 5\ V_{out} = 5\ V$ and leaving some margin V_{marg} to cover also for additional ringing caused by leakage inductances provides that a switch with a $V_{DSmax} \geq V_{secref} + V_{in} + V_{marg} \approx 25\ V$ can be used.

In terms of primary side's currents, we can consider that each cell transfers *1/k* of the total power. Thus:

$$I_{in\ k} = \frac{P_{in}}{k \cdot V_{in\ k}} = \frac{P_{out}}{\eta \cdot k \cdot V_{in\ k}}. \tag{3.1}$$

Applying 3.1 to the case considered before, with an efficiency per cell of $\eta = 0.7$, we obtain $I_{in\ k} \approx 29.8\ mA$. This value is very low with respect to available current ratings for 25 V rated commercial discrete power switches which are usually oriented to manage higher power levels. Consequently, commercial power switches have higher parasitic capacitance that directly contrasts with the possibility of working at high switching frequencies with reasonable speed and switching losses. Conversely, the requirements obtained do not present specific drawbacks when considering an integrated realization allowing to design a switch with very small area occupation and reduced parasitic capacitance with respect to transistors rated for higher currents.

Regarding secondary side switches we can define:

$$I_{out\ k} = \frac{P_{out}}{k \cdot V_{out}}. \tag{3.2}$$

At secondary side, due to the high step-down, the switch required is much bigger. In fact, we can still use a rating of $V_{DSmax} = 25\ V$ (i.e. a case where the turn ratio is 1:1 plus ringing) but $I_{out\ k} = 334\ mA$. In this case the benefit of integration is still noticeable, but it could be even greater if a higher turn ratio is used. In fact, this could reduce the breakdown voltage required for the device which generally improves its high switching frequency performance by allowing to use devices with a better $R_{on} \cdot Q_g$ figure of merit.

3.3 Integrated micro-transformer

As switching frequency increases, required inductance value decreases to a range of hundreds down to tens of nanohenries. As already introduced in section 1.3, these values can be achieved with an higher inductance density when a magnetic core is used. Nowadays, different materials and techniques are researched for micro-fabrication of transformers' cores. With respect to materials, soft ferrites compounds are the principal choice for power inductors and transformers. These provide high magnetizing inductance and a good coupling factor between the primary and secondary windings. The choice of the material is not only related to its magnetic properties but also to the availability of relatively low-cost techniques for core fabrication. The most diffused are based on sputtering, electroplating and screen printing aiming at the direct realization of magnetic core on a silicon oxide substrate. The final target of these techniques is to realize the core directly on the active silicon as it would be required for a PwrSoC.

An integrated micro -transformer design presented by Würth Elektronik in [11] has been considered a possible candidate solution for the feasibility study that we are conducting. The magnetic core is a CoFe thin-film alloy electroplated on a silicon oxide substrate. The device x-ray scan is shown in Fig. 3.2.

The transformer has a footprint of $2.5 \times 2\ mm$. The core is racetrack shaped and six identical coils are wound around it. The coils allow different possible values of transformer ratios, depending on which bonding scheme is adopted (i.e. 1:1, 1:2, 1:3, 2:1, 2:2, 2:3, 3:1, 3:2 and 3:3). The measured inductance values, tested at *1 MHz* plus DC bias, are reported in Tab. 3.2. The parasitic inductance with two-terminal measurement is *2 nH*. With respect to the saturation current, paper's authors have assumed $I_{sat} \approx 650\ mA$ obtained considering a variation with respect to the initial inductance value L_0 of $\Delta L/L_0 = 30\ \%$. The transformer shows a stable inductance value up to *40 MHz*.

Table 3.2 Measured parameters of micro-transformer presented in [11].

Parameter	Test condition	Calculated	Measured
Inductance (1 coil)	*5 mA / 1 MHz*	*3 nH*	*12 nH*
Inductance (2 coils)	*5 mA / 1 MHz*	*12 nH*	*22 nH*
Inductance (3 coils)	*5 mA / 1 MHz*	*29 nH*	*33 nH*
Max. inductance (6 coils)	*5 mA / 1 MHz*	*108 nH*	*116 nH*
Q (1 coil)	*5 mA / 1 MHz*	-	*3 at 20 MHz*
Q_{max} (1 coil)	-	-	*3 at 40 MHz*
R_{DC} (1 coil)	-	-	*350 mΩ*
Parasitic inductance	two-terminal meas.	-	*2 nH*
I_{sat}	$\Delta L/L_0 = 30\ \%$	-	*650 mA*

However, quality factor is still pretty low to achieve efficient power conversion and no details are reported with respect to core losses which could degrade even more the transformer performance when working with large AC current ripples. To the best of our knowledge, with respect to cores realized through electroplating, no studies have been published regarding a controlled magnetic anisotropy during core deposition. Thus, it is possible to assume that the hysteresis loop shown in the paper describes the core's behaviour without any induced magnetic anisotropy. As already introduced in section 1.3, this particular feature provides a linearization of inductance, improving current-handling capability. With respect to eddy current losses, a procedure to laminate the core could help in countering them. No mention of lamination is reported.

3.4 Overview on HF flyback design

The initial evaluation for the design of a miniaturized stackable flyback can be done considering the design of single cell managing *1/k* of the total required power. This is equivalent to the design of a HF flyback converter. The strategy adopted is to design a preliminary demonstrator, implemented with discrete components, which can be used as a test-bench for different micro-transformers before moving to a co-packaged integrated realization. For this reason a preliminary literature investigation has been conducted to evaluate discrete design of HF flyback.

The first study of a HF flyback design was proposed in 1989 [52], whose schematic is shown in Fig. 3.3. This solution provides $V_{in} = [40, 60]\ V$, $V_{out} = 5\ V$, $I_{out} = [1, 4]\ A$. In order to minimize the switching losses associated to the primary power mosfet, the design is focused on zero voltage switching (ZVS) "quasi-resonant" converter (QRC) operation. As a drawback of this technique, required voltage rating of the switch is increased with respect to hard switching. The gate driver is implemented with two NAND gates from a 74AC00 IC. In order to obtain a variable frequency, while maintaining the constant off-time of the switch required for ZVS, the remaining gates are used to implement a VCO controlled with a voltage applied at R_2 terminal. The switching frequency range in which ZVS is achieved is $f_s = [3, 13]\ MHz$. The transformer was manually wound on a pot core presenting: turn ratio 6:1, primary side inductance $L_{pri} = 5.8\ \mu H$, leakage inductance $L_{leak} = 2.5\ \mu H$. The ZVS is achieved with parasitic components only, thus L_{leak} resonates with the parallel of primary side's winding capacitance and output capacitance of the MOSFET $C_R = 40\ pF$ (not shown in figure). Q_1 is a IRF720 400 V MOSFET and D_{SCH} are two IR31DQ06 diodes. The average efficiency of the converter is around $\eta \approx 70\%$.

An increment in switching frequency has been achieved in the last decade with an RF-based design for switch and driver [53], as shown in Fig. 3.4. This solution works as step-up from a $V_{in} = 5\ V$ providing $V_{out} = [5, 10]\ V$, $I_{out} = 100\ mA$ at a switching frequency of $f_s = 63\ MHz$. The transformer is wound on a NiZn Fair-Rite 2861002402 multi-aperture core [54] made of 61 material ($\mu_i = 125$), with a nominal 1:2 turn ratio. It seems quite oversized considering the high switching frequency, in fact inductance values are $L_{pri} = 2.9\ \mu H$ and $L_{sec} = 10\ \mu H$ respectively. However,

with a volume of $7 \times 6.2 \times 4.2\ mm$ it is still a good achievement for that days. The choice of multiaperture magnetic core shape is related to the fact that with respect to an equivalent toroidal core with the same primary winding capacitance it presents a lower single-turn winding length, resulting in a wider bandwidth of the transformer. The converter is hard switched by Q_3 which is a SHF-0589, a 9V GaAs HFET. A dedicated driver is used to provide the required drive voltage for the switch to turn-on, with a negative bias to ensure a proper turn-off with short duty cycles. Secondary side diode is a HSSM-2700 Schottky with a *100 ps* carrier lifetime. Average efficiency is $\eta \approx 50 \div 70\ \%$ depending on load.

The solution shown in Fig. 3.5 has been presented in 2011 [55]. The principal innovation with respect to previous works is the use of a cascode configuration for the switch. This way, an high voltage MOSFET device (i.e. Q_2) is used to provide the required blocking while a lower voltage GaN FET (i.e. Q_1) is used to reduce the switching time and losses. The current absorbed and sinked by the capacitor C_2 during turn-on and turn-off of Q_2 tends ideally to a zero balance over a switching period. Thus, the drive power required is only the one related to the GaN FET which presents smaller gate charge Q_g with respect to the MOSFET. This can provide an efficiency improvement at light load with respect to a single switch flyback. The parameters of the implemented version are $V_{in} = [60, 120]\ V$, $V_{out} = 12\ V$, $I_{out} = 1.2\ A$. The switching frequency range is $f_s = [2.6, 3.7]\ MHz$ where ZVS is achieved. The transformer is an air-core PCB multilayer transformer with parameters: $L_{pri} = 29.38\ \mu H$, $L_{leak\ p} = 548\ nH$, $R_{pri} = 2.71\ \Omega$, $L_{sec} = 1.9\ \mu H$, $L_{leak\ s} = 38\ nH$, $R_{sec} = 80\ m\Omega$. Outer diameters of this type of transformers are in the range of $30 \div 40\ mm$ as reported in [56]. The switches used are a STP3NK60ZFP 600 V MOSFET for Q_2 while a EPC1013 150V GaN FET is used for Q_1. Reported efficiency is $\eta \approx 78 \div 81\ \%$ depending on V_{in}. It is interesting to notice that efficiency is *4 %* higher with respect to non-cascoded version of the same converter.

Another interesting design has been presented in 2014 for a *5 MHz* flyback with custom transformer [57]. Fig. 3.6a shows the schematic proposed, Fig. 3.6b the PCB implementation. The converter's parameters are $V_{in} = [36, 72]\ V$, $V_{out} = 12\ V$, $I_{out} = 2.5\ A$. As already said, switching frequency is $f_s = 5\ MHz$ with ZVS. The transformer has been designed with windings obtained with PCB layers' traces in order to maximize power density. It has a transformer ratio of 4:1 with $L_{pri} = 997.1\ nH$, $L_{sec} = 67.9\ nH$, $L_{leak} = 29.9\ nH$. An optimization study has been done in order to choose the layer arrangement for minimization of winding capacitance between primary an secondary side showing the scheme “PSPS” (i.e. Primary - Secondary - Primary - Secondary) as the best trade-off between winding losses due to primary-secondary capacitance and each side self-capacitance. Primary and secondary switches are GaN FETs, for instance Q_{SW} is an EPC2010 200V and Q_{SR} is EPC2001 100V. The board comprises also the LM5114 gate drivers. A negative V_{GS} voltage level of $-2\ V$ is required to ensure turn-off of the switches due to parasitic gate inductance. The achieved power density is $81\ W/in^3$, which is *14 %* better than the commercial flyback converter with the same specification at *300-500 kHz* range. Peak efficiency is $\eta \approx 87\ \%$.

After this literature review we can say that semiconductor technology has enabled an improvement with respect to power switches moving from power MOS-

FETs to GaN FETs solutions. The different designs presented are targeting different power levels in ranges up to few tens of Watts. As a drawback, the use of advanced semiconductor technologies adds a significant cost and reduces the possibilities in terms of active devices miniaturization.

Moreover, it is possible to notice how the reduced development in magnetics technology have slowed down size reduction of the transformers. Another problem which is more evident with these discrete implementations is related to the parasitic inductance and capacitances which impact power losses and proper switches drive capability. This limits minimum turn-on time of switches and consequently maximum frequency.

3.5 Micro-transformer preliminary simulation

Considering the transformer's parameters we can define an ideal test-bench in order to evaluate transformer's capability of transferring the amount of power required on a single cell. Complexity can be incrementally added (i.e. real switches models, parasitics, etc...) as the manageable power levels are defined. The test-bench will also serve as a comparison to better understand the causes behind power losses. The schematic of the test-bench shown in Fig. 3.7 has been set up using LTspice.

The flyback transformer is modeled using micro-transformer's parameters arranged as three series-connected coils on both primary and secondary side. This configuration gives $L_1 = L_2 = 33\ nH$, leakage inductance $L_3 = 2\ nH$ and parasitic resistance $R_1 = R_2 = 1.05\ \Omega$. Switches are ideal and modeled with the SPICE directive shown in Fig. 3.7 with $R_{on} = 100\ m\Omega$, $R_{off} = 1\ M\Omega$ and a threshold $V_t = 1\ V$. On secondary side, diode D1 models the body diode of synchronous rectifier. Input and output capacitor are kept ideal. The control signals are defined as shown. As required by the requirements of Tab. 3.1 with $V_{in} = 16\ V$ and $k = 3$, with this set of parameters is possible to achieve $V_{out} = 1\ V$ and $I_{out} = 0.35\ A$. However, as reported in Tab. 3.3, transformer's losses are very large and impact dramatically on efficiency. These losses are only related to transformer's DCR. They totally exclude the core losses which will definitely make this balance even worse.

Table 3.3 Power losses breakdown of ideal switches test-bench.

Parameter	Value	Power losses %
P_{in}	*631 mW*	-
P_{leak}	*31.4 mW*	*11.87*
P_{S1}	*5.8 mW*	*2.19*
P_{S2}	*18.3 mW*	6.92
P_{D1}	*3.6 mW*	1.36
P_{transf}	*205.4 mW*	77.66
P_{out}	*366.5 mW*	-
η	*58 %*	-

Moreover, in order to obtain the required output power with the available values of magnetizing inductance, boundary conduction mode (BCM) has been used. This operating mode enables to transfer the most of the power over one switching cycle, in fact it completely discharges the flyback transformer. As a side-effect, current ripple is very large causing large core losses. In the simulated case, if we compare with the measured values of Tab. 3.2, we are using the core in deep saturation. This can be noticed from Fig. 3.8 where the simulated transformer's currents are shown and considering that from Tab. 3.2, $I_{sat} \approx 650\ mA$ while here $I_{peak} \approx 830\ mA$.

Even with such a preliminary analysis, we can conclude that the available transformer is undersized with respect to the initial requirements. For this reason we have decided to focus the study on the development of an optimization script which can define and visualize the trade-offs existing between the minimum inductance values, maximum transferred power, switching frequency and additional constraints related to physical implementation in order to assist the design of a miniaturized custom transformer for the LVSF. This procedure is described in section 3.6.

3.6 Transformer optimization script

As previously introduced, transformer's performances are a principal limit for the design of a HF flyback converter. In order to understand which is the optimal trade-off between available inductance and managed power there are some variables and parameters which can be used to define the electrical properties of the transformer, the switching frequency of the converter and the switches' breakdown voltages and RMS currents.

3.6.1 Model degrees of freedom, constraints and outputs definition

For this analysis we will make three simplifying assumptions. The first one is that we will assume $L_{leak} = 0$. The second is removing the synchronous rectifier. This second modification will also simplify the realization of a discrete prototype focused on evaluating transformer's performances. Leakage inductance and synchronous rectifier can be added later to the model, without losing the validity of the analysis done, just adding few modifications to the equations. The third assumption is a negligible winding resistance for the transformer which also helps to simplify the initial comparison. The simplified circuit which has been assumed for the optimization is shown in Fig. 3.9. As our target is to define the electrical properties of the flyback transformer, L_{pri} and the turn ratio $n = N_1/N_2$ will be two degrees of freedom in our analysis. L_{sec} can be calculated as:

$$L_{sec} = \frac{L_{pri}}{n^2}. \tag{3.3}$$

The values of input V_i and output V_o voltages will be defined as fixed constraints.

The first important observation is related to the flyback mode of operation. We can recall that there are three possible operating modes, continuous conduction

mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM) [2]. In CCM mode the flyback transformer stores an amount of energy higher with respect to the energy transferred per each cycle. This requires large inductance values but ensures reduced magnetic ripple inside the transformer and consequently reduced peak current stress on switches and capacitors. Conversely, BCM and DCM modes provide a complete discharge of the flyback transformer over a switching cycle, allowing to transfer the same energy with a smaller inductance value when compared to CCM. However, this causes increased magnetic ripple inside the transformer and higher current stresses on the rest of the components. Due to the fact that we are working towards a miniaturization of the converter, it is reasonable to stick with BCM and DCM modes, in order to minimize the required inductance value. It is easy to notice how, for a defined inductance value, the BCM mode transfers an higher power than DCM. For this reason we can set an optimization aiming at BCM mode which, for a certain transformer configuration and switching frequency, will give maximum energy transfer over one switching cycle. BCM operation can be defined as one of the constraints of our optimization. Fig. 3.10 shows the parameters which will influence BCM mode. Parameters refer to the circuit of Fig. 3.9.

The energy E stored inside the transformer is:

$$E = \frac{1}{2} L_{pri} I_p^2 \tag{3.4}$$

where L_{pri} is the primary side inductance and I_p is the peak value of primary side current i_{pri}. The maximum allowed value for I_p directly depends on magnetic core's properties, its geometry and the number of primary side windings N_{pri}. From Ampere's law we can obtain:

$$H_{max} = \frac{N_{pri} I_p}{l_e} \tag{3.5}$$

where H_{max} is the maximum magnetic field allowable in order to avoid saturation of the magnetic core, l_e is the effective magnetic path length inside the core. In this analysis we will assume that I_p is our constraint, obtained by defining a proper number of windings N_{pri} for the magnetic core used. For BCM, the value of I_p defines ripple amplitude, too.

When the main switch Q 1 is turned on, in order to reach I p with primary side current, we have that:

$$I_p = \frac{V_i}{L_{pri}} t_{on} \tag{3.6}$$

where V_i is the input voltage and t_{on} is the on time of Q_1. With respect to t_{on} we can define a constraint on the minimum on time which depends on the turn-on time of Q_1. This will avoid unfeasibly small values for t_{on}. With respect to secondary side we have that t_{off} should be long enough to allow a complete discharge of the flyback transformer at secondary side.

Considering that secondary current i_{sec} peaks at nI_p we have that:

$$t_{off} = \frac{L_{pri} I_p}{n(V_o + V_f)} \tag{3.7}$$

where V_o is the output voltage and V_f is the diode's forward conduction drop.

As soon as i_{sec} reaches zero, we can switch on Q_1 again, thus the BCM switching frequency f_s will be defined as:

$$f_s = \frac{1}{t_{on} + t_{off}}. \tag{3.8}$$

An additional constraint on f_s is related to its maximum value, $f_{s\ MAX}$. This maximum value could be related to the performance of transformer's magnetic material, losses or other limits depending on implementation.

Assuming zero losses inside the transformer, the transformer output power P_{out} is obtained from the complete transfer of the stored energy E and can be defined as:

$$P_{out} = E \cdot f_s = \frac{1}{2} L_{pri} I_p^2 f_s. \tag{3.9}$$

Converter's output power could be obtained subtracting the losses on secondary side which in this case are related to the diode only.

The main switch duty cycle D in BCM and DCM operation can be obtained combining equations 3.6 and 3.9 and considering $t_{on} = DT_s$. This gives:

$$D = \sqrt{\frac{2P_{out} L_{pri} f_s}{V_i^2}}. \tag{3.10}$$

With the duty cycle it is possible to calculate the RMS values for primary and secondary currents. From RMS definition we have:

$$i_{pri}\big|_{RMS} = \lim_{T\to\infty} \sqrt{\frac{1}{T}\int_0^T i_{pri}(t)dt} = I_p \sqrt{\frac{D}{3}}. \tag{3.11}$$

The same works for secondary current:

$$i_{sec}\big|_{RMS} = nI_p \sqrt{\frac{1-D}{3}}. \tag{3.12}$$

These values can be used to estimate the tolerable value of transformer's DCR at both sides and evaluate the power ratings of switch and diode.

Summarizing the degrees of freedom, we have:

- Primary side inductance defined within a range $L_{pri} = [L_{pri\ MIN}, L_{pri\ MAX}]$;
- Transformer turn ratio range $n = [nMIN, nMAX]$;

With constraints:

- Input voltage V_i;
- Output voltage V_o;
- BCM operating mode;
- Fixed maximum current peak value I_p;
- Minimum on time of the main switch t_{on};
- Diode average forward drop V_f;
- Maximum switching frequency $f_{s\,MAX}$.

As outputs we obtain:

- Transformer's output power P_{out};
- Switching frequency for BCM mode f_s;
- Primary and secondary side RMS currents . $i_{pri}|_{RMS}$ and $i_{sec}|_{RMS}$;
- Duty cycle of main switch D.

The model is implemented using a MATLAB script which provides as output five three-dimensional plots (i. e. one per each of the outputs) with n and L_{pri} as x and y axes respectively. The script can be found in Appendix C. To obtain an easier read-out of the results, couples (n, L_{pri}) which generates switching frequencies or on times outside of the defined constraints are removed from the output plots. Thus, it is possible to appreciate easier the limits set by the chosen conditions.

To demonstrate its operation, we can use as input settings the constraints required by the transformer previously presented aiming at the design of a flyback cell to be used in an LVSF which works from 48 to 1 V. As input and output we set $V_i = 16\ V$ and $V_o = 1\ V$. We have $I_p = 650\ mA$ and $f_{s\,MAX} = 50\ MHz$ directly from transformer performances (see Tab. 3.2). With respect to minimum on time, we assume that $t_{on} = 3.5\ ns$ is a feasible value. Diode forward drop is $V_f = 0.79\ V$. The degrees of freedom are $L_{pri} = [10, 200]\ nH$ and $n = [0.1, 3]$.

The result is shown in Fig. 3.11. It is possible to notice that with the inductance values achievable with the presented micro-transformer (i.e. a maximum of *33 nH*) the BCM mode is obtained for frequencies much higher than *50 MHz* and with an on time much smaller than *3.5 ns*. For this reason the surfaces are cutted at the minimum possible values allowing a BCM mode with the constraints set. As an example, minimum $L_{pri} = 88.29\ nH$ with $n = 1$ which guarantees that $t_{on} \geq 3.5\ ns$ is highlighted. This case has $f_s = 28.05\ MHz$ and $P_{out} = 523\ mW$. The required duty cycle to obtain this condition is $D = 10.06\ \%$.

3.6.2 Testing of the model

In order to verify the correctness of the results estimated from the model, a LTspice simulation can be used. The circuit is shown in Fig. 3.12. With respect to the circuit of Fig. 3.7, the synchronous rectifier has been removed and a voltage controlled current source is replacing the load resistor. As we do not have a way to regulate the output voltage, this could vary from the nominal value depending on the transformer's performances. If the voltage moves from the nominal value, the assumptions done for the simplified model are not valid anymore. Therefore, G_1 be-

haves as a constant voltage load which can sink any current, allowing the converter to work with constant output voltage. The output current will depend on the power managed by the flyback inductor. This configuration allows a fair comparison among different possible settings of the transformer.

Fig. 3.13 shows the simulated waveforms of interest. It is possible to notice how the BCM mode is correctly obtained, with $I_p \approx 622\ mA$, $t_{on} \approx 20.84 - 17.4 = 3.44\ ns$. The output values are $V_o \approx 1\ V$ and $I_o \approx 281\ mA$.

Tab. 3.4 compares the values estimated by the script and the values obtained with simulation. Simulation values of I_p and t_{on} are obtained from Fig. 3.13. The simulation value of P_{out} is obtained with the plot tools of LTspice. This is the average power of L_2 (see Fig. 3.12) on an integer number of steady-state switching periods. The simulation values of RMS currents are also obtained with LTspice tools on an integer number of steady-state switching periods. The error is evaluated as:

$$\Delta x = \frac{x_{script} - x_{simulation}}{x_{script}} \cdot 100. \tag{3.13}$$

It is possible to notice a good accordance between the script results and simulation results with errors under *5 %*. This error is tolerable for such a preliminary analysis.

Table 3.4 Comparison between script estimated values and simulation results.

Parameter	Script value	Simulation value	Error (%)
I_p	*650 mA*	*622 mA*	*4.3*
t_{on}	*3.5 ns*	*3.44 ns*	*1.7*
P_{out}	*523.2 mW*	*501.46 mW*	*4.2*
$i_{pri}\|_{RMS}$	*119 mA*	*114.84 mA*	*3.5*
$i_{sec}\|_{RMS}$	*355.9 mA*	*345.3 mA*	*3*

3.7 Considerations on discrete components prototype design

As the previous analysis has shown, with the small inductance values achievable with the available micro-transformer it is not possible to obtain the required output power. Previous example showed that a minimum primary side inductance of around $L_{pri} \approx 90\ nH$ is required. Moreover, the micro-transformer is not characterized in terms of core power losses. This makes its use in the design of an integrated converter still unfeasible. Following these considerations, the script can be used to estimate the optimal values needed to transfer the required power and consequently design a custom micro-transformer with such parameters. In order to prove the validity of such a design flow this analysis could start with the design of a discrete implementation solution. This could allow to better characterize additional design constraints related also to the choice of power switches, gate drivers and control techniques, while still improving the power density with respect to the LVSF presented

in [31]. The flyback transformer can be initially chosen among commercially available transformers and, subsequently, the validated discrete setup could allow an easier testing of actual and future micro-transformers before starting the evaluation of an integrated realization. For these reasons, the estimation of parameters oriented to a discrete components prototype design of a single flyback cell will be presented. The obtained parameters will be used in subsection 3.7.2 to evaluate possible solutions for the power switches at primary side.

3.7.1 Estimation of parameters

Aiming at a discrete implementation, we can see from the works presented in section 3.4, that the maximum switching frequency should be reduced from the initial target of $f_{s\,MAX} = 50\ MHz$. In fact, such a high frequency value directly compromises efficiency due to switching losses, parasitic inductances, capacitances and core losses. Even if ZVS techniques are used to minimize switching losses related to $V_{DS} \cdot I_D$ contributions, gate losses related to Q_g are still present and can only be minimized using a switch with small gate capacitance. Moreover, the problems related to parasitics are impairing the drive capability at high frequency where a fast rise and fall time of the gate signal is required. This last phenomena is mostly noticeable in [53, 57] where the gate of the main switches are provided a negative voltage on turn-off to ensure that they remain turned off on ground bounces due to parasitic inductance. For this reason, we will reduce maximum frequency to $f_{s\,MAX} = 20\ MHz$.

In order to relax the requirements on minimum L_{pri} for a fixed minimum t_{on}, it is possible to reduce the step-down associated to the single cell. If we invert equation 3.6, it is easy to notice how V_i and L_{pri} are directly proportional when the t_{on} and I_p are fixed. For this reason we will evaluate two cases for the input voltage, $V_{i1} = 5\ V$ and $V_{i2} = 16\ V$. This can help also in reducing the breakdown voltage required on main switch. In discrete implementation the $5\ V$ input can also be directly used to supply the main switch gate driver, without any additional regulation. The reduction of input voltage will require a longer on time to charge the same amount of energy inside the flyback inductor. This will cause an extension of duty cycle ensuring an easier regulation at higher frequencies.

With respect to the rest of constraints we will still maintain the same values as for the analysis done in section 3.6. The estimation results are shown in Fig. 3.14.

As it is possible to notice from Fig. 3.14, $V_i = 5\ V$ ensures a wider range of inductances and transformer ratios which are respecting the constraints set. This means that it is also more immune to variation of inductance values and effective turn ratios relative to physical implementation. The highlighted point, with $L_{pri} = 160\ nH$ and $n = 1.5$, has been chosen for two reasons: the available "area" around it which can still ensure a BCM operation within the constraints if variations of inductance value and turn ratio happen, the capability of transferring around $0.5\ W$ of power which could be enough to respect the initial requirements on output power per each cell once the losses are included. It is easy to appreciate how the duty cycle is much more extended with respect to the $V_i = 16\ V$ case. As a drawback, the $V_i = 5\ V$ case, presents higher RMS current at primary side. This difference (i.e. around $100\ mA$) is incident on conduction losses balance but it is negligi-

ble in terms of switches' current rating selection when considering the discrete implementation.

3.7.2 Evaluation of different solutions for main switch

The results of the analysis done in subsection 3.7.1 are used to set an LTspice test-bench for the evaluation of different solutions for the primary side switch. Fig. 3.15 shows the test-bench loaded with the proper parameters. The test-bench is identical among all of the possible different solutions for the implementation of the main switch, the only part changing is the one enclosed by the dashed rectangle. The gate driver A_1, has been placed equal for all the different solutions in order to simplify the comparison. It models the non-ideal output resistance after LM5134 gate driver [58] which is a good candidate for the discrete implementation. This IC is a single low-side gate driver with an optional pilot output. The pilot output provides the capability to drive an additional external mosfet which can be placed close to the power switch's gate in order to minimize the PCB area of the turn-off loop and consequently its parasitic inductance. As it is possible to read from its datasheet, with a power supply of $4.5\ V$, the pulling down output resistance is $R_{ON\text{-}DW} = 0.2\ \Omega$ while the pulling up value is $R_{ON\text{-}UP} = 1\ \Omega$.

The different circuital solutions for the switch are shown in Fig. 3.16. Each device shown has been modeled with its equivalent SPICE model obtained from available online databases. A very wide range of possibilities has been evaluated but, for sake of brevity, only relevant results obtained with specific devices are shown. Each of them is considered both as single switch solution and also implemented in a relevant Cascode combination. For each solution, node A_x is connected with node A of Fig. 3.15. The unlabeled node is connected to the gate driver output. Solutions with Cascode configuration also have a node C_x denoting the drain of the cascoded device. Their cascoding device is biased at a proper constant voltage.

As it is possible to notice there are four different switch types: BJT, NMOS, GaN FET, RF LDMOS, identified by different symbols and labels. These are described in Tab. 3.5. It is quite difficult to find parameters capable to compare devices belonging to different technologies. For this reason, the different devices have been chosen starting from their voltage and current ratings. In fact, we could consider a voltage rating V_{rated} obtained as:

$$V_{rated} \geq V_i + n\left(V_o + V_f\right) + 0.2 \cdot V_i \tag{3.14}$$

where the switch is rated to block a voltage higher than input voltage plus reflected secondary voltage and a $20\ \%$ margin considering ringing that will be generated by leakage inductance. In the test case, with $V_i = 5\ V$, $n = 1.5$, $V_o = 1\ V$ and assuming $V_f = 0.8\ V$ we have $V_{rated} \geq 8.7\ V$.

With respect to I_{rated} we can consider a $20\ \%$ margin on the RMS current at primary $I_{pri}|_{RMS} = 222\ mA$, thus $I_{rated} \geq 267\ mA$.

A more interesting selection can be done by considering the dynamic behavior of the switches which can be directly addressed by input and output capacitances magnitudes. With respect to Q_1, the BJT, the collector capacitance C_C can be con-

sidered as an output capacitance. This is a much smaller value with respect to other devices. As a drawback, the BJT presents the second highest on resistance. The MOSFET Q_2 is a device with a Q_g value among the lowest commercially available in order to reduce its drive losses. It presents also the lowest on resistance while it has the higher capacitances. Q_3, the GaN FET, seems to be the best trade-off among the selected parameters. This emerging technology provides better $R_{on} \cdot Q_g$ figure of merit with respect to Si devices, as explained in section 1.2. We decided to include in our investigation also an RF LDMOS transistor, Q_4. This device, being specifically designed to work in linear region, is characterized with parameters focusing on its small-signal operation. Its input and output capacitances result to be very low, in order to allow the transistor to work as an amplifier at frequencies up to *1 GHz*. However, its $R_{ds\ on}$, which has been estimated from the V_{DS} vs I_D characteristic, results to be the highest among the selected devices. A general drawback which has been noted with respect to RF transistors is related to the unavailability of non-linear SPICE models. It is very common, among this type of devices, to find only s-parameters models. With respect to the cost of these devices, it is important to underline that both GaN FET and RF LDMOS are much more expensive than actual dominant technologies[3].

Table 3.5 Discrete devices selection for main switch evaluation.

Id.	Device	I_{rated} *(A)*	V_{rated} *(V)*	$V_{beon}\|V_{th}$ *(V)*	C_{iss} *(pF)*	$C_C\|C_{OSS}$ *(pF)*	Q_g *(nC)*	$R_{ceon}\|R_{dson}$ *(mΩ)*	*Price (€)*
Q_1	BJT NPN PBSS2515MB	*0.5*	*15*	*0.9 (max)*	-	*4.4 (typ)*	-	*300 (I_C=0.1A)*	*0.08*
Q_2	MOSFET N IRLML0030TR	*5*	*30*	*2.3 (max)*	*382 (typ)*	*84 (typ)*	*2.6 (typ)*	*33 (typ)*	*0.67*
Q_3	GaNFET EPC8004	*4.4*	*40*	*2.5 (max)*	*45 (typ)*	*17 (typ)*	*0.36 (typ)*	*125 (max)*	*4.04*
Q_4	RF LDMOS PD84002	*2*	*25*	*≈3.5 (graph)*	*16 (typ)*	*16 (typ)*	-	*1000 (graph)*	*3.26*

Going back to Fig. 3.16, solutions (1),(2), (4) and (6) are single switch solutions. Solution (1) requires an additional network in order to provide a proper current drive of the BJT base current. At turn-on the driver rises to V_{Hi} = *5 V*, C_1 is a short for the turn-on peak current pulse which should not exceed the maximum base current. Thus:

$$I_{B\ peak} = \frac{V_{Hi} - V_{BE}}{R_1}. \tag{3.15}$$

[3] Prices of December 2014 as obtained from various distributors from www.octopart.com.

The peak current decreases and settles to a constant value when C_1 is charged. This happens with a time constant $\tau_{chrg} = R_2C_1$. The settling current is needed to sustain BJT conduction. Its value is obtained as:

$$I_B = \frac{V_{Hi} - V_{BE}}{R_1 + R_2}. \tag{3.16}$$

At turn-off the driver output falls to ground. C_1 discharges with time constant $\tau_{dchrg} = R_1R_2C_1/(R_1 + R_2)$. For Q_1 from datasheet we can obtain $I_{B\ peak} = 100\ mA$, $I_B = 50\ mA$. These values give: $R_1 = R_2 = 39\ \Omega$. For the time constant, we assume $\tau_{chrg} = t_{on\ min}/5 = 700\ ps$, which gives $C_1 = 18\ pF$.

Solutions (3) and (5) implement the BJT as Cascode. The idea is to provide the BJT turn-on and turn-off by driving a device which requires a smaller drive in order to spare on gate drive losses. The topological configuration provides also a much faster turn-on and turn-off of the BJT. The collector current at turn-off flows out from base as a negative current providing a much greater turn-off current, in fact, $i_{B\ off} = i_C = \beta I_B$. This way the charge stored in the base is removed much faster achieving reduced turn-off times.

On-state losses are increased by the series of two devices but they are minimized considering that the Cascode provides a voltage protection for the lower transistor and its maximum off-state voltage is limited by the voltage biasing the base of the BJT. For this reason, a low voltage MOSFET (which has low losses) can be used. The MOSFET will also switch with a reduced V_{DS} providing lower switching losses.

In solution (7) the same principle is applied to the RF LDMOS. In this case the main target of this configuration is minimization of the parasitic capacitance seen by node A_7 by using the low output capacitance of the RF device.

Figures from 3.17 to 3.23 show the simulated waveforms comparison for the different main switch solutions of Fig. 3.16 against ideal switch. Voltage of switching nodes A_x, C_x and currents i_{pri}, i_{sec} are reported.

Solution (1) shows how the selected driver and R-C network cannot switch off the BJT at such high switching rates. In fact, in order to provide the turn-off, the driver should provide the sinking of a higher base current in order to remove the charge stored in the base. This would require much additional drive power and is not considered as a solution because it would cause incremented losses. An additional benefit could be obtained by providing a sinking towards a negative voltage instead that to ground on turn-off. However, this solution causes an additional complexity of the drive system.

Solution (2) shows how the MOSFET switch properly turns on and off. The drive and switch dynamic performances cause the switching node's transitions to be less steeper. As consequence, there are hard switching losses. Turn-on time seems to be slightly faster than turn-off, causing the primary side current to store more energy on the inductor with respect to ideal case. This causes a slight CCM mode of operation.

In solution (3) we consider the use of BJT as a Cascode for the MOSFET. The first interesting observation is that in this configuration the BJT can be turned on and off providing only the drive power required for the MOSFET. As previously said, the turn-off collector current is forced through the base causing a fast removal of the

stored charge. This charge can be stored in a capacitor connected between BJT's base and ground and recovered at turn-on. For this reason the BJT has greatly reduced drive losses. The bias node is at *2 V* ensuring a proper turn-on of the BJT and a limiting of the MOSFET's drain voltage C_3. This limitation ensures that MOSFET's turn-on losses are reduced. However, even if this solution allows to switch on and off the BJT at such high rates, it is possible to notice how the turn-off is much longer than turn-on causing not only a reduced power transfer at secondary but also increased $V_A \cdot i_{pri}$ switching losses.

Solution (4), the GaN FET, is actually the best candidate. Due to the low Q_g and C_{iss}, C_{oss} capacitances it turn-on and turn-off times are minimal and the switch can "copy" ideal behaviour.

Due to the very good dynamic performances of the GaN FET, we have decided to simulate it in combination with the BJT in solution (5). It is pretty clear how the GaNFET, being faster than the MOSFET, allows to additionally reduce the BJT turn-off time which still remains as the main limitation.

Solution (6) shows the behaviour of the RF LDMOS. As expected it has very good dynamic behavior, ensuring a fast turn-on and turn-off. However, its on resistance is pretty high causing a sensible tilting of the switching voltage when turned on. This causes increased conduction losses and reduced power transfer at secondary side which causes the converter to operate in a slightly DCM mode. The ringing on currents is addressable to parasitics included in the SPICE model of the switch.

Solution (7) proposes the use of the LDMOS as a Cascode for the GaN FET. This configuration exploits the excellent dynamic performances of both of the devices which allows to ensure a true voltage limiting of C_7. In fact, as it can be seen in previous cascoded configurations, the slow turn-off of BJT caused the C_x node voltage to rise almost to the value assumed by node A_x. The only drawback related to this configuration is the high on resistance of the RF device which is summed to the GaN FET's one. The ringing on currents seems to be pushed to an higher frequency and damped by the slightly increased resistance. This suggests that the parasitics capacitances seen by the inductor are also reduced by cascoding.

As final considerations we can say that with such a reduced input voltage (i.e. $V_i = 5\ V$) solutions involving single switches are preferable with GaN FETs as best candidates. If cost is an issue, MOSFET can be used and if the switching losses caused by the device are not tolerable a study on ZVS could be done to reduce them. As a drawback the ZVS will definitely increase the required voltage ratings for each component and a Cascode solution could be evaluated. If cost is not an issue, RF devices show very good dynamic performances but their on resistance is usually much higher than devices designed for switching applications. Moreover, their cost is often quite high and doesn't justify their use in place of devices like GaN with similar cost and extremely better power handling capabilities. Cascode solutions can become useful in situations where the input voltage is higher than in the considered case. If the required primary side power is fixed, from switches' point of view, the solution of using an higher input voltage with reduced current becomes attractive. In fact, the cascoding device should be rated for an higher voltage while the cascoded one could be a low voltage device with reduced parasitics and resistance. Due to the

reduced RMS current (see the comparison of Fig. 3.14 between $V_i = 5\ V$ and $V_i = 16\ V$), the series of the on resistances can be tolerated.

3.8 Conclusion

This chapter has presented a preliminary study focusing on the design of a LVSF converter with increased power density. The switching frequency of the converter can be moved from the *500 kHz* of the actual solution in the range $10 \div 50\ MHz$. The main part of the LVSF converter is the flyback cell, and the design of a high frequency cell is very similar to the design of a high frequency flyback. The frequency increment allows a reduction on the required inductance values and this could allow the use of currently under development integrated micro-transformers. For this purpose an available integrated micro-transformer has been evaluated and a preliminary simulation including a transformer characterized with its parameters has been done. Due to its low inductance values, significant DCR and to the absence of additional details on magnetic core losses for a large signal operation of the core, the results have shown that this technology is not yet ready to satisfy the required power ranges. Following this result, the study has been oriented to a more general approach focused on the definition of the criteria necessary to obtain additional requirements for the design of a custom micro-transformer. This can help to understand which is the best trade-off between the switching frequency, available inductance values and turn ratios in order to achieve the maximum power transfer per each cell. This study has been structured around the development of a MATLAB optimization script which can help the designer to easily visualize the different parameters. The starting point of this analysis has been the definition of a simplified flyback circuit which has been used to obtain the basic requirements. Due to the low inductance values which can be reached with integrated micro-transformers, the BCM/DCM operating mode of the single flyback cell has been selected. Following this choice, additional parameters like the peak current and minimum on time of the main switch creates additional constraints related to the characteristics of the transformer and switches which are considered for the evaluation. Inductance value and turn ratio have been left as variables within a defined range. Once all the constraints are combined with electrical equations, the output produced by the script are surfaces describing transformer's output power, BCM mode switching frequency and transformer's RMS currents in the chosen inductance and turn ratio range. These parameters are loaded in a SPICE test-bench to prove their validity and to allow a more detailed study. The script can be considered as an evaluation platform on which complexity related to parasitics or other non-ideal phenomena could be added for a more precise analysis. Focusing on the design of a single cell prototype implemented with discrete components, the script results have been used to evaluate the performances of different solutions for the realization of the main switch. For this analysis different devices, considering also unconventional solutions like RF-based transistors and BJTs, have been considered and combined in order to estimate their dynamic behaviour with the circuital parameters obtained from the script.

Future work can be divided in short and long term tasks. As a short term task, the design of a discrete prototype should be accomplished finalizing the selection of proper components. This prototype could be used to measure the performances of available micro-transformers in open loop. Initially the secondary side rectifier could be implemented with a diode relieving the effort of designing a synchronous rectifier. With some additional effort, the discrete components prototype could be designed in such a way that different cells can be stacked and tested as a open loop LVSF converter. This would require additional considerations involving the level-shifting of signals for the drivers of each different cell. This could be initially done by capacitive coupling. At this stage an higher frequency version of the minimum deviation controller could be prepared to close the feedback loop. As a long term task, following the results obtained with the HF discrete prototype, a solution involving the design of an integrated modular cell could be evaluated. In order to maintain the voltage isolation between primary and secondary side a two-dies solution is required. Basically, each cell could be a PwrSip with stackable outputs. In order to achieve this result a lot of different studies and considerations are needed. The main issues are not only related to the technology required for the development of the micro-transformer and its co-packaging with the dies, but also to the feedback and thus control techniques. In fact, in such a compact and high frequency system, the isolated feedback transmission from secondary to primary is a delicate matter. A solution which could allow to eliminate additional feedback windings on the flyback transformer or other feedback systems, could be a primary-side regulation based on secondary to primary reflected voltage.

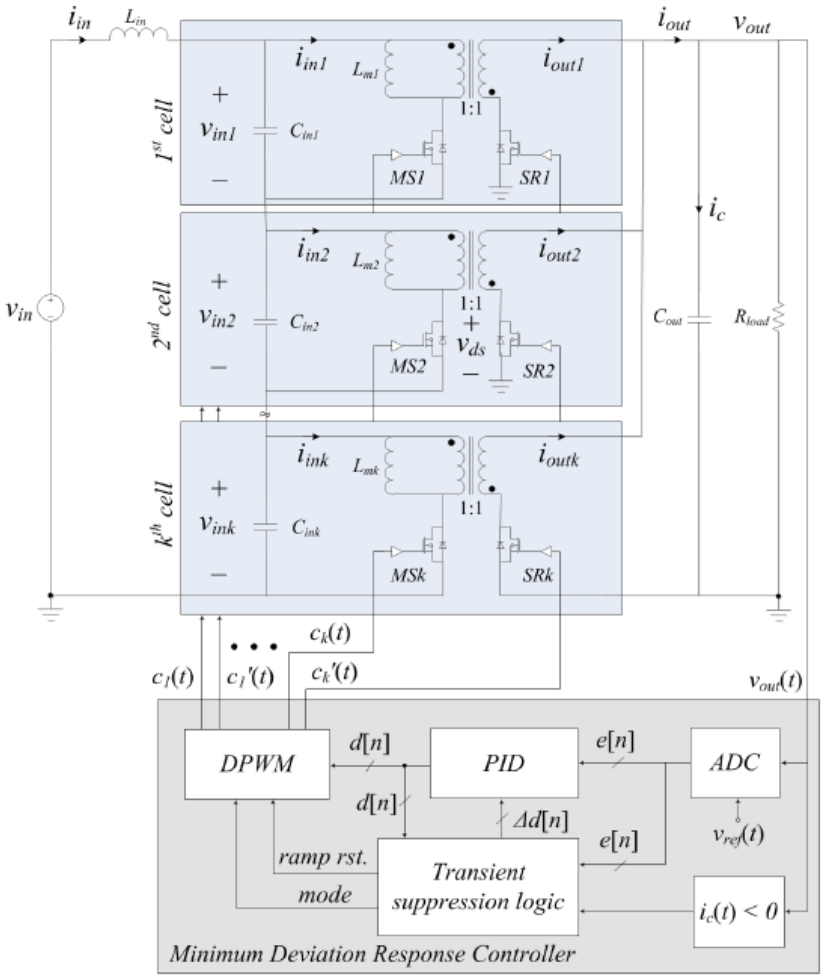


Fig. 3.1. Low volume stackable flyback converter topology.

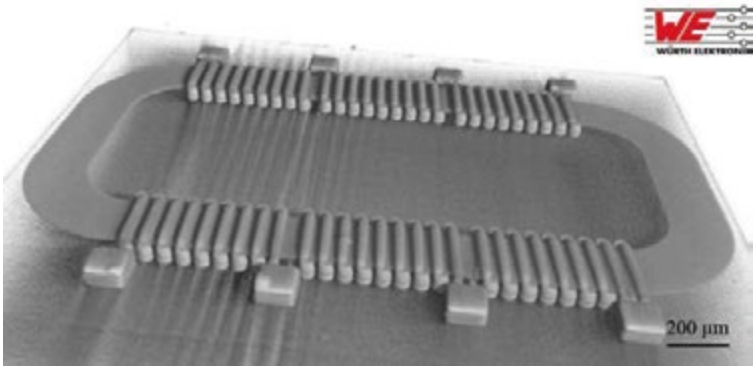


Fig. 3.2. X-ray computed tomography scan of completed micro-transformer chip [11].

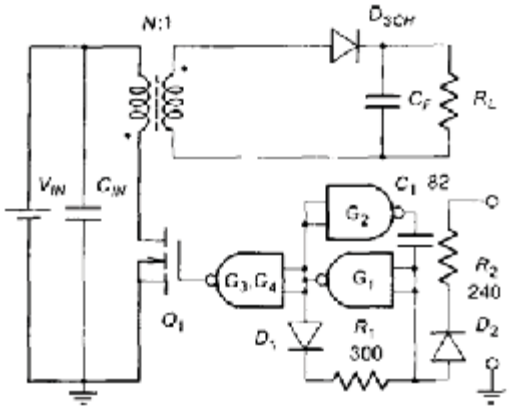


Fig. 3.3. ZVS-QRC flyback [52].

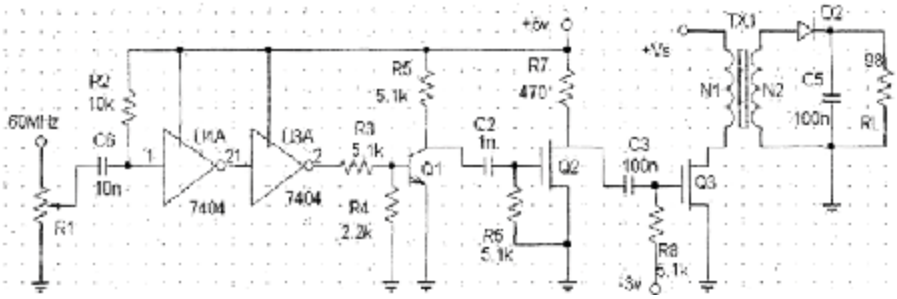


Fig. 3.4. 63 MHz flyback [53].

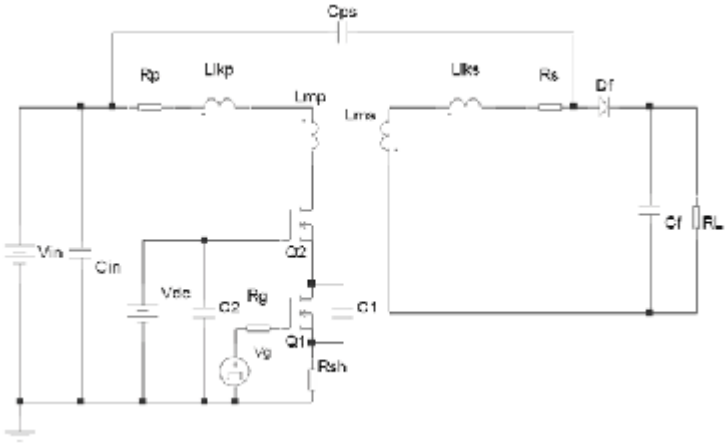
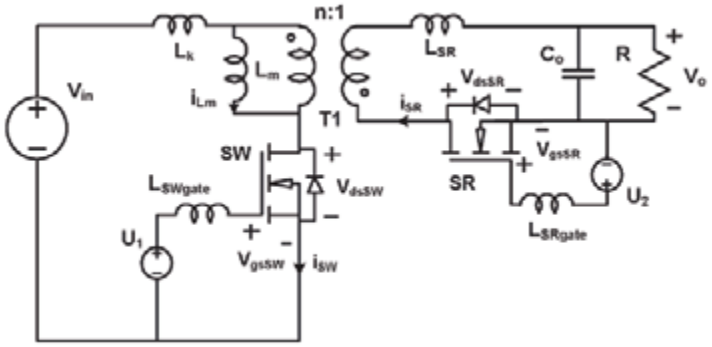
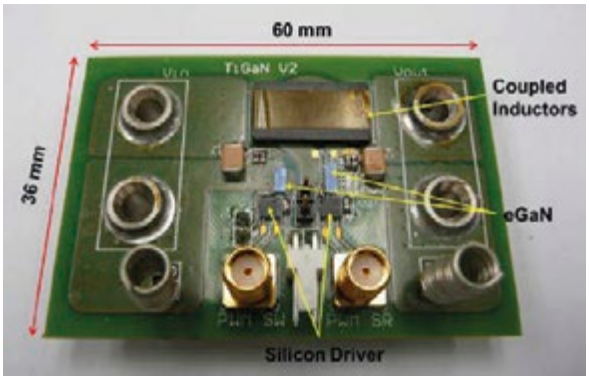


Fig. 3.5. Cascode flyback [55].



(a) Schematic.



(b) Implemented PCB.

Fig. 3.6. Flyback converter operating at 5 MHz [57].

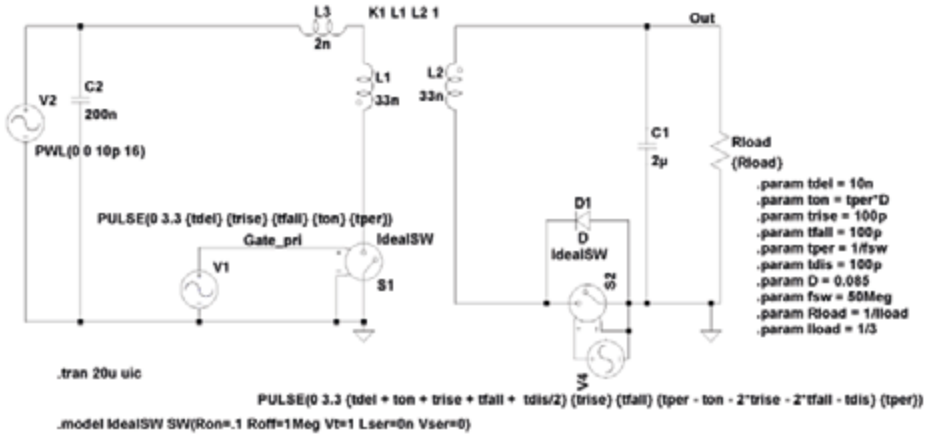


Fig. 3.7. Transformer's parameters test-bench implemented with LTspice using ideal switches model.

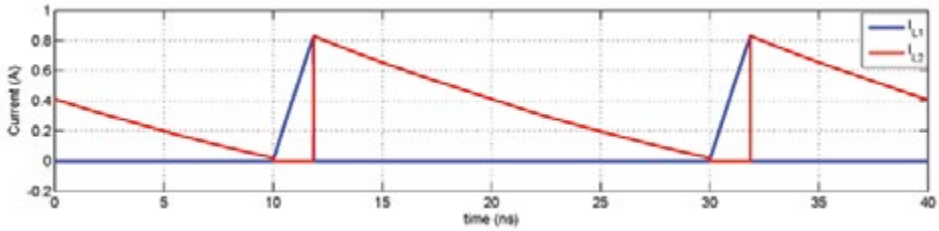


Fig. 3.8. Transformer's primary and secondary currents, referred to schematic in Fig. 3.7.

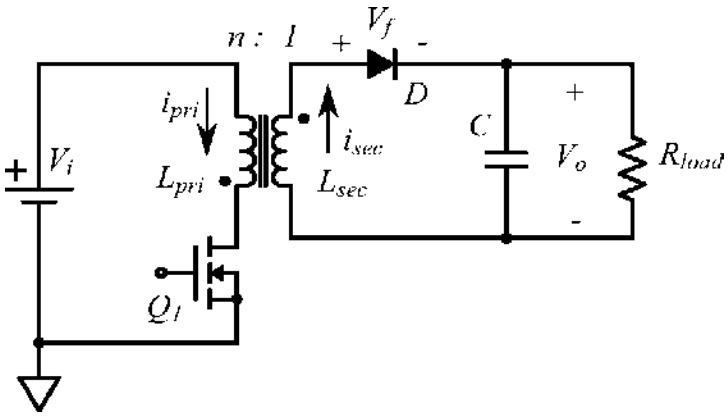


Fig. 3.9. Simplified flyback circuit used for the optimization.

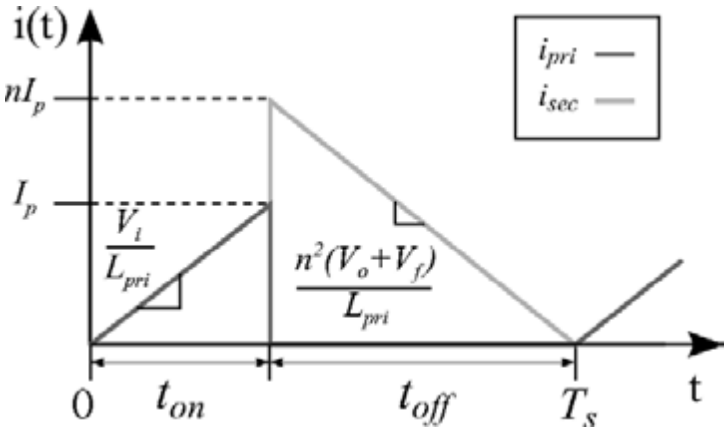


Fig. 3.10. Flyback converter's primary and secondary currents with relative parameters under BCM assumption.

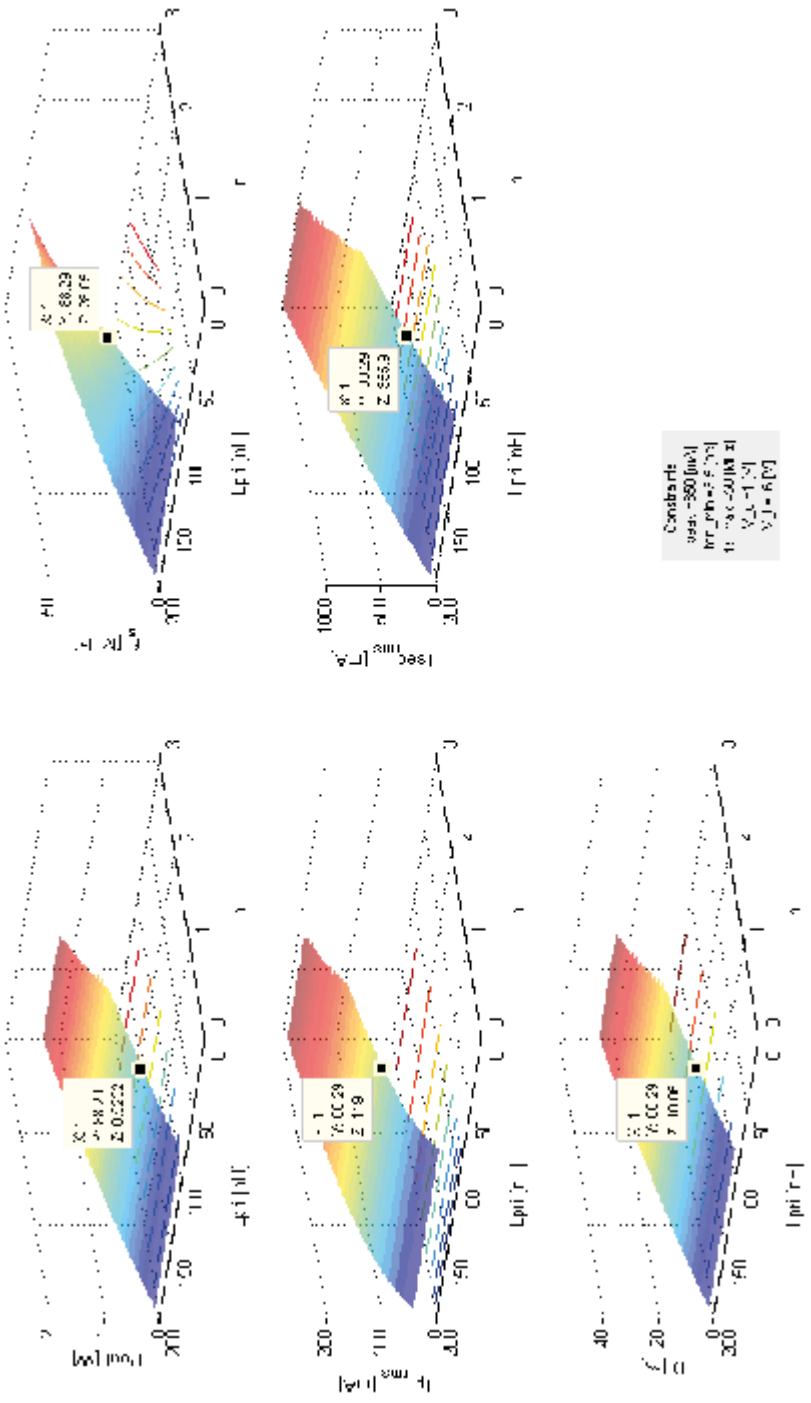


Fig. 3.11. Flyback transformer script plot results for micro-transformer constraints, $V_i = 16\ V$, $V_o = 1\ V$.

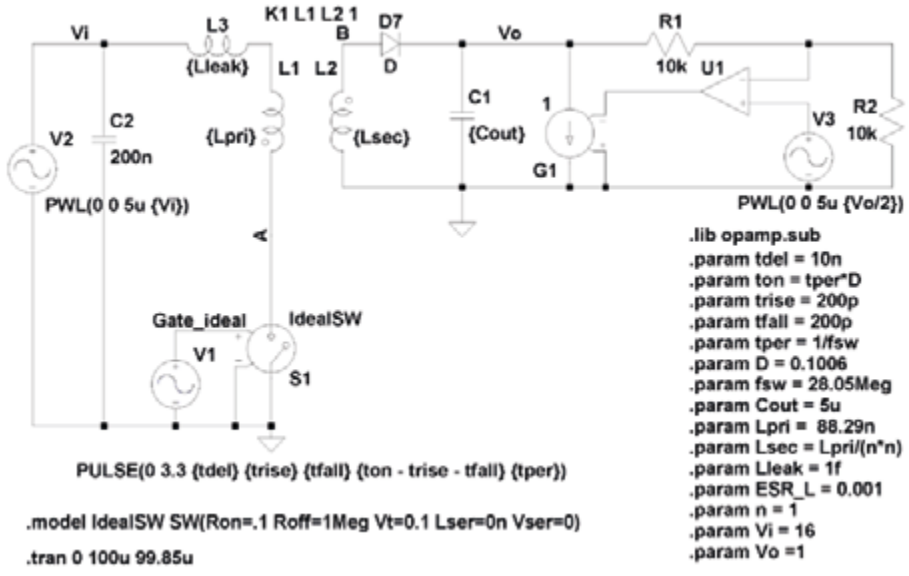


Fig. 3.12. Flyback schematic used to validate model results, loaded with the outputs of Fig. 3.11.

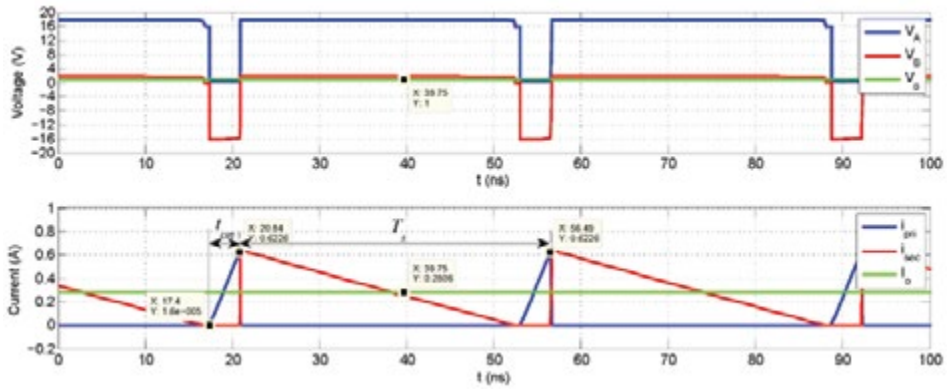


Fig. 3.13. Simulated waveforms obtained from model validation example of Fig. 3.12.

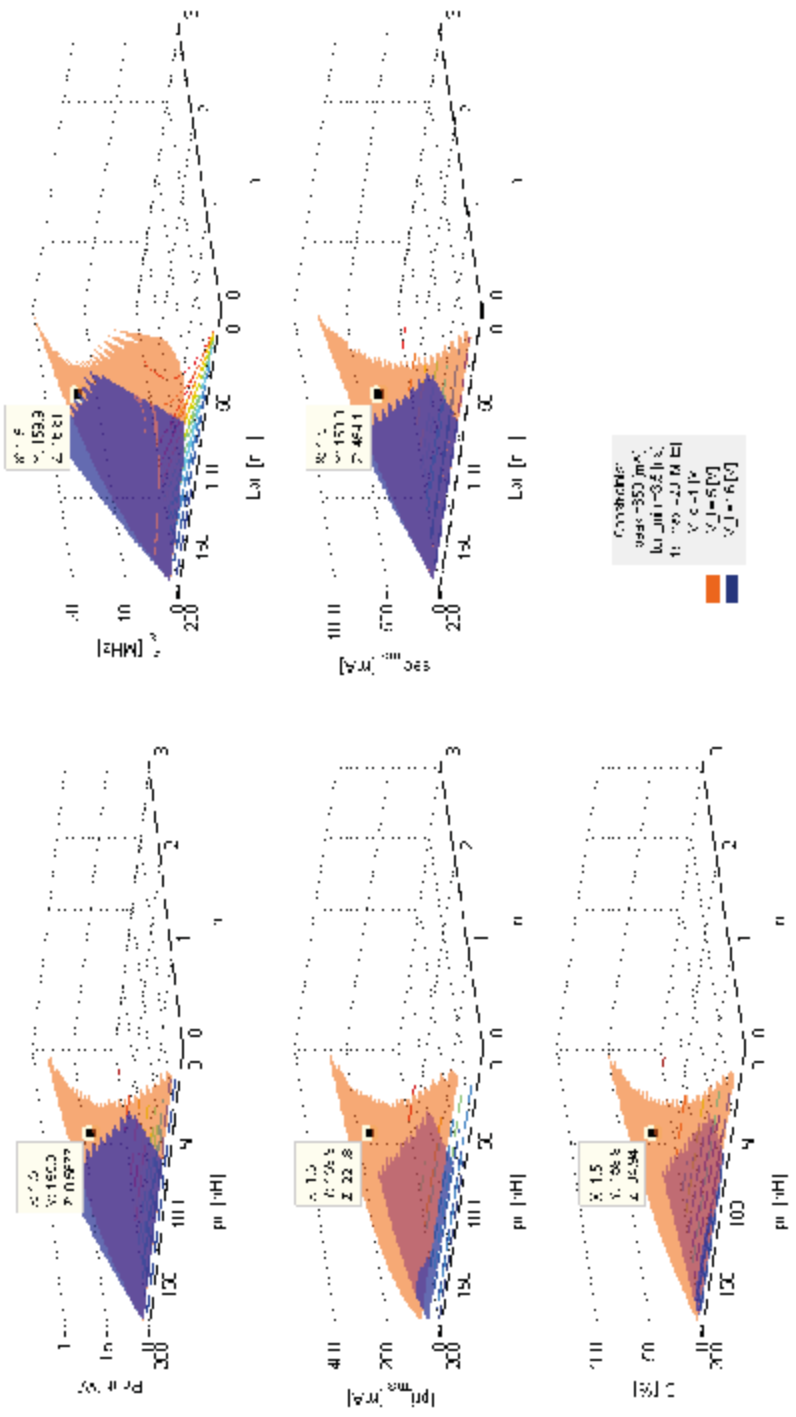


Fig. 3.14. Flyback transformer script plot results for discrete implementation constraints, $V_{i1} = 5\ V$, $V_{i2} = 16\ V$, $V_o = 1\ V$.

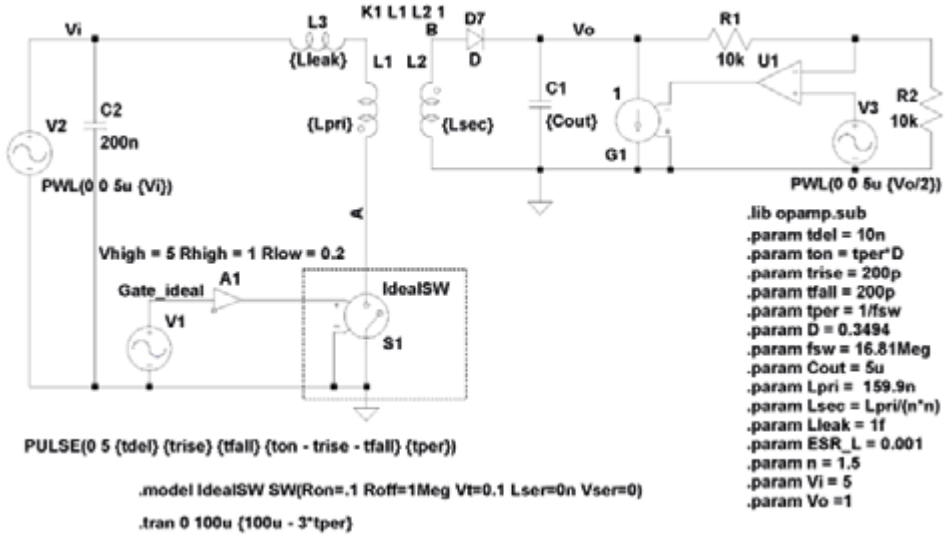


Fig. 3.15. Main switch evaluation test-bench.

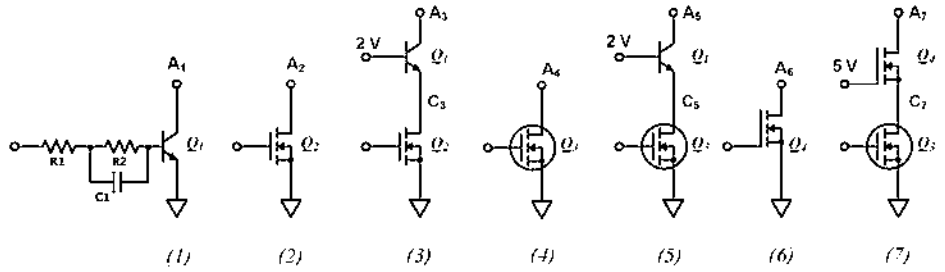


Fig. 3.16. Different solutions evaluated for the main switch in Fig. 3.15.

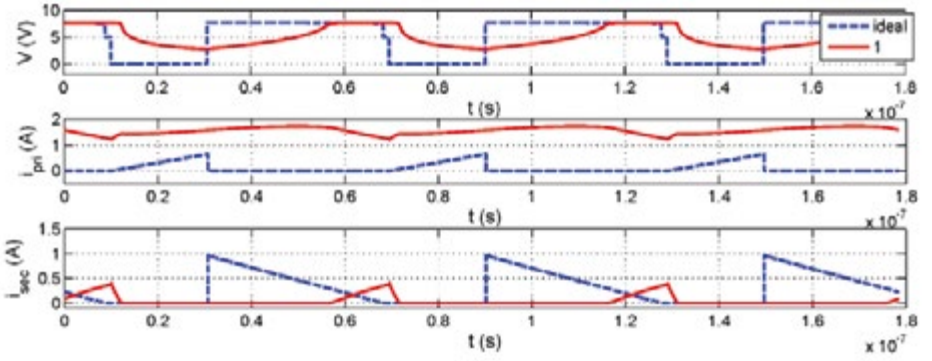


Fig. 3.17. Flyback switch comparison: case (1), BJT.

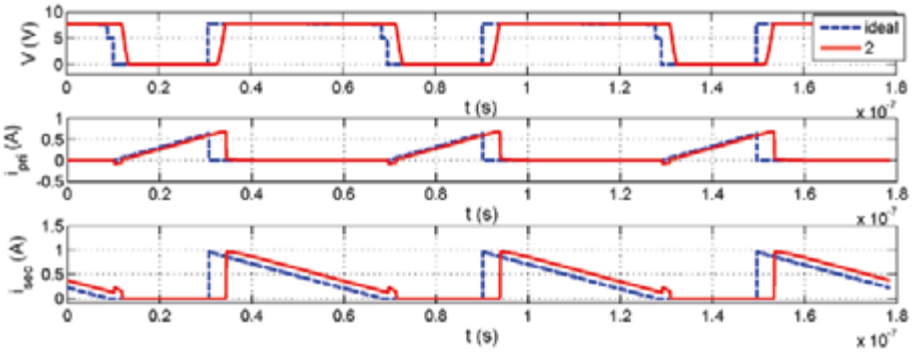


Fig. 3.18. Flyback switch comparison: case (2), MOSFET.

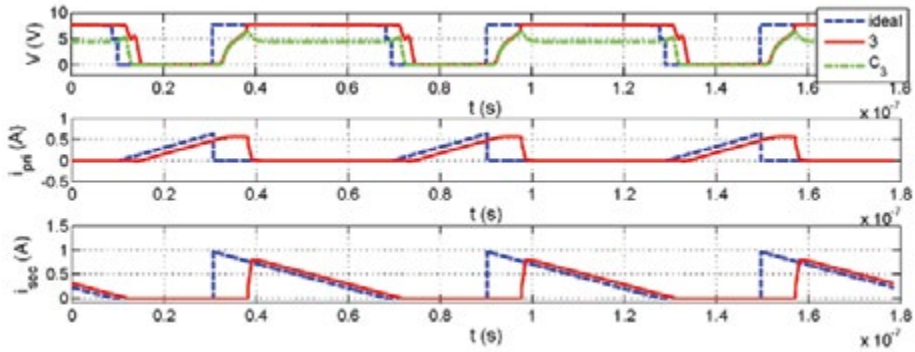


Fig. 3.19. Flyback switch comparison: case (3), MOSFET with BJT Cascode.

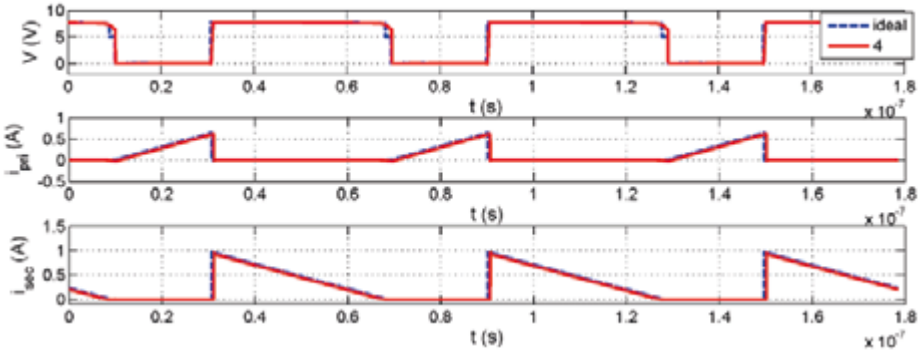


Fig. 3.20. Flyback switch comparison: case (4), GaN FET.

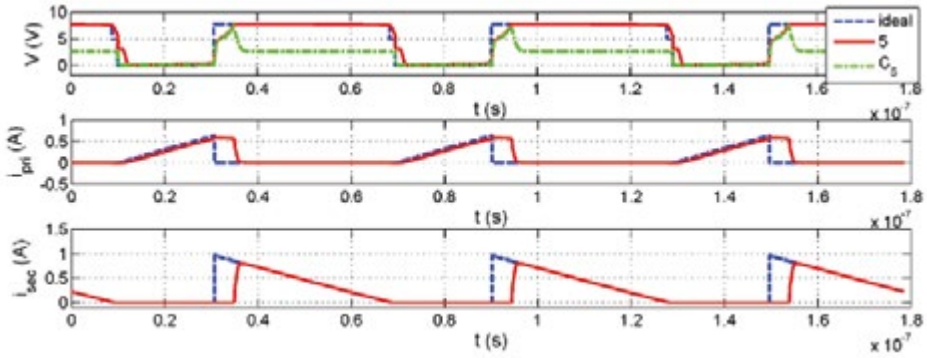


Fig. 3.21. Flyback switch comparison: case (5), GaN FET with BJT Cascode.

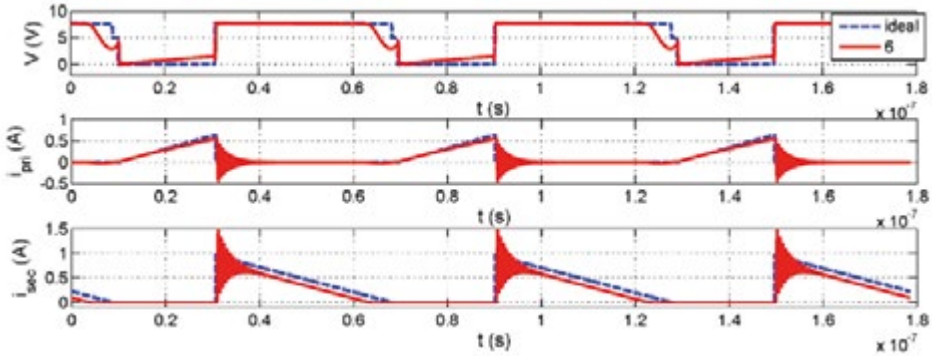


Fig. 3.22. Flyback switch comparison: case (6), RF LDMOS.

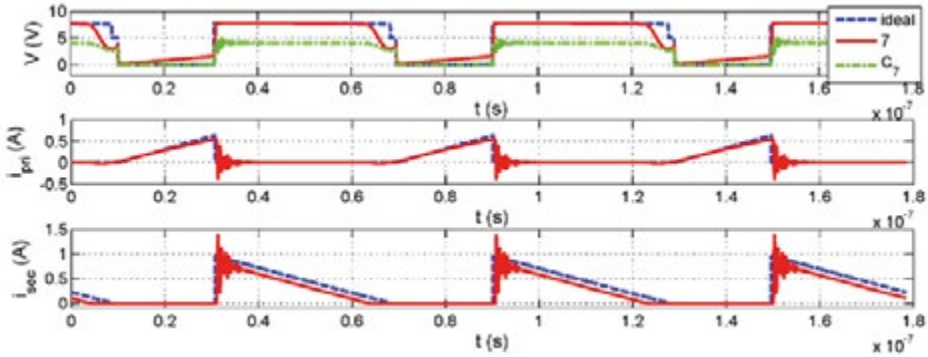


Fig. 3.23. Flyback switch comparison: case (7), GaN FET with RF LDMOS Cascode.

Chapter 4
Hysteresis core losses model

The choice of magnetic components has an important role in the design of efficient high power density DC-DC converters. The switching frequency range which is currently targeted to obtain a size reduction of passives is from *1 MHz* to *100 MHz* [1]. In this range, magnetic core inductors show an higher inductance density with respect to air core components and they can also provide advantages in terms of EMI due to the capability of providing magnetic flux confinement [6, 7, 8, 10]. The miniaturization of inductors with magnetic cores requires a research effort based on the selection of magnetic materials which can be used. These must be compatible with the integration processes and at the same time capable of providing acceptable inductance values in the frequency range of interest. Moreover, magnetic materials present loss mechanisms which introduce additional power losses to the power conversion process. The study of core losses and their modeling is of fundamental importance in order to allow a more precise selection of the magnetic material which best suits a particular operating condition required for the passive component which employs it.

This chapter starts by briefly recalling the losses contributions in a power inductor. Subsequently, the most common techniques used to estimate core losses are compared focusing on Jiles-Atherton hysteresis model. Then, the implementation of a method for modeling hysteresis loops and related losses in magnetic core inductors used for power converters applications is described. The implemented model can be loaded with parameters which are specific for the magnetic material which needs to be modeled. The method has been applied to some commercially available ferrite materials in order to verify the accordance of B-H loops and power losses density estimation against manufacturer's data with acceptable results. The main limitations of actual model are also treated in order to set the basis for future development.

4.1 Power losses contributions

Magnetic core inductors contribute to the converter power losses mainly with conductor losses and core losses.

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4.1.1 Conductor losses

Conductor losses are related to the resistivity of the windings, skin and proximity effects. They strongly depend on both the winding's and core's geometries which influence the amount of losses caused by the different terms.

With respect to resistivity the power loss can be simply estimated as:

$$P_{res} = \frac{1}{2} I_{RMS}^2 R_w = \frac{1}{2} I_{RMS}^2 \frac{\rho l}{S} \tag{4.1}$$

where the winding resistance R_w depends on the geometry of the windings (i.e. length l and cross-section S) and on the used conductor's resistivity ρ.

Equation 4.1 is valid at DC and low frequency, while as frequency increases, skin effect comes into play reducing the effective cross-section S, thus increasing R_w. In fact, as shown in Fig. 4.1, as an alternating current I flows into a wire, a variable magnetic field H is generated. This causes eddy currents I_e which tend to decrease the current density J in the inner part of the conductor from the surface value J_s.

The skin depth δ is defined as the depth where current density equals J_S/e, thus it is reduced to *37 %* of the surface value. Moreover, the *98 %* of the current density is concentrated within a depth of 4δ. Skin depth can be defined as a function of frequency f as:

$$\delta(f) = \sqrt{\frac{\rho}{\pi f \mu}} \tag{4.2}$$

where μ and ρ are the magnetic permeability and the resistivity of the conductor material. Applying equation 4.2 to R_w gives that as frequency increases, R_w increases approximately as the square root of the frequency, as shown in Fig. 4.1. As an example, table 4.1 reports the skin depth for copper (i.e. $\rho = 1.68 \times 10^{-8}\ \Omega{\cdot}m$ and $\mu \approx 4\pi \times 10^{-7}\ H/m$). It is possible to notice how, as the frequency of the current increases it is practically useless to maintain large cross-sections of the conductors if there is no DC component.

Table 4.1 Skin depths for copper

$f\,[MHz]$	$\delta\,[\mu m]$
0.1	*206*
1	*65*
10	*20.6*
100	*6.5*

When the conductor carrying an alternating current is adjacent to other conductors still carrying alternating currents, the magnetic field generates eddy currents also in the adjacent conductors changing the distribution of their current densities. The result is that the current is concentrated in areas of the perturbed conductor furthest away from conductors carrying current in the same direction. This ultimately increases the resistance of the conductors. This effect, know as proximity effect, strongly depends on geometry and is usually countered by spacing the conductors, if possible, or by avoiding them to be exactly parallel to each other.

4.1.2 Core losses

Magnetic materials are divided in magnetic domains. These are regions of the material characterized by a uniform orientation of the magnetization. Magnetic domains are generated as a form of energy minimization inside the material. In fact, if the material is composed by a single, large magnetic domain, a high magnetostatic energy is required while an amount of smaller domains with different orientations tend to minimize the magnetostatic energy required and result as a minimum energy state for the material. The division in magnetic domains happens directly on the formation on the magnetic sample, when it is cooled below the Curie temperature. The domains have a size which depends on the material and its crystal arrangement but are usually ranging in sizes from few to hundreds of micrometers, thus comprising a large number of material's molecules. The regions between different domains are called “domain walls”. Here the magnetization rotates from the direction in one domain to the direction in the adjacent one. When an external magnetic field is applied to the material, the domain walls move as the magnetic domains rotate to align the direction of magnetization with the external field. The domain walls movement and their resonance require energy due to the presence of impurities inside the materials which causes the core losses.

Core losses are mainly addressable to two terms, hysteresis losses and eddy currents losses. Hysteresis loss is related to the energy required by the movement of the magnetic domains' walls to change the orientation of the domains' magnetic moments. As shown in Fig. 4.2, the relationship between applied magnetic field H and magnetic induction B is not linear in these materials, as it is for vacuum (a), but it follows an hysteresis loop as shown in (b). If the material is initially demagnetized (i.e. $H(0) = B(0) = 0$) the initial magnetization curve is followed up to saturation. Then, as the magnetic field decreases, the upper path is followed. It is important to notice that for $H = 0$, $B = B_r$ called remanence field. Thus, the material remains magnetized. Only at the coercitive field $H = -H_c$, the induction field goes back to $B = 0$.

The loop area is proportional to the hysteresis losses. This can be easily demonstrated considering for example a toroidal core inductor with N windings, A_c core section, l_c magnetic core path length to which is applied a sinusoidal current of period T with zero DC component. The energy W dissipated in one cycle is:

$$W = \int_0^T v(t) \cdot i(t) dt. \tag{4.3}$$

If the inductor is ideal, there is a linear relationship between *v(t)* and *i(t)*. These are phase shifted by *90°* and *W = 0*. However, in a real inductor with magnetic core, we have a non-linear and hysteretic relationship. We can express *v(t)* as:

$$v(t) = NA_c \frac{dB(t)}{dt} \tag{4.4}$$

using Faraday's law. We can also express *i(t)* using Ampere's law:

$$i(t) = \frac{H(t)l_c}{N}, \tag{4.5}$$

which also shows how the magnetic field *H(t)* is linear with the current. Substituting equations 4.4 and 4.5 in equation 4.3 we obtain:

$$W = \int_0^T NA_c \frac{dB(t)}{dt} \cdot \frac{H(t)l_c}{N} dt = A_c l_c \int_{B(0)}^{B(T)} H\, dB. \tag{4.6}$$

Thus, the energy loss is not zero, but it proportional to the H-B loop area and to the core's volume. It is straightforward that the higher is the magnitude of *H*, the larger is the area and ultimately, the higher are the losses.

An interesting quantity, which allows to characterize the losses independently from material geometry, is the power losses density P_V which can be defined as:

$$P_V = \frac{fW}{A_c l_c} = f \int_{B(0)}^{B(T)} H\, dB \qquad \left[\frac{W}{m^3}\right]. \tag{4.7}$$

Materials used for power conversion should provide low losses which at the same time means it is easy to change their magnetization. The candidate materials for this application are the “soft” magnetic materials. Conversely, in applications like data storage, where the magnetization ensures the data retentivity, a material which is hard to demagnetize is preferred. These are called “hard” magnetic materials. A qualitative comparison of hard and soft magnetic materials is given in (c) of Fig. 4.2.

Considering loop area solely dependent on hysteresis is an approximation valid at quasi-static or very low frequency applied magnetic field. As the frequency increases the loop area becomes bigger, due to the losses related to eddy currents. These currents are generated by the magnetic flux *Φ* flowing through the core as shown in Fig. 4.3.

In order to reduce eddy currents' magnitude, magnetic materials are usually designed to present high resistivity in the operating frequency range. High resistivity can be obtained through core lamination, as it is done for low-frequency laminated steel cores, or by properly mixing the compound which forms the core, as it is done for sintered materials, like ferrites. These usually present eddy currents losses few orders of magnitude below the hysteresis ones in the operating frequency range, leaving the latter as the dominant contribution [2].

Eddy current loss is divided in two parts, the classical eddy current defined as above and the excess (or anomalous) loss. Excess loss is related to the difference be-

tween measured loss and the sum of hysteresis and classical eddy current loss. This loss has been related to non-uniform magnetization inside the material resulting from skin effect and non-linear diffusion of magnetic flux [59, 60].

Power losses density P_V, is usually measured by the manufacturers and reported in magnetic core materials' datasheets. Being a measured value, this includes all the losses contributions and different curves are reported as a function of maximum induction field B_{max} and signal frequency. As an example, Fig. 4.4 shows the power losses density measured for Ferroxcube 4F1 material.

These measurements are usually reported only for sinusoidal current signals with small amplitudes and far from the saturation of the material. For these operating conditions it is possible to assume, also for the measurements of Fig. 4.4 that both H and B fields are sinusoidal and consequently, characterize the losses just by indicating B_{max} and the frequency.

However, the loop area directly depends on the shape of the current signal crossing the inductor and also on its DC bias. Fig. 4.5 qualitatively shows how different current signals used in power conversion provide different loop areas. In power converters, the waveform of the current crossing the inductors usually belongs to one of these three categories: sinusoidal, triangular or triangular plus a DC bias, depending on the inductor function. This ultimately affects the power losses estimation. DC bias doesn't directly cause power loss, however, it pre-magnetizes the material to an operating point which increases the energy amount required by the AC component of the current to vary the magnetization.

Ultimately, the core losses depend on temperature. This is especially relevant for ferrites which have minimum core loss between *60 °C* and *100 °C*. Fig. 4.6 shows the power losses density for 4F1 ferrite material as a function of temperature for different values of B_{max} and frequency. As for Fig. 4.4 the manufacturer provides this data only for sinusoidal signals without DC bias. In Fig. 4.6 it is possible to notice how P_V has a parabolic behavior which also varies in a very wide range depending on both B_{max} and frequency.

In conclusion we can summarize that core losses are non linear depending on:

- H amplitude;
- H repetition frequency;
- H waveform (i.e. DC component and harmonics related to non-sinusoidal waveform);
- temperature.

These parameters are all interconnected among each other with non-linear relationships. The best way to estimate core loss is by now to replicate the exact operating conditions and evaluate them through measurement. However, this is a very uncomfortable method, and a way to model them in advance is usually more convenient to the designer. In the next section we will briefly describe the models which have been proposed to estimate the core presented losses.

4.2 Overview on magnetic materials' power losses models

The models used to estimated core losses can be divided in “small signal” and “large signal” models.

4.2.1 Small signal models

The first category refers to applied magnetic fields which are of a much smaller amplitude with respect to the saturation magnetic field H_{sat}. For this case, the hysteresis loop is very narrow, relative permeability μ_r and consequently inductance can be easily approximated to a constant value as shown in Fig. 4.7.

The models used in this operating condition are usually based on an equivalent electrical circuit modeling of the inductor's core including an inductor L and a resistor R_L to take into account the losses. The most common example of these kind of core losses models is the quality factor Q_L, which is evaluated for a sinusoidal signal of a specific pulsation ω_0 as:

$$Q_L = \frac{\omega_0 L}{R_L}. \tag{4.8}$$

However, this model is valid only for a specific frequency, and for the magnetic field value which has been used for the measurement.

A more detailed model, which keeps track of the inductive and resistive part as a function of frequency, is the complex permeability μ_c [61, 62], which is defined as:

$$\mu_c = \mu_{real} - j\mu_{imag}\,. \tag{4.9}$$

Equation 4.9 can be also used to model the inductor core loss in terms of equivalent circuital parameters. If we consider for example a toroidal inductor of impedance Z_L and use μ_c in the inductance formula we can obtain:

$$Z_L = j\omega \frac{\mu_c N^2 A_c}{l_c}, \tag{4.10}$$

which becomes:

$$Z_L = j\omega\mu_{real} \frac{N^2 A_c}{l_c} + \omega\mu_{imag} \frac{N^2 A_c}{l_c} = j\omega L + R_L. \tag{4.11}$$

Magnetic core's manufacturers provide the frequency behavior of complex permeability, as for example is shown in Fig. 4.8 for 3F4 material [87]. At low frequency, the real part is dominant and constant with frequency. As frequency increases, the losses becomes more significant, due to eddy currents and, eventually, the magnitude of the imaginary permeability becomes comparable with the magnitude of the real part. At high frequency, the real permeability starts to decrease, due to the relaxation of magnetic dipoles. This is caused by the combination of domain wall motion and magnetic moment rotation [63].

We can observe that complex permeability graphs provided in material datasheets are usually obtained with sinusoidal signals at a specific value of maximum induction field B_{max}. If the value of B_{max} changes, the complex permeability is affected in a non linear way depending on the non-linearity of the hysteresis loop. A good explanation of this can be found in [64] where a procedure to measure the complex permeability for different values of B_{max} is given. Fig. 4.9 shows how the real and imaginary parts of complex permeability change as a function of the applied B_{max} for a MN80 MnZn ferrite core measured at *100 °C*. As the B_{max} magnitude increases the real part starts to decrease at lower frequencies while the imaginary part starts to increase at lower frequencies.

This means that the datasheet's complex permeability behaviour is not reliable to estimate the core losses for a different B_{max} condition. Moreover, even if a measurement as the one shown in Fig. 4.9 is done, complex permeability can only trace the behaviour of sinusoidal signal.

4.2.2 Large signal models

In order to estimate the core losses for "large signal" behavior, two approaches are the empirical equations and the hysteresis model.

4.2.2.1 Empirical equations

With respect to the empirical equations, the basic idea is to curve-fit a set of measured values. The obtained curves will be the model used to estimate the loss. The most common approach is based on Steinmetz equation. For 3F4 this model is obtained by the experimental measurements done by the manufacturer under sinusoidal excitation without DC bias and is given in [65] for a temperature of *100 °C*:

$$P_{mag} = C_m \cdot f^x \cdot B_{max}^y \cdot\cdot (ct_0 - ct_1 T + ct_2 T^2) \quad \left[\frac{kW}{m^3}\right] \tag{4.12}$$

where f is the frequency, B_{max} is the peak flux density, T the temperature and the other coefficients are defined as in table 4.2.

Table 4.2 3F4 Steinmetz equation constants.

Frequency [k*Hz*]	C_m	x	y	ct_2	ct_1	ct_0
500 – 1000	$1.2 \cdot 10^{-4}$	*1.75*	*2.9*	$0.95 \cdot 10^{-4}$	$1.1 \cdot 10^{-2}$	*1.15*
1000 - 3000	$1.1 \cdot 10^{-11}$	*2.8*	*2.4*	$0.34 \cdot 10^{-4}$	$0.01 \cdot 10^{-2}$	*0.67*

The temperature coefficients are chosen is such a way that the term enclosed in brackets in equation 4.12 is *1* with *T = 100 °C*. In order to evaluate the coherency of the core losses values estimated from equation 4.13 against datasheet measured values, Fig. 4.10 shows a superposition of the losses obtained with the model above and

the values presented by the 3F4 datasheet. It is possible to notice how low-frequency losses are underestimated for values under *400 kHz*.

In fact, in power applications inductors are often crossed by currents that are not sinusoidal. Even if this model is defined for a sinusoidal current signal, it is possible to adapt it to other waveform shapes. This leads to the Modified Steinmetz Equation (MSE) [21] where the losses are defined as:

$$P_{mag} = \frac{1}{\tau} \cdot C_m \cdot f_{eq}^{x-1} \cdot B_{max}^{y} \cdot (ct_0 - ct_1 T + ct_2 T^2) \quad \left[\frac{kW}{m^3}\right] \tag{4.13}$$

where τ is the switching period and f eq an equivalent frequency defined as:

$$f_{eq} = \frac{2}{\pi^2} \sum_{k=2}^{K} \left(\frac{B_k - B_{k-1}}{B_{max} - B_{min}}\right)^2 \frac{1}{t_k - t_{k-1}} \tag{4.14}$$

where:

- B_{max}: maximum flux density in a switching period
- B_{min}: minimum flux density in a switching period
- B_k: flux density at t_k
- t_k: k^{th} instant in time
- K: number of time instances in a switching period

Following the MSE, other versions of the Steinmetz equation have been proposed to improve its estimation accuracy [23, 66, 67, 68]. Even if these modified versions show improved accuracy, they do not take into account the presence of a DC bias component in the current. The solution is, also in this case, a measured curve-fitting which does the following replacement in equation 4.13 [69,70]:

$$C_m \rightarrow C_m \left(1 - C_1 B_{dc} e^{-\frac{B_{dc}}{C_2}}\right) \tag{4.15}$$

This results in a C_m constant which has a dependency on the applied DC bias. B_{dc} and B_{ac} are the dc and ac portions of the flux density waveform, while C_1 and C_2 are parameters fitting the experimental measurements.

Steinmetz models can work for both "small" and "large" signal analysis. However, they rely on empirical data and are well defined only for sinusoidal currents. As we have seen, other types of current signals and the presence of DC bias require the approximations described above. These approximations are very specific depending on the operating conditions of the core and on the material type. This can lead to a not precise estimation of the losses.

4.2.2.2 Magnetic hysteresis model

Generally speaking, hysteresis models make possible to characterize the behaviour of an hysteresis cycle, which in our case refers to the B-H loop, as a function of an arbitrary magnetic field waveform which can also include DC bias. The model of hysteresis has been developed in literature following two different approaches. The

first one follows a mathematical approach and examples are the Preisach [71] and the Hodgdon [72] models. Preisach model is based on the description of the bulk hysteresis as a whole system composed by many single domain hysteresis loops with different switching fields. This model has the advantage to describe the shape of arbitrary loops with a high accuracy. However, the model is not linked to the physical phenomena generating hysteresis and, consequently, it must be recalculated on a variation of the external conditions (e.g. stress or temperature). The second approach led to models which are based on physics such as the Stoner-Wohlfahrt model [73] which is based on the concept of domain rotation or the Jiles-Atherthon model [74] based on the domain boundary displacement. The advantages are that these models can be adapted to include the effects of temperature, stress and external field frequency. Moreover, the limitations imposed by the consideration of physical constraints reduces the numbers of degrees of freedom with respect to mathematical models allowing a description of hysteresis with a reduced number of parameters.

4.2.3 Conclusion

As a conclusion, some interesting features for power inductors design are reported in table 4.3 comparing the different power losses models considered. Small signals models are capable of estimating small sinusoidal signal losses only. Empirical equations can extend the estimation to large signals and with some approximations also to DC bias and arbitrary waveforms. However, these require approximations which needs to be verified depending on the specific case. The hysteresis models based on differential equations are the most versatile solution in modeling both magnetic hysteresis and its associated losses. Following the availability of literature and model parameters for many common magnetic materials, we have focused our study on the Jiles-Atherthon model. Its mathematical background and implementation will be recalled in section 4.3.

Table 4.3 Review of small and large signal core losses models.

	Small signal models	Large signal models	
		Empirical equations	Magnetic hysteresis model
Small signal	✓	✓	✓
Large signal	×	✓	✓
Sinusoidal signal	✓	✓	✓
DC bias	×	✓/×	✓
Arbitrary waveforms	×	✓/×	✓

4.3 Jiles-Atherthon Hysteresis model

As introduced in section 4.2, Jiles-Atherton hysteresis model is based on the physics of domain wall displacement. The detailed physical theory of the model can be found in [74] while here we will briefly recall it for completeness focusing on isotropic magnetic materials.

As the external magnetic field changes, the magnetic domains' walls move, but the presence of impurities (i.e. non magnetic inclusions) or dislocations in the crystallographic structure of the material can cause the "pinning" of the domain wall as shown in Fig. 4.11. When pinning occurs, the moving domain wall sits in a local energy minimum and additional energy is required from the external magnetic field in order to "unpin" the domain wall. This additional energy directly generates the magnetic hysteresis.

4.3.1 Anhysteretic magnetic permeability

A magnetic material free from impurities and dislocations (i.e. crystallographic defects) would not be affected by pinning and its magnetization could follow an "anhysteretic" behavior. Considering the presence of an inter-domain coupling inside the magnetic material, described by a parameter α, it is possible to define an effective magnetic field H_e as:

$$H_e = H + \alpha M. \tag{4.16}$$

For an isotropic material, the anhysteretic magnetization M_{an} is determined with the Langevin function connecting the isotropic anhysteretic magnetization to the effective field [75, 76]:

$$M_{an}(H) = M_s \left[\coth\left(\frac{H_e}{a}\right) - \left(\frac{a}{H_e}\right) \right] \tag{4.17}$$

where M_s is the saturation magnetization, while a quantifies the magnetic domain walls density in the magnetic material. More precisely:

$$a = \frac{k_B T}{\mu_0 \langle m \rangle} \tag{4.18}$$

where k_B is the Boltzmann constant, T is the temperature, μ_0 is the vacuum magnetic permeability, $\langle m \rangle$ is the mean effective domain size.

For anisotropic materials modifications of equation 4.17 have been proposed in [77, 78, 79].

For materials with impurities, the anhysteretic magnetization is related to irreversible and reversible magnetic susceptibility in order to obtain the complete hysteresis model.

4.3.2 Irreversible differential susceptibility

Due to the pinning, there is an energy loss which can be expressed as an irreversible change in magnetization M_{irr}. The energy lost to pinning is [74, 76]:

$$E_{pin}(M_{irr}) = \frac{n\langle\epsilon_\pi\rangle}{2m_d}\int_0^{M_{irr}} dM_{irr} \tag{4.19}$$

where n is the density of pinning sites, $\langle\varepsilon_\pi\rangle$ is the average pinning energy of the sites for $180°$ domain walls and m_d is the magnetic moment of a typical domain. The coefficient multiplying the integral in equation 4.19 can be expressed as:

$$\mu_0 k = \frac{n\langle\epsilon_\pi\rangle}{2m_d}. \tag{4.20}$$

As a consequence, the parameter k quantifies the average energy required to break a pinning site in the magnetic material. We can rewrite:

$$E_{pin}(M_{irr}) = \mu_0 k\int_0^{M_{irr}} dM_{irr}. \tag{4.21}$$

From equation 4.21 the hysteresis equation for irreversible changes in magnetization can be derived [74, 76] as:

$$M_{irr} = M_{an} - k\delta\frac{dM_{irr}}{dH_e} \tag{4.22}$$

where H_e is the effective field and δ is a directional parameter such that:

$$\delta = \begin{cases} 1 & for\ \dfrac{dH}{dt} \geq 0 \\ -1 & for\ \dfrac{dH}{dt} < 0 \end{cases} \tag{4.23}$$

Equation 4.22 can be rearranged (providing $k \neq 0$ and $k\delta - \alpha(M_{an} - M_{irr}) \neq 0$) to describe the irreversible differential susceptibility as:

$$\frac{dM_{irr}}{dH} = \frac{M_{an} - M_{irr}}{k\delta - \alpha(M_{an} - M_{irr})}. \tag{4.24}$$

4.3.3 Reversible differential susceptibility

The reversible magnetization reduces the difference between the prevailing irreversible magnetization and the anhysteretic one for a given field strength.

$$M_{rev} = c(M_{an} - M_{irr}) \tag{4.25}$$

where *c* is a parameter which describes the reversibility of the magnetization.

The reversible differential susceptibility is simply:

$$\frac{dM_{rev}}{dH} = c\left(\frac{dM_{an}}{dH} - \frac{dM_{irr}}{dH}\right). \tag{4.26}$$

4.3.4 Total differential susceptibility

The sum of reversible and irreversible magnetizations gives the total magnetization as:

$$M = M_{irr} + M_{rev} \tag{4.27}$$

and, consequently the sum of the susceptibilities gives the total differential susceptibility as:

$$\frac{dM}{dH} = \frac{dM_{irr}}{dH} + \frac{dM_{rev}}{dH}. \tag{4.28}$$

Substituting equations 4.24 and 4.26 in equation 4.28 we obtain:

$$\frac{dM}{dH} = (1-c)\frac{(M_{an} - M_{irr})}{k\delta - \alpha(M_{an} - M_{irr})} + c\frac{dM_{an}}{dH}. \tag{4.29}$$

Equation 4.29 is an ordinary differential equation which gives as solution *M(H)*, the magnetization hysteresis quasi-static behaviour.

4.3.5 Time domain model

A convenient form of the model is by expressing it in time domain. This can be done differentiating equation 4.29 with respect to time as:

$$\frac{dM}{dt} = \left((1-c)\frac{dM_{irr}}{dH} + c\frac{dM_{an}}{dH}\right)\frac{dH}{dt}. \tag{4.30}$$

Combining equations 4.25 and 4.27 is possible to obtain:

$$M_{irr} = \frac{M - cM_{an}}{1-c}. \tag{4.31}$$

Substituting this result in equation 4.24 gives:

$$\frac{dM_{irr}}{dH} = \frac{\frac{M_{an}-M}{1-c}}{k\delta - \frac{\alpha}{1-c}(M_{an}-M)} \tag{4.32}$$

which is a function of only M and H (considering equation 4.17 for M_{an}). Equation 4.32 can be replaced in equation 4.30 giving as result:

$$\frac{dM}{dt} = \left(\frac{M_{an}-M}{k\delta - \frac{\alpha}{1-c}(M_{an}-M)} + c\frac{dM_{an}}{dH} \right) \frac{dH}{dt}. \tag{4.33}$$

This form of the ordinary differential equation of M describes its behavior as a function of both magnetic field H and time. It can be solved with a numerical solver and in our case it has been implemented with SAGE using "desolve_rk4" function which is based on 4th order Runge-Kutta algorithm [80]. This can work for an arbitrary *H(t)* input, provided that the function has not such discontinuities that the differential equation solver cannot overcome.
From this solution, B can be simply obtained considering:

$$B(t) = \mu_0\big(M(t) + H(t)\big). \tag{4.34}$$

4.3.6 Material parameters

We can recall that the solution of equation 4.33 gives the quasi-static behavior of hysteresis once five parameters, typical of the magnetic material are provided. These are:

- M_s [*A/m*] the saturation magnetization of the material. Sometimes instead of it, the saturation flux density B_s is given but M_s can be obtained reverting equation 4.34 for saturation values;
- a [*A/m*] giving the domain walls density in the magnetic material;
- k [*A/m*] which quantifies the average energy required to break a pinning site in the magnetic material;
- α which quantifies the internal coupling between the domain magnetizations;
- c describing the reversibility of the magnetization.

These parameters can be obtained from hysteresis measurements applying specific considerations to the model equations already presented [76, 81, 82]. Some widely used magnetic materials have already been measured and their parameters are available for specific temperatures of interest (most commonly *25 °C* and *100 °C*). Concerning the examples which will follow in the next section, table 4.4 reports the Jiles-Atherton parameters for Ferroxcube 3C81 and 3F4 magnetic materials [83].

Table 4.4 Jiles-Atherton model parameters for 3C81 and 3F4 magnetic materials [83].

Mat.	B_s (mT)		a (A/m)		k (A/m)		α		c	
	25 °C	100 °C	25 °C	100 °C	25 °C	100 °C	25 °C	100 °C	25 °C	100 °C
3C81	500	340	44	15	27	22	2.1×10^{-4}	6.7×10^{-5}	0.91	0.66
3F4	450	360	114	44	88	90	6.4×10^{-4}	1.9×10^{-4}	0.72	0.52

4.3.7 Frequency dependency

The model, as it has been previously defined, is only capable of describing the quasi-static behavior of hysteresis. However, as the frequency of the magnetic field increases, the hysteresis is deformed depending on material characteristics. The deformation of hysteresis is usually an enlargement associated to eddy currents losses, magnetic resonance and magnetic relaxation of the magnetic material. While eddy currents are a dominant phenomena in conducting materials, magnetic resonance and magnetic relaxation are more evident in non conducting materials.

In order to include the frequency dependency, the Jiles-Atherton model has been modified depending on whether the considered material can be approximated to the first or second category mentioned above. Materials like steel or iron are good conductors, thus they are subject to eddy currents and have been modeled as explained in [84]. On the other hand, we are aiming at the characterization of high frequency materials in order to enhance the converter's power density. For this reason, we have chosen to consider the model applicable to non conducting media as high frequency ferrites can be approximated [85].

The frequency behaviour model is based on a second order linear differential equation of motion of domain walls obtained from the Landau-Lifschitz equation [86]. This differential equation is averaged to describe the behaviour of the whole material, resulting in:

$$\frac{d^2M_f}{dt^2} + 2\lambda\frac{dM_f}{dt} + \omega_n^2 M_f = \omega_n^2 M \tag{4.35}$$

where ω_n and λ depend on the magnetic material and describes the oscillation of domain walls with frequency. M is the solution of obtained from equation 4.33, which becomes M_f on the solving of equation 4.35, being modified to include the frequency behaviour.

As previously stated, this frequency dependency model is an approximation, in fact real materials are not characterized by exact values of ω_n and λ, but these parameters are associated to a distribution of values. This is due to the fact that the

magnetic domains composing a real material are not all identical in size, thus they have slightly different dynamic behavior in response to an external magnetic field.

4.4 Model implementation and results

The proposed model for hysteresis and power losses estimation has been implemented following the scheme shown in Fig. 4.12. The model receives as inputs the magnetic field *H(t)* waveform (obtainable from inductor current once the geometry is defined) and the parameters which describe the magnetic material hysteresis. These are the five parameters associated with the quasi-static hysteresis model and the two parameters associated with frequency dependency. Using *H(t)* as stimulus, the differential equation based on the Jiles-Atherton model for quasi-static magnetic hysteresis is solved. The output is the quasi-static magnetization *M(t)*. A second processing stage applies the frequency dependent model to obtain the frequency behavior of the magnetization $M_f(t)$. At this point, the graph of the B-H hysteresis loop is extracted and power losses are evaluated integrating its area.

4.4.1 Full saturation hysteresis loop

The first estimation which has been done using the implemented model is related to the full saturation hysteresis loop obtained with a *10 kHz* sinusoidal *H(t)* signal. A measurement of this signal is often reported in materials' datasheets and can be used as comparison with the model outputs for validation purposes.

Fig. 4.13 shows the full saturation hysteresis loop for 3F4 material obtained with a *10 kHz* sinusoidal signal and Jiles-Atherton parameters at *100 °C*. It is in very good agreement with datasheet's loop [87]. Due to the fact that the simulation starts from $H = 0$ and $B = 0$ condition it is also possible to appreciate the first magnetization curve.

4.4.2 Loop plots for various current waveforms

Fig. 4.14 shows the hysteresis loops obtained with the described model using 3F4 material in three different operating conditions which simulate different inductor currents in power converter applications. These are examples of: a sinusoidal (blue), a triangular (green) and a triangular boundary conduction mode (red) at a period of *500 kHz* as shown in Fig. 4.14a. While the sinusoidal signal presents no discontinuities of its derivative, the triangular ones can dramatically increase the computational time of the differential equation solvers due to the discontinuities in their derivatives. For this reason, we have approximated these type of signals with their Fourier series considering the first fifteen harmonics. As it is possible to notice from Fig. 4.14a, these approximations are not compromising the overall waveform shape. Fig. 4.14b shows the various *B(t)* solutions obtained from the complete model. It is also interesting to notice how this modeling technique allows to evaluate signal and magnetic core response to transients associated to the different waveforms. Fig. 4.14c shows the steady-state hysteresis loop which has been drawn considering only

a steady-state period of *H* and *B* signals to allow an easier readability. The full saturation hysteresis loop of the magnetic material (black) is also plotted for comparison. Fig. 4.14d shows a zoomed version where it is easier to appreciate the difference between the loops areas for the different signals.

4.4.3 Core losses density estimation

The first validation step of the proposed model has been carried out comparing the power losses densities obtained from the model loaded with 3F4 and 3C81 material parameters at *100 °C* against datasheet graphs. The datasheet values have been measured by the manufacturer of the material under sinusoidal excitation, varying the amplitude and frequency of the magnetic field signal. In order to generate a comparable data set, the procedure followed starts with the modeling of the hysteresis loop for a sinusoidal magnetic field with a certain amplitude and frequency. The resulting *B(t)* waveform maximum, B_{max} is estimated. This will be the value used on horizontal axis of the power losses density plot. The loop area gives the losses density associated to hysteresis P_{hyst}.

For this comparison, the eddy current losses density contribution has been included with an estimation formula obtained from [64]:

$$P_{eddy} = \frac{(\pi B_{max} f d)^2 \sigma}{16} \tag{4.36}$$

where the core is ideally approximated with a cylindrical cross-section of diameter *d*, the core conductivity is σ and can be obtained from the material datasheet, and B_{max} is the maximum flux density.

The total power losses density is:

$$P_d = P_{hyst} + P_{eddy} \tag{4.37}$$

which will give the vertical axis value of the plot. The procedure is repeated for various amplitudes of the *H(t)* signal to obtain a line and for various frequencies to obtain multiple lines. The result is shown in Fig. 4.15 where Fig. 4.15a shows the overlap of the estimated power losses densities graph for 3F4 material (coloured lines with stars indicating the simulated coordinates) over datasheet graph (black bold lines) while Fig. 4.15b shows the same overlap for 3C81 material.

In both cases it is possible to notice how there is a quite good general agreement between the modeled losses and datasheet values. However, the noticeable discrepancies requires further investigation and modeling improvement.

The first is related to the frequency dependency model. In fact, the frequency dependency is modeled as a second order system with parameters obtained from [85], as explained in subsection 4.3.7. Fig. 4.16 shows the frequency behaviour of 3F4 full saturation hysteresis loop when the frequency is varied from *25 kHz* to *3 MHz*. The frequency model parameters are $\omega_n = 5 \cdot 2\pi$ *rad/s* and $\lambda = 14.28 \times 10^6$. At lower frequencies, the loop starts to enlarge due to the phase shift introduced by the frequency model. As it reaches frequencies comparable with the ω_n value, the

modeling has a non-physical behaviour which causes overshoots and over-saturation dynamics. A better modeling of the frequency behavior could be done measuring the frequency dependency of magnetization on a test sample and modeling its transfer function with an higher order system. Moreover, it could be interesting to understand how the frequency behavior changes when passing from a “small signal” condition, as the one used for the core losses in the datasheets is, to a “large signal” condition, as the one shown in Fig. 4.16 tries to model.

4.5 Conclusions

A modeling technique to estimate hysteresis power losses in magnetic materials has been implemented based on Jiles-Atherton hysteresis model which provides flexibility in terms of signal waveform, DC bias and both small and large signal modeling. The model, implemented in SAGE, has been preliminarily verified against manufacturers' datasheets full saturation hysteresis loops where it has shown a good agreement. A set of small sinusoidal signals at different amplitudes and frequencies, corresponding to the measurement conditions used in datasheets for core losses density estimation, have been evaluated, too. This comparison has also shown a good agreement with datasheet's data. Moreover, the model is capable of plotting loops associated with various current waveforms. Unfortunately, these do not have a datasheet measurement which can be used as comparison against the simulated results.

Some discrepancies within the core losses density data seems to be addressable to a poorly realistic modeling of the material's magnetization frequency behavior. Following this consideration and the lack of manufacturer's data for non-sinusoidal signal waveforms, future work involves a measurement campaign on different magnetic materials. This will help to further calibrate and validate the different model sections. Once this tool will be correctly calibrated, it will allow an accurate power losses estimation, enabling power density maximization of inductors for DC-DC power conversion, taking also into account their specific operating mode.

For these reasons, the study has consequently been focused on the design of an hysteresis measurement setup which is explained in Chapter 5.

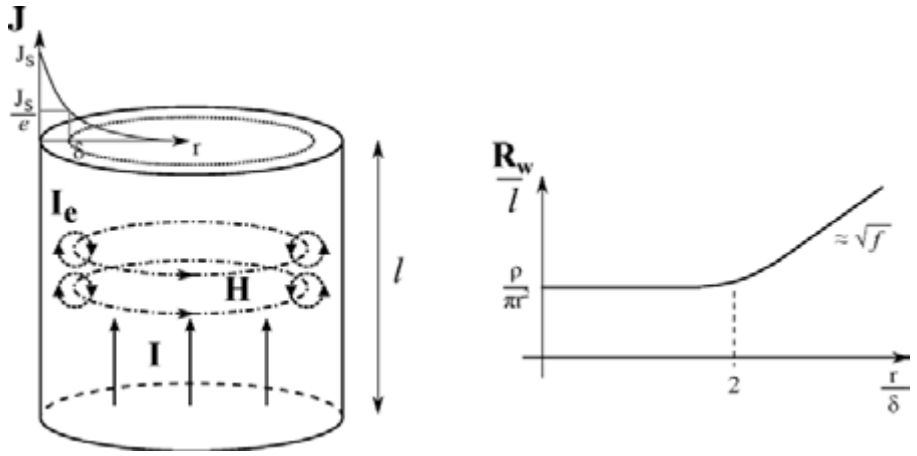

Fig. 4.1. Skin effect.

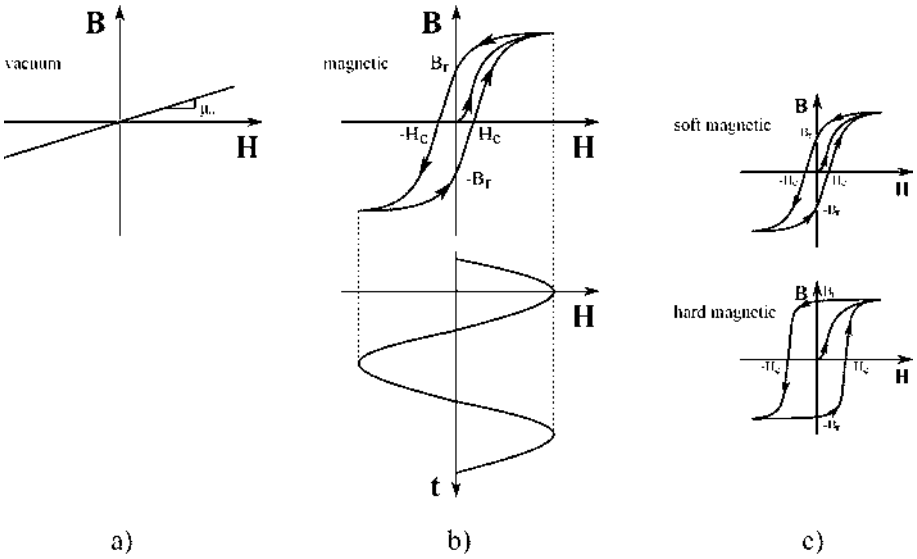

Fig. 4.2. Magnetic hysteresis loop.

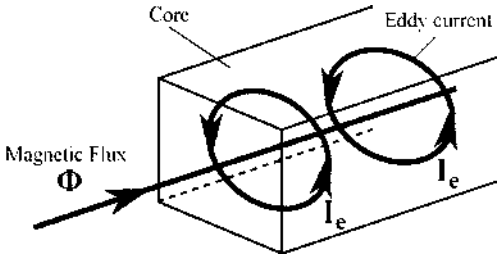

Fig. 4.3. Eddy currents generation.

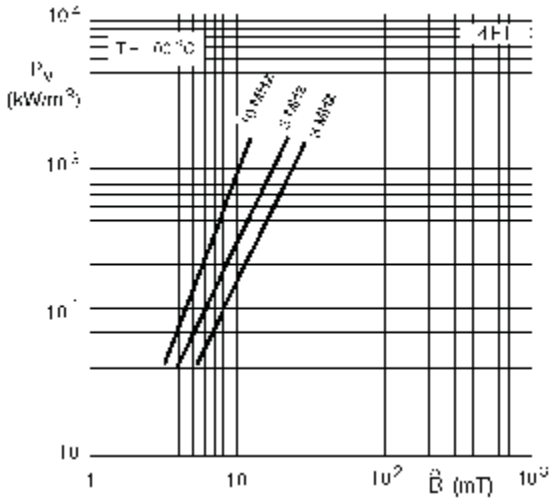

Fig. 4.4. Power losses density as a function of B_{max} and frequency for 4F1 ferrite under sinusoidal excitation.

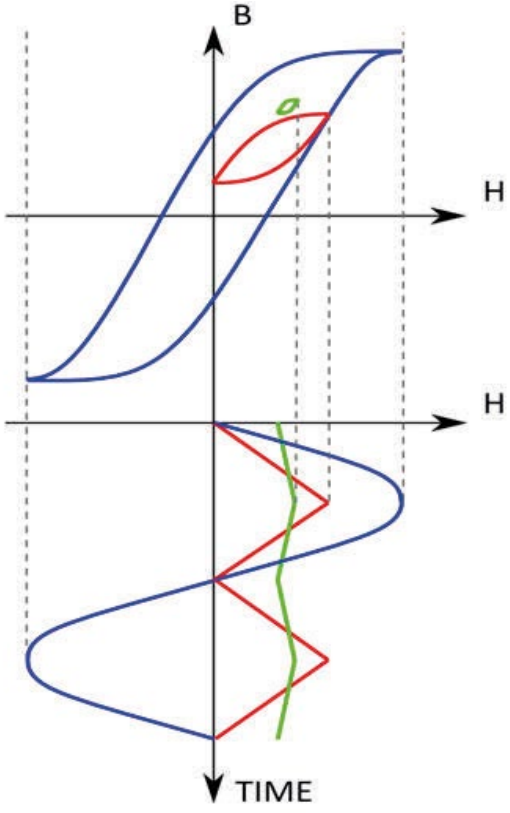

Fig. 4.5. Dependence of hysteresis loop area on current waveform properties.

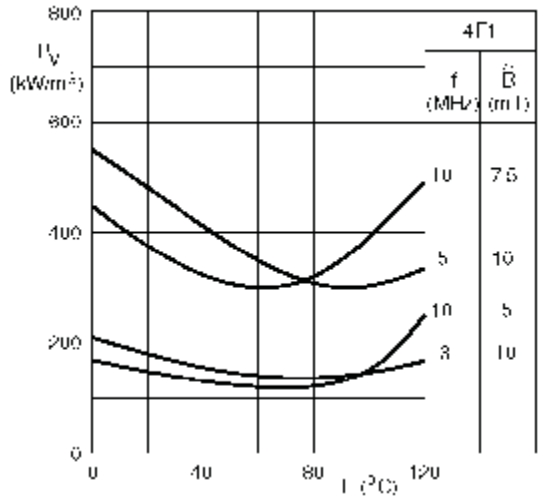

Fig. 4.6. Power losses density as a function of temperature for some specific values of B_{max} and frequency for 4F1 ferrite under sinusoidal excitation.

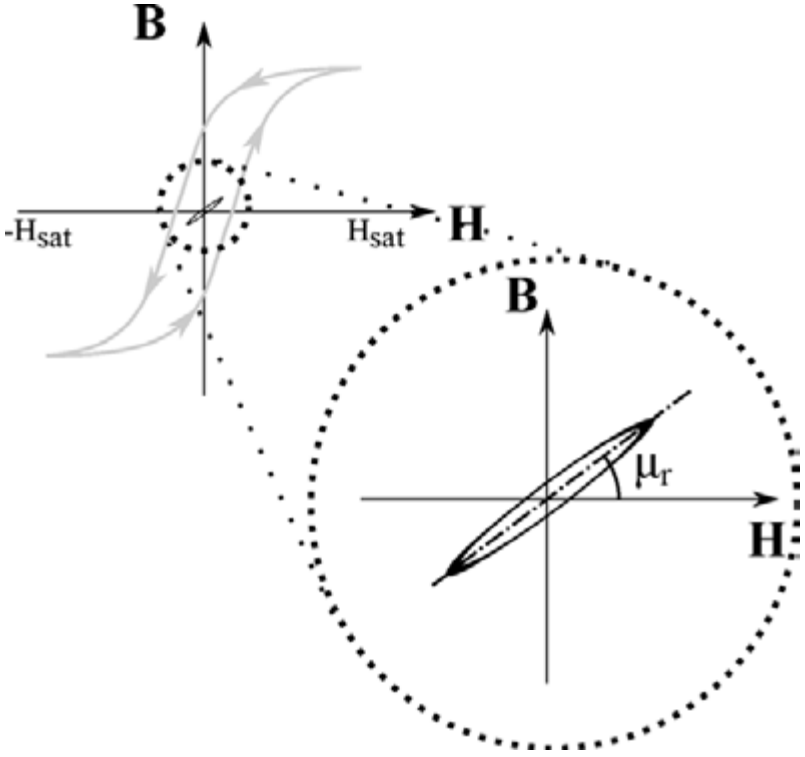

Fig. 4.7. Small signal hysteresis loop.

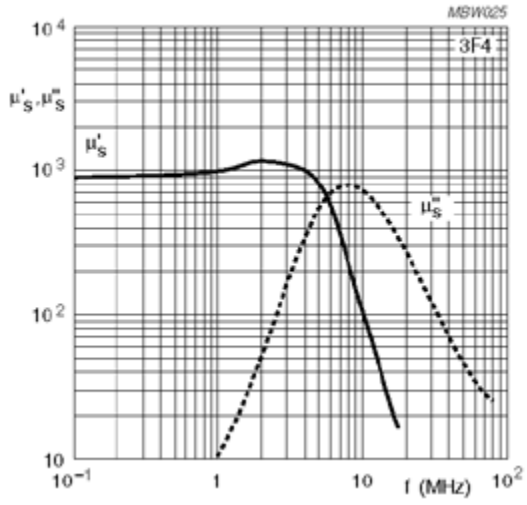

Fig. 4.8. Real part μ_s' and imaginary part μ_s'' of complex permeability versus frequency for 3F4 material.

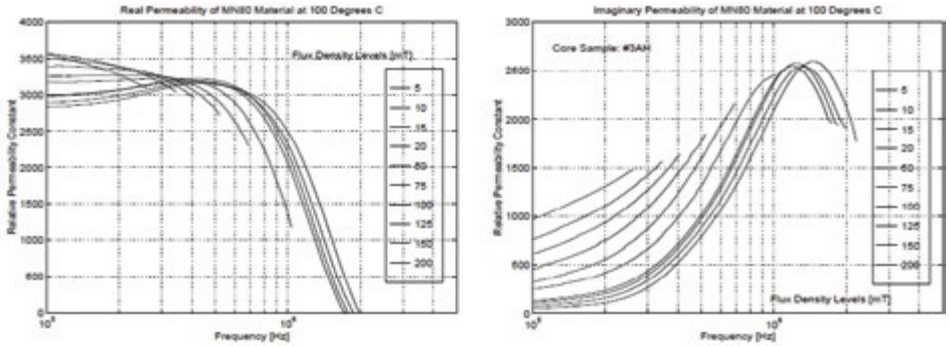

Fig. 4.9. MN80 real (left) and imaginary (right) permeability at *100 °C* with different B_{max} values [64].

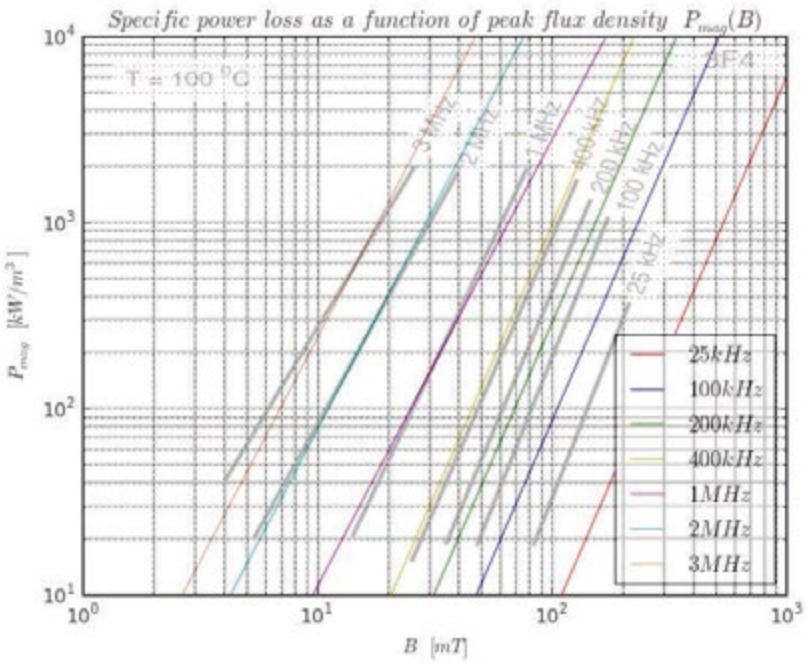

Fig. 4.10. Core losses estimated with Steinmetz equation (coloured) superposed on measured (thick black) core losses for 3F4 material.

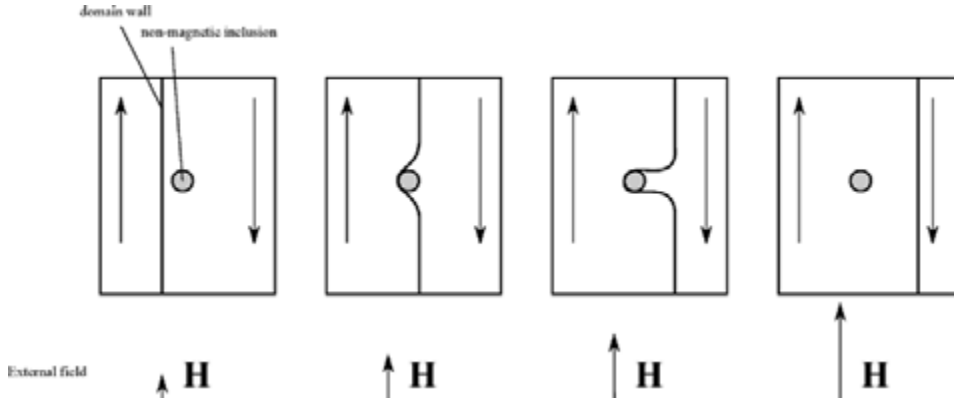

Fig. 4.11. Domain wall movement behavior due to external field and pinning.

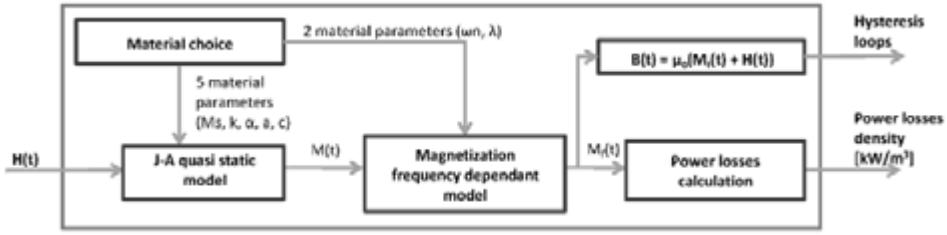

Fig. 4.12. Implemented hysteresis model structure.

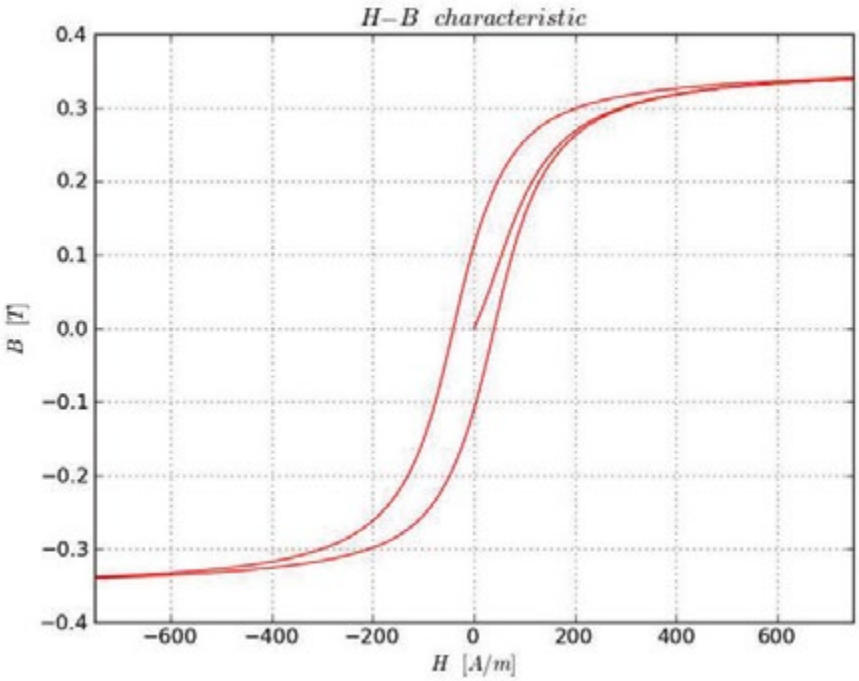

Fig. 4.13. Full saturation hysteresis loop for 3F4 material evaluated for a *10 kHz* sinusoidal signal.

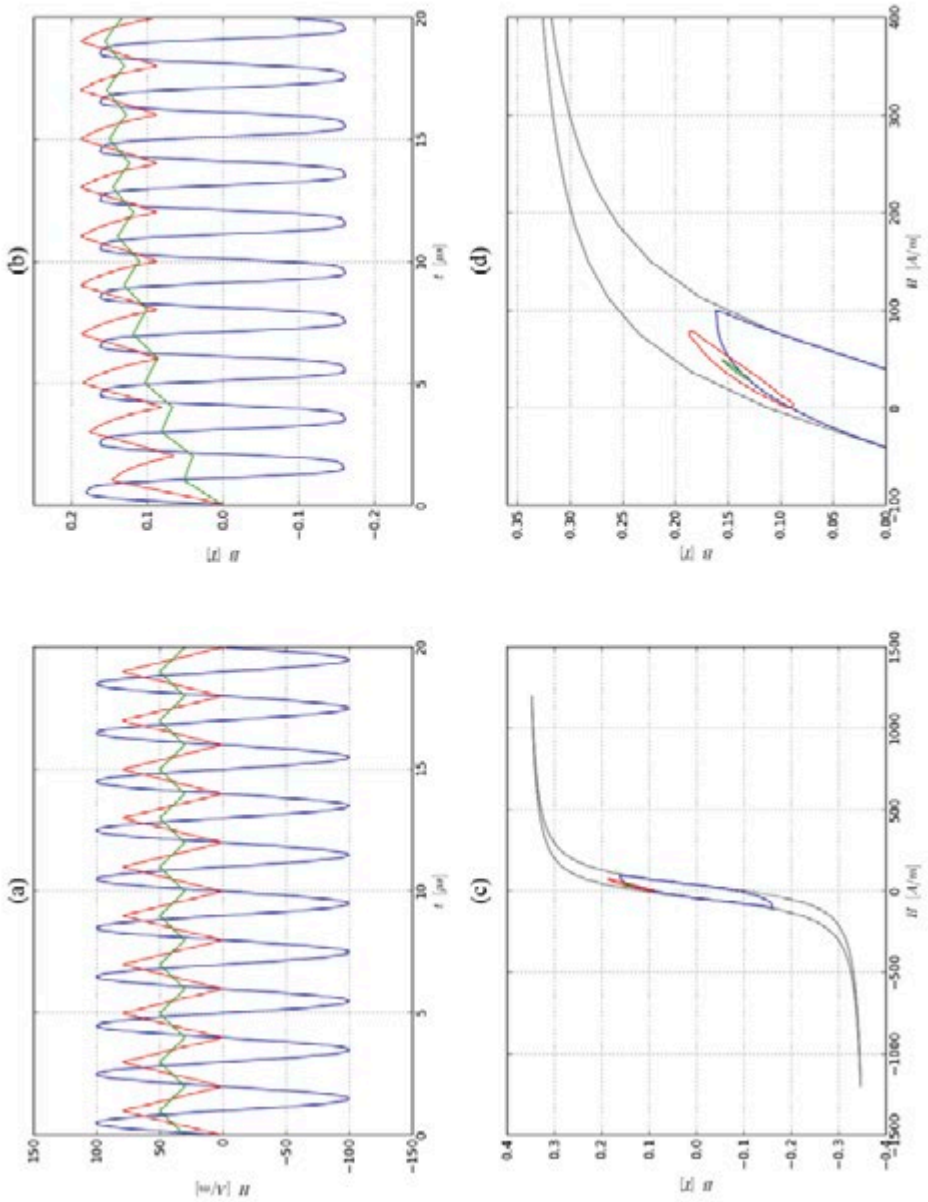

Fig. 4.14. Different H(t) stimuli (a): sinusoidal (blue), triangular (green), triangular boundary mode (red); their calculated B(t) (b); their steady state B-H loops compared with full saturation hysteresis (black) for 3F4 material (c) and a close-up of the same loops (d). The signals' period is *500 kHz*.

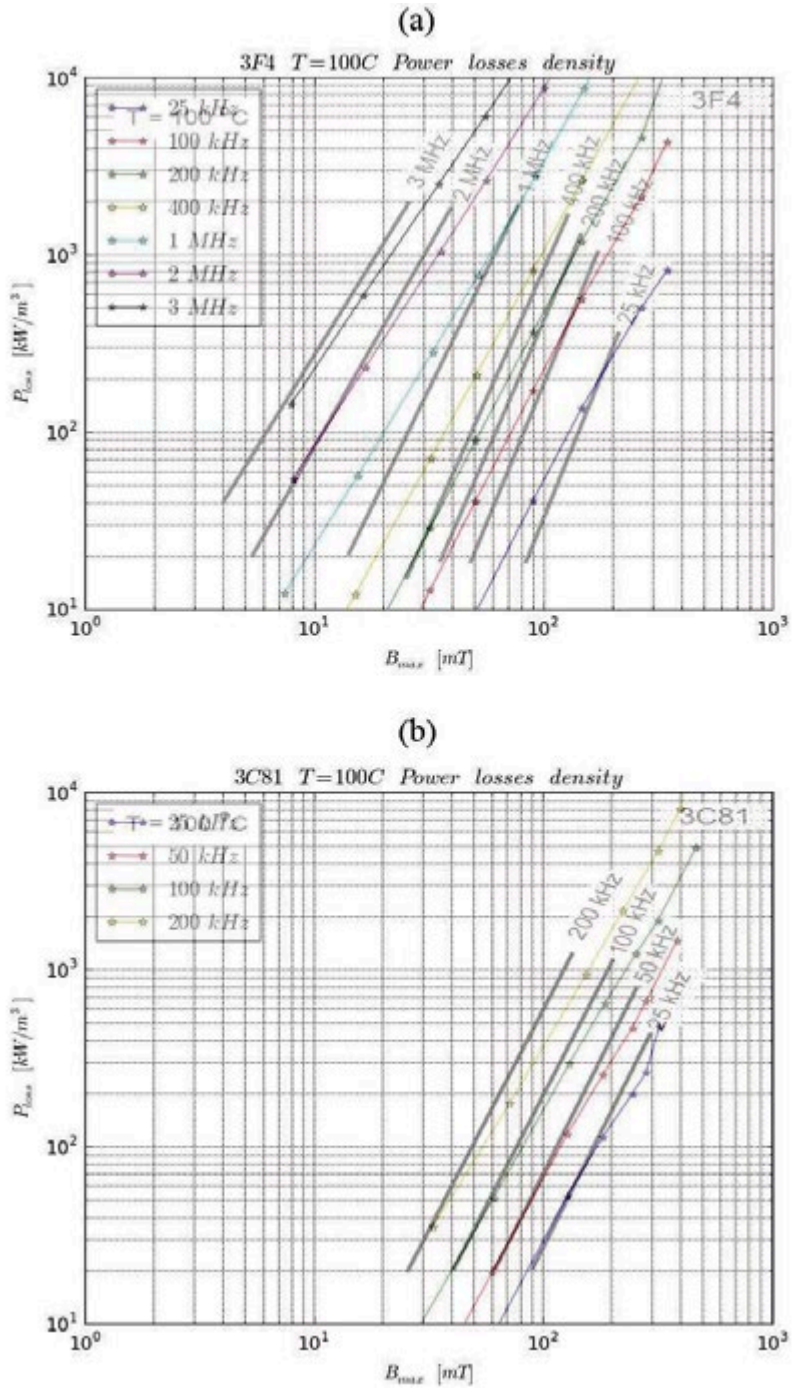

Fig. 4.15. Estimated power losses density compared against datasheet for 3F4 (a) and 3C81 (b) materials. Dotted lines: estimated values at *100 °C*. Bold black lines: material datasheet power loss densities measured at *100 °C* [87, 88].

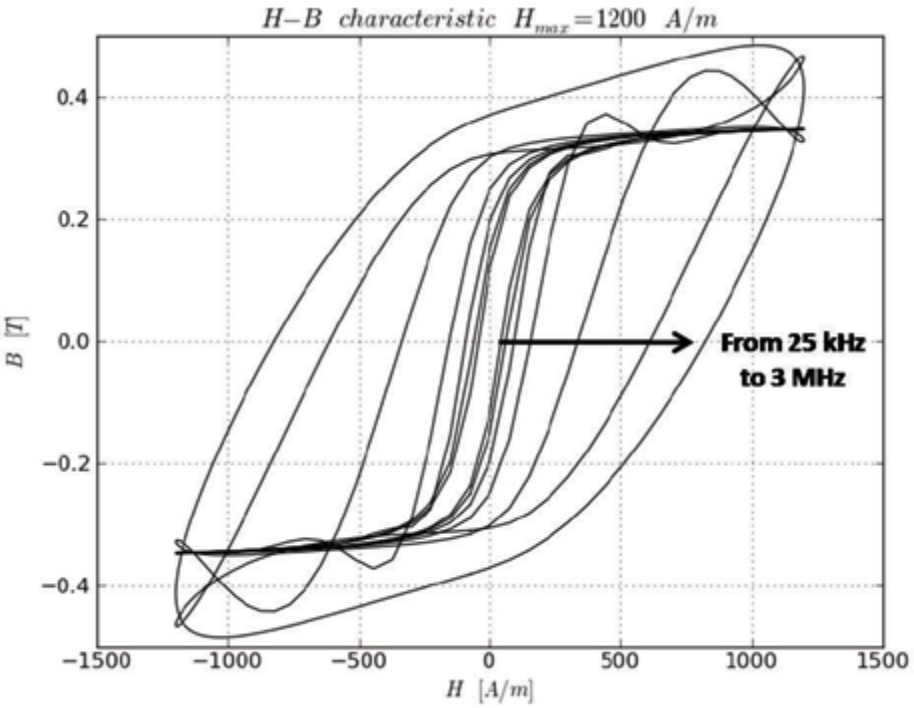

Fig. 4.16. Frequency behavior of 3F4 loop estimated with the second order frequency model.

Chapter 5
Hysteresis measurement setup

In previous chapter, a frequency-dependent hysteresis model has been described, implemented with SAGE and applied to estimate the core losses of two commercial soft ferrite materials with reasonable accordance. However, in order to obtain a more accurate estimation, additional experimental measurements are required to calibrate the model both in frequency and temperature behaviour. For this reason this chapter describes the work done for the design of an hysteresis measurement setup which can be used to calibrate the model. Before entering into the details related to the hysteresis characterization setup, it is important to briefly recall the experimental characterization of core loss.

The experimental characterization of core loss is mainly obtained with two methods: by measuring applied voltage and current on an inductor test sample [89] or by calorimetric analysis [90]. Calorimetric analysis requires specifically dedicated and more complicated setups involving the thermal and mechanical design of calorimeters while electrical characterization is of simpler implementation and it correctly estimates the losses at quasi-static and low frequency condition (i.e. below *100 kHz*) [91]. At higher frequencies this second method is affected by phase discrepancy error [92].

Various solutions have been proposed to counter the phase discrepancy; these are mainly based on minimizing the phase angle between measured voltage and current by exploiting resonance mode [93 ,94]. However, these methods are mostly valid for losses estimation only with sinusoidal excitations, even if a solution for wide band excitations has been proposed [95]. The main drawbacks of these setups are that they require additional components with values depending on the CUT inductance value (i.e. resonant capacitors, air-core transformers) or additional transformers to include the DC bias. At the same time they loose the information on hysteresis loop shape due to the v to i phase angle minimization technique.

On the other hand, a setup capable of measuring hysteresis provides additional information directly related to the hysteresis loop's shape (i.e. inductance value depending on the operating point, study of inductor demagnetization, study of saturation). In order to calibrate the previously introduced model and develop a simpler electronic setup, which can provide a DC bias without any additional transformer and which can work for an arbitrary waveform, we decided to investigate this approach trying to minimize the impact of phase discrepancy.

The work presented by Walker [96] has been focused on evaluating both temperature and frequency behavior using an electronic setup capable of controlling the

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core's excitation current. In fact, current excitation is linear with magnetic field *H(t)* and ensures a direct comparison with Jiles-Atherton model where *H(t)* is the input. With respect to temperature, this work has been focused on modeling both static and dynamic conditions. With respect to frequency, the electronic setup allowed investigations up to *100 kHz* with a peak current of *2.5A*.

Our work aims to extend the capabilities of investigation of hysteresis loop with higher frequency, higher current and simpler solution for applying a DC bias. For achieving such requirements we have designed an electronic set up based on a power voltage controlled current source (VCCS) with a modular architecture and accurate current sensing with minimization of current sensing resistor's parasitic inductance.

Section 5.1 describes the proposed electronic system. The measurement principle used is briefly recalled. Then a description of the various parts and functionality is given focusing on the system functionality and flexibility in terms of possible measurements and computing. The main issues solved in the design of the VCCS, including considerations on stability, choice of sensing components and measurement error contributions, are explained. Section 5.2 shows measurement results taking into account both air-core and magnetic-core sample inductors. The former are used as a validation for the proposed design sizing and the latter are characterized in terms of magnetic hysteresis behavior for different operating conditions. Measurements demonstrating the agreement with datasheet results are shown for some commercial ferrite core samples. As a demonstration of the setup capabilities, the frequency and temperature dependent behavior of the hysteresis of the same samples is characterized. Finally, an example of composite excitation with variable DC bias and different current waveforms is shown.

5.1 System overview

5.1.1 Magnetic hysteresis measurement principle

The hysteresis measurement is based on the two windings method with a nominal 2:1 ratio [89, 92]. Using this approach, the winding resistance voltage drop does not affect the measurement. The different Core Under Test (CUT) samples are of toroidal shape for better field confinement. The applied magnetic field strength *H(t)* and magnetic flux density *B(t)* of the CUT are obtained as in equations 5.1 and 5.2 respectively measuring the current *i(t)* applied through the primary winding and the secondary winding voltage *v(t)*.

$$H(t) = \frac{N_1 i(t)}{l_e} \tag{5.1}$$

$$B(t) = \frac{1}{N_2 S}\int_0^t v(\tau)d\tau \tag{5.2}$$

The parameters depend on the geometry of the core. N_1 is the number of windings at primary side, N_2 the windings at secondary, S the cross-sectional area of the core, l_e the effective length of the magnetic path. In this paper we assume a uniform magnetic field distribution inside the core.

5.1.2 Setup description

The proposed setup scheme is shown in Fig. 5.1 while Fig. 5.2 shows a picture of the implemented system. As it is possible to notice from equation 5.1, the relationship between *i(t)* and *H(t)* is linear, thus we decided to control the current flowing in the CUT. In this way it is possible to assume that we are exciting the material with a known *H* waveform while *B* will depend on the hysteretic magnetic response of the CUT. Moreover, the current control allows setting excitation currents which can have significant DC components. This is of particular interest when testing materials used in choke inductors or DC-DC power inductors. For this purpose, an Agilent 33120A arbitrary waveform generator (ARB) is used to provide the desired magnetic field waveform to a power VCCS. The VCCS converts the voltage output of the ARB in a current signal which is directly used to drive the core. This power electronic circuit has been designed as explained in the next section. A Tektronix TDS3054B oscilloscope is used to measure the secondary winding voltage v by means of a P6246 differential voltage probe and a voltage v_r proportional to the current i with a P6139A voltage probe. The differential measurement of v allows the maximum rejection of undesired common mode voltages which could be generated by parasitic due to the windings and the ground traces of the VCCS power circuit. While the measurement of v is direct, i is obtained by measuring v_r and the value of the sensing resistor R_s with a 34410A digital multimeter. The direct measurement of the current with a current probe has been avoided for two reasons: the band-pass behavior of the current probe and the consequent different phase delay introduced with respect to the voltage probe. Nevertheless, the voltage measurement of v_r done directly on the sensing resistor R_s is perturbed by its parasitic inductance which affects both current's magnitude and phase estimation at high frequency. In order to minimize the influence of this parasitic inductance, an additional R-L network is used as explained in subsection 5.1.6. Both the ARB and the oscilloscope are directly interfaced with the MATLAB environment through the Instrument Control Toolbox.

This solution has been adopted for the following reasons:

1) avoid an electronic hardware version of the integrator needed in equation 5.2 which can introduce additional complexity and distortions;
2) realize an automated measurement system;
3) keep flexible computing capability on measures and real-time results visualization.

The MATLAB scripts which have been developed define two modes of operation. A real-time hysteresis scope and an automated acquisition of hysteresis as a function of one or more parameters. The first mode is useful to see the variations occurring in the hysteresis loop when manually changing the parameters of the ARB,

oscilloscope and VCCS. This implements the functionality of common setups with an electronic integrator circuit and an oscilloscope set with channels in X – Y mode but has the advantage of eliminating the electronic integrator non-idealities by doing a numerical integration. The second mode allows the acquisition of multiple hysteresis loops which are subsequently plotted on the same graph as one or more parameters vary (e.g. waveform frequency, *H* amplitude, waveform type, DC bias, temperature). This is useful for the characterization of magnetic materials behavior under different operating conditions. An additional functionality of the scripts is the autoscaling of oscilloscope waveforms before acquisition. This allows the use of the full dynamic range of the oscilloscope, which implements a 9 bit ADC, under every waveform amplitude.

5.1.3 Voltage Controlled Current Source

The voltage controlled current source must have the capability to bring the CUT to saturation while still providing a stable control of the current flowing in it. Its transconductance g_m transfer function can be defined as in 5.3.

$$g_m(s) = \frac{i(s)}{v_{ARB}(s)} \tag{5.3}$$

where s is the Laplace variable. Considering equation 5.1 it is possible to estimate the maximum current needed to reach the saturation. We decided to assume a maximum magnetic field strength $H_{max} = 2000\ A/m$ which is enough to saturate the soft materials of interest. With respect to the core geometry we assumed $l_e \leq 25mm$, $N \leq 10$ to ensure the capability of a manual winding of the test samples but still limiting the maximum inductance generated by the CUT. These values give a maximum current $I_{max} = 5\ A$.

Using operational amplifiers, there are two main configurations which can be adopted to implement a VCCS depending on whether the load is grounded or not [97]. The grounded solution is based on the "Howland current pump" [98] which has severe requirements of matching between the feedback resistors [99, 100]. For this reason we adopted the floating load solution designed as in Fig. 5.3. An input stage provides $50\ \Omega$ impedance matching for the ARB output signal $v_{ARB}(t)$ and an adjustable gain. The second stage accomplishes the voltage to current conversion. An LM7171 operational amplifier is followed by four EL2009 current boosters which have been paralleled to meet the requirements in terms of drive current [50]. With a gain of $2\ V/V$ set on the first stage and $R_s = 2\ \Omega$ a $g_m = 1\ S$ is achieved.

The operational amplifiers are chosen with high gain-bandwidth products to ensure a non limiting frequency behavior in the bandwidth of interest. Same considerations apply to the boosters.

The power supplies $V_+ = +17\ V$, $V_- = -17\ V$ are properly decoupled with ceramic and tantalum capacitors. This supply range guarantees an output voltage dynamic range of $\pm 16\ V$. This limit is imposed by the maximum supply voltage range of the used components.

The P6246 differential probe presents a maximum input voltage rating for linear response of $8.5\ V$ from each input to common ground. For this reason the CUT

winding ratio has been set to 2:1. Aluminium heat sinks and two fans with a diameter of *40 mm* provide a proper thermal dissipation for the current boosters, sensing resistor and CUT.

Placing the non-linear inductive load inside the feedback loop gives advantages in terms of accuracy and linearity of the current control. However this directly affects the stability and transfer function of the circuit. For the purpose of stabilization it is convenient to consider the voltage gain A_v transfer function:

$$A_v(s) = \frac{v_{out}(s)}{v_{ARB}(s)}. \tag{5.4}$$

The main feedback path transfer function β, which includes the CUT, can be defined as:

$$\beta(s) = \frac{R_s}{R_s + Z_{CUT}(s)}, \tag{5.5}$$

where $Z_{CUT}(s)$ is the CUT impedance. This is obtained under the approximations of $i_x(t) << i_s(t)$ and $ESL = 0$ which are valid under the assumptions explained in subsection 5.1.6. For this reason, the branch of R_x and L_x can be neglected in stability calculation.

The stabilization technique adopted here is based on the rate of closure between the voltage gain and the feedback network [97] and it is provided through an additional high frequency feedback path β_c composed by R_c, C_1 and R_p defined as:

$$\beta_c(s) = \frac{R_p + R_s}{R_p + R_s + R_c + \frac{1}{sC_1}}. \tag{5.6}$$

The capacitor $C_2 = 68\ pF$ and resistors $R_b = 100\ \Omega$ are needed to provide the stabilization of the boosters. The C_2 value has been set with the help of AC simulation while R_b is recommended by EL2009 datasheet.

The impact of CUT on the circuit transfer function has been estimated with a LTspice AC simulation. For the purpose of this simulation the CUT has been modeled as an ideal inductor of values ranging from *10 μH* to *10 nH* with a series resistance $R_{CUT} = 0.2\ \Omega$. The operational amplifiers have been modeled with the parameters obtained from the manufacturers' datasheets and the boosters with the SPICE model provided in the datasheet. The result is shown in Fig. 5.4.

Comparing the open loop response A_{OL} of the amplifier composed by the LM7171 and the boosters with the reciprocal of the feedback transfer function $1/\beta$ it is possible to observe that the feedback response varies with the CUT inductance value and that the rate of closure is of *40 dB/decade* in the whole range of interest. For this reason the secondary feedback path $1/\beta_c$ is provided for compensation which is ensured as the secondary feedback path becomes dominant at the closure. The values of $R_c = 1\ k\Omega$ (trim pot), $R_p = 100\ \Omega$, $C_1 = 1\ nF$ are chosen to meet the compensation of the biggest inductance value of interest which is *10 μH*. The trim pot allows optimal compensation with the different CUTs. The current i is then stably controlled at frequencies where it can be assumed that:

$$|Z_{CUT}(j\omega)| \ll \left|R_c + R_p + \frac{1}{j\omega C_1}\right|. \tag{5.7}$$

In this range, the main feedback path is dominant and the transconductance g_m can be approximated as:

$$g_m(s) \approx \frac{v_{out}(s)}{v_{ARB}(s)} \cdot \frac{1}{R_s(s) + Z_{CUT}(s)} = \frac{i(s)}{v_{ARB}(s)}. \tag{5.8}$$

An important consideration is related to the fact that we are not directly measuring the current flowing through the CUT but instead the current $i_s(t)$ flowing in R_s. We can define a transconductance g_{mr} as:

$$g_{mr}(s) = \frac{i_s(s)}{v_{ARB}(s)}. \tag{5.9}$$

We need to verify an assumption in estimating i using this indirect method. This is that g_{mr} closely matches g_m. This can be reduced to proving that the current $i_s(s)$ flowing through R_s closely matches $i(s)$ which is based on the same assumption done in 5.8. Fig. 5.5 shows the ratio $i(s)/i_s(s)$ for a simulation with different CUT values. The closer to 0 dB the ratio is, the better the current sensing. It is possible to notice how the current i can be estimated by the measurement of i_s in a frequency range that is larger as the CUT inductance decreases.

Moreover, R_s has a parasitic inductance *ESL* which can cause its impedance to vary from a purely resistive value. For this reason, the current $i_s(s)$ is not directly estimated as $v_x(s)/R_s$ but instead it is obtained adding the R_x - L_x network, which minimizes the influence of parasitic inductance, and measuring $v_r(s)$. This analysis is explained in detail in subsection 5.1.6.

5.1.4 Setup performance boundaries

The proposed setup has boundaries to its performances directly related to its VCCS behavior and physical implementation. In fact, as already explained, the inductance value of the CUT set the upper frequency limit to which it is possible to characterize the hysteresis at full saturation. The results in Fig. 5.4 indicate a $g_m \approx 1\ S$ characterization limited to few hundreds of *kHz* for an ideal $10\ \mu H$ inductor which is extended to around *10 MHz* for an ideal *100 nH* inductor. This limitation is related to the higher impedance of the more inductive CUTs as the frequency increases. As the frequency goes up, the amplifier needs more voltage to maintain the same current flowing through the CUT. As the required voltage exceeds the values of the VCCS output voltage dynamic, the system is not capable of correctly controlling the current.

To get a better estimation of this limit, we can consider a sinusoidal current signal with a peak amplitude I_{max} sufficient to reach the saturation of the core under test. If we suppose the system ideal and only limited by CUT inductance value L and VCCS output peak voltage V_{peak}, we can define a maximum frequency f_{max} at which we can be sure to properly control the current as in 5.10.

$$f_{max} \approx \frac{V_{peak}}{2\pi L I_{max}} \tag{5.10}$$

Fig. 5.6 shows an evaluation of 5.10 for our case where $V_{peak} = 16\ V$, $I_{max} = 5\ A$. This boundary can be extended by providing a higher output voltage dynamic.

5.1.5 Phase delay errors evaluation

A significant measurement error on phase between *v(t)* and *i(t)* can lead to non-consistent results. Three main contributions leading to a phase measurement error have been addressed: the oscilloscope sampling frequency, the phase mismatch between the voltage probes and the parasitics.

The Tektronix TDS3054B oscilloscope sampling frequency is *5 Gsamples/s*, this gives a *200 ps* error on phase which is *0.72°* at *10MHz*. We considered this contribution negligible as it gives an error of *0.2 %* at the highest frequency.

With respect to the second contribution we have measured the P6139A and P6246 probes phase mismatch connecting them in parallel on a *50 Ω* load and testing in a range [*1 kHz*, *10 MHz*] with a sinusoidal signal of $8.5\ V_{pp}$ (maximum linear dynamic of P6246 probe). The phase difference measured with oscilloscope was below *0.2°* up to *2 MHz* and within *0.8°* up to *10 MHz*.

With respect to the parasitic components, the main contribution is related to the parasitic Equivalent Series Inductance (*ESL*) of the sensing resistor R_s which has required a careful analysis treated in the next section.

5.1.6 Current sensing network design

5.1.6.1 Sensing resistor: parasitic analysis and design

The sensing resistor R_s has quite severe requirements. Following the VCCS requirements it should be rated to stand an RMS power $P_r = 25\ W$, with a max $I_{peak} = 5\ A$, and it should also have an *ESL* as low as possible. To test the impact of the sensing resistor's ESL on the current sensing a LTspice simulation of the circuit of Fig. 5.3 has been done modeling R_s as an ideal resistor plus an *ESL* of different values (i.e. *1 nH*, *10 nH*, *100 nH*). The $i(s)/i_s(s)$ ratio already introduced in subsection 5.1.3 has been replaced by the ratio $i(s) \cdot R_s/v_x(s)$. This ratio takes into account the approximation of the sensing resistor to the sole real part of its impedance $Z_s = R_s + j\omega \cdot ESL$. Fig. 5.7 shows the result of this comparison for the different values of *ESL* and for different CUT values. While the *ESL = 1 nH* case is practically identical to the ideal case shown in Fig.5.5, the case with *ESL = 10 nH* shows a slightly incremented phase shift at the higher frequencies. The case with *ESL = 100 nH* shows a dramatic reduction of the frequency range which provides a correct estimation of *i*, independently of CUT inductance value.

To give a better idea of how the ESL influences the hysteresis loop measurement a CUT has been modeled with the non-linear core model available in LTspice [101]. The model parameters, set to simulate a 3F45 TC4/2.2/2 core with 3 windings, are: $H_c = 60$, $B_s = 0.42$, $B_r = 0.15$, $A = 1.75 \times 10^{-6}$, $L_m = 9.18 \times 10^{-3}$, $L_g = 0$,

N = 3. Transient simulations with a sinusoidal input have been made at various frequencies (i.e. *10 kHz* to *10 MHz*) and the relative hysteresis loops results, obtained applying equations 5.1 and 5.2, are shown in Fig. 5.8.

The value of *ESL = 1 nH* is a best-case with respect to our prototype physical implementation while *ESL = 100 nH* solution is a worst-case not very far from the parasitic *ESL* shown by standard ceramic power resistors. An *ESL = 10 nH* seems to be a good trade-off both in terms of feasibility and sensing accuracy. Due to the high power rating required, our choice has been the commercial Caddock MP850 *2 Ω 1%* power resistor which has a parasitic inductance [102] of *10 nH* with a TO-220 power package. The DC resistance has been measured with the 34410A digital multimeter giving $R_s = 2.020 \pm 0.001\ \Omega$. A solution with a lower *ESL* could probably be implemented using several SMD resistors in parallel and a proper PCB layout.

5.1.6.2 Measurement network of the current signal

In order to further minimize the impact of the sensing resistor's *ESL*, the R_x - L_x compensation network shown in Fig. 5.3 has been used to obtain the current measurement. Its operation can be explained starting by considering the impedance of the sensing resistor as:

$$Z_s = R_s + sESL \tag{5.11}$$

and the impedance of the R_x - L_x branch as:

$$Z_x = R_x + sL_x. \tag{5.12}$$

The currents flowing in the two branches can be calculated as:

$$i_s = \frac{v_x}{Z_s}; \tag{5.13}$$

$$i_x = \frac{v_x}{Z_x} = \frac{v_r}{R_x}. \tag{5.14}$$

Combining equations 5.11, 5.12, 5.13 and 5.14 we can obtain i_s as:

$$i_s = \frac{R_x\left(1 + s\frac{L_x}{R_x}\right)}{R_s\left(1 + s\frac{ESL}{R_s}\right)}\frac{v_r}{R_x}. \tag{5.15}$$

If we set $L_x/R_x = ESL/R_s$ the two time constants are equal and i_s results:

$$i_s = \frac{v_r}{R_s}. \tag{5.16}$$

Consequently, matching the time constants, we can measure i_s without knowing the exact value of the parasitic inductance *ESL*. Most of all, the compensated relationship between v_r and i_s is linear and independent from frequency. Considering that the assumption $i_s \approx i$ must be valid for a proper measurement, we need to minimize i_x. For this reason, we have chosen $i_x = i_s/50$ as a trade-off between current absorption and v_r voltage amplitude. Thus we have $L_x = 50\ ESL$ and $R_x = 50\ R_s$. Due to the fact that the *ESL* value is unknown, we have set $L_x = 500\ nH$ and used a $2\ k\Omega$ precision potentiometer to adjust R_x in order to match the time constants. The benefit of this compensation network is shown in Fig. 5.9. The calibration of the physical circuit has been achieved by measuring i current and i_x current with a Tektronix P6022 current probe using v as time reference. The potentiometer has been trimmed to match amplitude and phase of both currents on a sinusoidal test signal at *5 MHz*, *350 mA* peak.

5.1.7 VCCS transconductance measurement

Once the sensing resistor has been chosen, it is possible to verify the behavior of the implemented VCCS against the simulated results. For this purpose, two PCB air-core inductors with different inductance values have been used to measure the frequency behavior of g_{mr}. The use of linear-core inductors allows a direct comparison with AC simulations and can also be exploited as a calibration reference. The first inductor has $11\ \mu H$ of nominal inductance and $180\ m\Omega$ of ESR and the second has *80 nH* of nominal inductance and $80\ m\Omega$ of ESR. Fig. 5.10 shows the frequency response of g_{mr} measured with the air-core inductors against the simulated behavior. This proves how the VCCS behavior is in accordance with the simulated results when using linear inductors. Considering the limitations of the current sensing done through R_s, the g_{mr} measure can be considered correctly estimated only up till a certain frequency depending on the CUT value. For this reason the reliable data interval is shown with a line joining the markers.

5.2 Results

5.2.1 Ferrite materials test samples

Different test samples have been realized using Ferroxcube 3F45, Ferroxcube 4F1 and FairRite 67 ferrite materials. These materials have been chosen as a reference to test the proposed setup. The windings have been manually wound using enameled copper wire AWG 24. The number of windings N_1 has been chosen simply reverting 5.1 and considering the magnetic field values required to reach saturation from the datasheets of the materials and the peak current of the VCCS, $I_{max} = 5\ A$. An estimation of the small signal inductance has been used to get a feeling on the maximum frequency range which could be reached with a specific CUT. In this estimation we considered the initial permeability μ_i from datasheet and inductance is evaluated as:

$$L = \frac{\mu_0 \mu_i N_1^2 S}{l_e}. \tag{5.17}$$

The realized test samples are listed in Table 5.1. An estimation of primary winding equivalent series resistance ESR_1 has been obtained as:

$$ESR_1 = \left(2\pi \sqrt{\frac{S}{\pi}} N_1 + l_c \right) \frac{\rho}{A} \tag{5.18}$$

where $\rho = 1.678 \times 10^{-5}\ \Omega \cdot mm$ is the copper resistivity, $l_c = 15\ mm$ takes into account the contacts and $A = 0.2\ mm^2$ is the AWG 24 cross-sectional area.

For simplicity the different samples will be identified with the serial number reported in Table 5.1 throughout the chapter. Fig. 5.11 shows a picture of the realized samples.

Table 5.1 Magnetic core test samples.

Serial N.	Core Material	Core size	$L\ (\mu H)$	N_1	N_2	$ESR_1\ (m\Omega)$
1	*3F45* $\mu_i = 900$ $H_s = 1000\ A/m$	*TN10/6/4* $l_e = 24.1\ mm$ $S = 7.8\ mm^2$	*13.2*	*6*	*3*	*6.3*
2	*4F1* $\mu_i = 80$ $H_s = 1500\ A/m$	*TN10/6/4* $l_e = 24.1\ mm$ $S = 7.8\ mm^2$	*2.08*	*8*	*4*	*7.9*
3	*3F45* $\mu_i = 900$ $H_s = 1000\ A/m$	*TC4/2.2/2* $l_e = 9.18\ mm$ $S = 1.75\ mm^2$	*3.45*	*4*	*2*	*2.8*
4	*4F1* $\mu_i = 80$ $H_s = 1500\ A/m$	*TC4/2.2/2* $l_e = 9.18\ mm$ $S = 1.75\ mm^2$	*0.31*	*4*	*2*	*2.8*
5	*67* $\mu_i = 40$ $H_s = 1500\ A/m$	*5967000101* $l_e = 13\ mm$ $S = 2\ mm^2$	*0.124*	*4*	*2*	*2.9*

5.2.2 Hysteresis loop characterization of magnetic cores

The first measurement is related to the comparison of hysteresis with datasheet values. The measurements have been taken with a sinusoidal *H(t)* at a frequency of *10 kHz* and a peak value equal to the specific sample H_s from Table 5.1. Fig. 5.12 shows the measured *v(t)* and *i(t)* obtained for sample 1. We can observe the presence of two spikes in the current waveform. These are related to the finite bandwidth of the control loop. In fact, as the CUT saturates, it presents a very rapid voltage variation. This variation is corrected by the VCCS feedback, in terms of provided current, with a delay dependent on its closed loop bandwidth. Applying 5.1 and 5.2 the hys-

teresis loop is then estimated by *i(t)* and *v(t)* averaged measurement over a period. Fig. 5.13 shows the result for sample 1, Fig. 5.14 for sample 2. In both figures, it is possible to notice how the current spike affects the loop on the ascending curve in the first quadrant and symmetrically on the descending curve in the third quadrant. The induction field saturation value B_{sat} is well estimated while the remanence field and the coercive magnetic fields are overestimated with respect to datasheet values.

The hysteresis changes if measured on smaller cores like samples 3 and 4, this is probably related to a less uniform magnetic field distribution inside the smaller cores. The principal effect that can be noticed with respect to the bigger cores is a variation of B_{sat} which can be related to a coupling factor that differs from the nominal 2 : 1 ratio. For this reason the coupling of primary to secondary winding has been measured at *10 kHz* by applying a *1 V* peak sinusoid at the primary side. Sample 3 has shown a measured coupling of 2 : 1.1 and sample 4 has shown a measured coupling of 2 : 0.9. Fig. 5.15 shows the hysteresis results for sample 3 taking into account the measured coupling factor.

5.2.3 Frequency behaviour

To study the behaviour of the hysteresis loop with frequency, a MATLAB script has been written to automatically set the oscilloscope and ARB and acquire the loops for an array of frequency values. As frequency increases the core losses increase causing a sensible variation of the core temperature which ultimately affects the magnetic properties. The frequency behaviour has been evaluated keeping the lower losses possible as the frequency increases thus preventing the heating of the core. This has been done using a limited burst of sinusoidal current cycles, thus limiting the average power passed to the core. This method is explained in detail in the next subsection. The measurements have been taken at ambient temperature (*25 °C*). Fig. 5.16 shows the estimated loops for sample number 3. It is possible to notice how the full saturation limit imposed by the response of the VCCS gives smaller loops for frequencies greater than *500 kHz*. Using a lower inductance core, like sample 4, we can observe in Fig. 5.17 how the hysteresis loops at full saturation can be obtained also at higher frequencies.

5.2.4 Test signal with multiple waveforms and DC bias

In order to show the different behavior of the hysteresis loop depending on the magnetic field *H* excitation's amplitude, frequency, DC bias and shape the current test signal in Fig. 5.18 has been applied to sample 5. This signal is composed by a sequence of five different waveforms: *2.5* A_{pp} sine with *2.5 A* DC bias, *5* A_{pp} sine with *2.5 A* DC bias, *10* A_{pp} sine with zero DC bias, *1.5* A_{pp} triangular with *1.25 A* DC bias, *10* A_{pp} degaussing signal with damped sine wave. This composite signal has been tested for two different waveforms' frequencies: on the left *100 kHz* and on the right *500 kHz*. From the measurement of *v* and *i*, *H* and *B* have been calculated applying 5.1 and 5.2. The hysteresis loops related to the different waveforms are highlighted with different colours. The purpose of the degaussing signal is to remove the

residual magnetization at the end of each waveform sequence. For a better clarity, it is not shown in the hysteresis loops.

This result demonstrate the usefulness of the realized setup to perform a real-time hysteresis analysis. The example shows how at different operating conditions the area and the average slope of loops varies. Consequently the core losses and equivalent inductance are affected. This effects are important for example in power conversion electronic design.

5.2.5 Temperature dependence of hysteresis loop

As already introduced, the magnetic properties of core materials are highly dependent on their temperature. As the frequency f of the test signal increases the core losses due to hysteresis and eddy currents increase causing a heating of the core. This can be demonstrated applying to the core a current signal which is composed by bursts of N_{cyc} cycles of a periodic signal with a certain burst repetition frequency BRF. For a fixed BRF value, as N_{cyc} varies the power losses produced by the core are proportional to a duty cycle D defined as in 5.19.

$$D = \frac{N_{cyc} \cdot BRF}{f} \tag{5.19}$$

Fig. 5.19 shows the behavior of sample 3 when a sinusoidal current with $I_{peak} = 3.7\ A$ and $f = 500\ kHz$ is applied as bursts with a $BRF = 100\ Hz$ and for various D values. The fans have been disabled to allow a proper thermal transient of the CUT during the measurement. Fig. 5.20 shows the thermal images acquired with a FLIR B335 thermal imaging camera for the different values of D shown in Fig. 5.19. As D increases the core heats up, its magnetic properties change thus the B_{sat} decreases and consequently the CUT impedance, too. This varies the VCCS feedback compensation behavior which affects the g_m and ultimately the H_{max} value.

5.3 Conclusions

In this chapter the design of a setup for the hysteresis characterization of soft magnetic materials has been presented. The setup is capable of generating programmable magnetic field waveforms, which includes also DC bias, through the control of the CUT current. This can reach peak values up to $10\ A$ peak-to-peak, in a frequency bandwidth up to $500\ kHz$ depending on the CUT inductance value.

The proposed solution is based on a power VCCS whose design has been described focusing on stability, passives selection and parasitics compensation. The hysteresis characterization can benefit of a versatile and real-time computing, implemented with MATLAB scripts, which combines both the generation of specific test signals and computing of the acquired results through the interface with laboratory instrumentation.

An overview on the possible setup applications has been shown with experimental results obtained with inductors in the range from $100\ nH$ to $10\ \mu H$ made with 3F45, 4F1 and 67 ferrite materials. At first, the realized samples have been used to

compare the estimation of measured hysteresis loops against manufacturer's data with good agreement.

Additional measurements focusing on large signal frequency and thermal behaviour of hysteresis have been presented in order to explore the system capabilities. These have shown a qualitative behaviour which is in agreement with the physics of ferrite materials. However, in order to quantitatively estimate hysteresis parameters, a system calibration is needed.

A test with multiple waveform shapes and DC bias values has shown that the system is capable of working with arbitrary signals up to *500 kHz* (considering *10* A_{pp} signals) which can be useful to simulate real operating conditions of power inductors.

Finally, another application of the power VCCS is as current driver of high frequency coils in medical research, where the realized system has higher peak current capabilities, frequency bandwidth and compactness with respect to similar solutions proposed in literature [103].

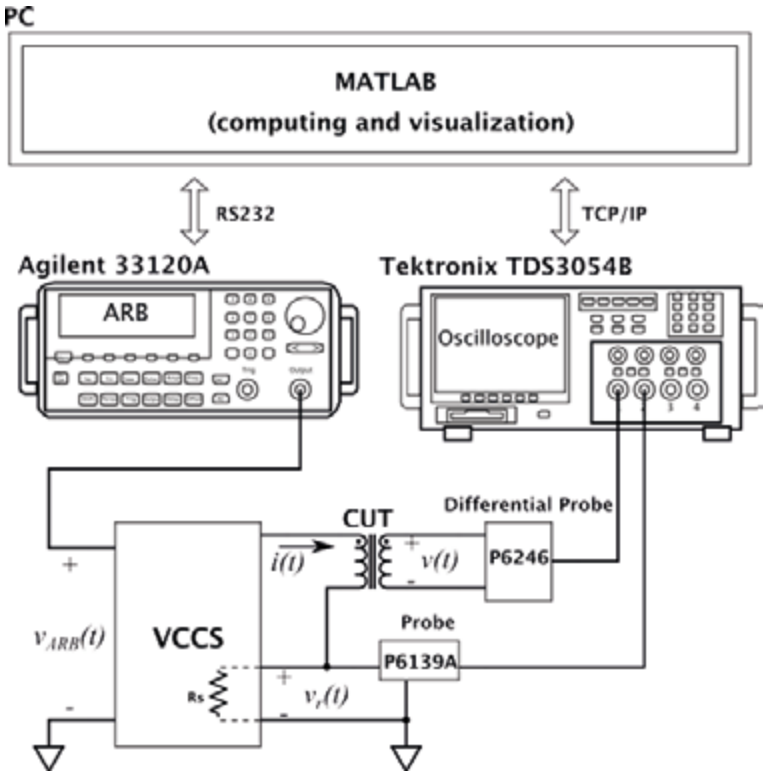

Fig. 5.1. Hysteresis loop characterization setup scheme.

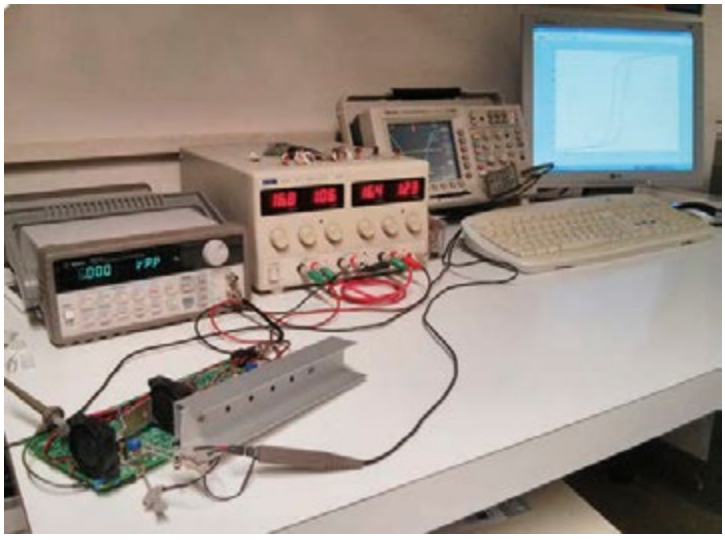

Fig. 5.2. Hysteresis loop characterization setup picture.

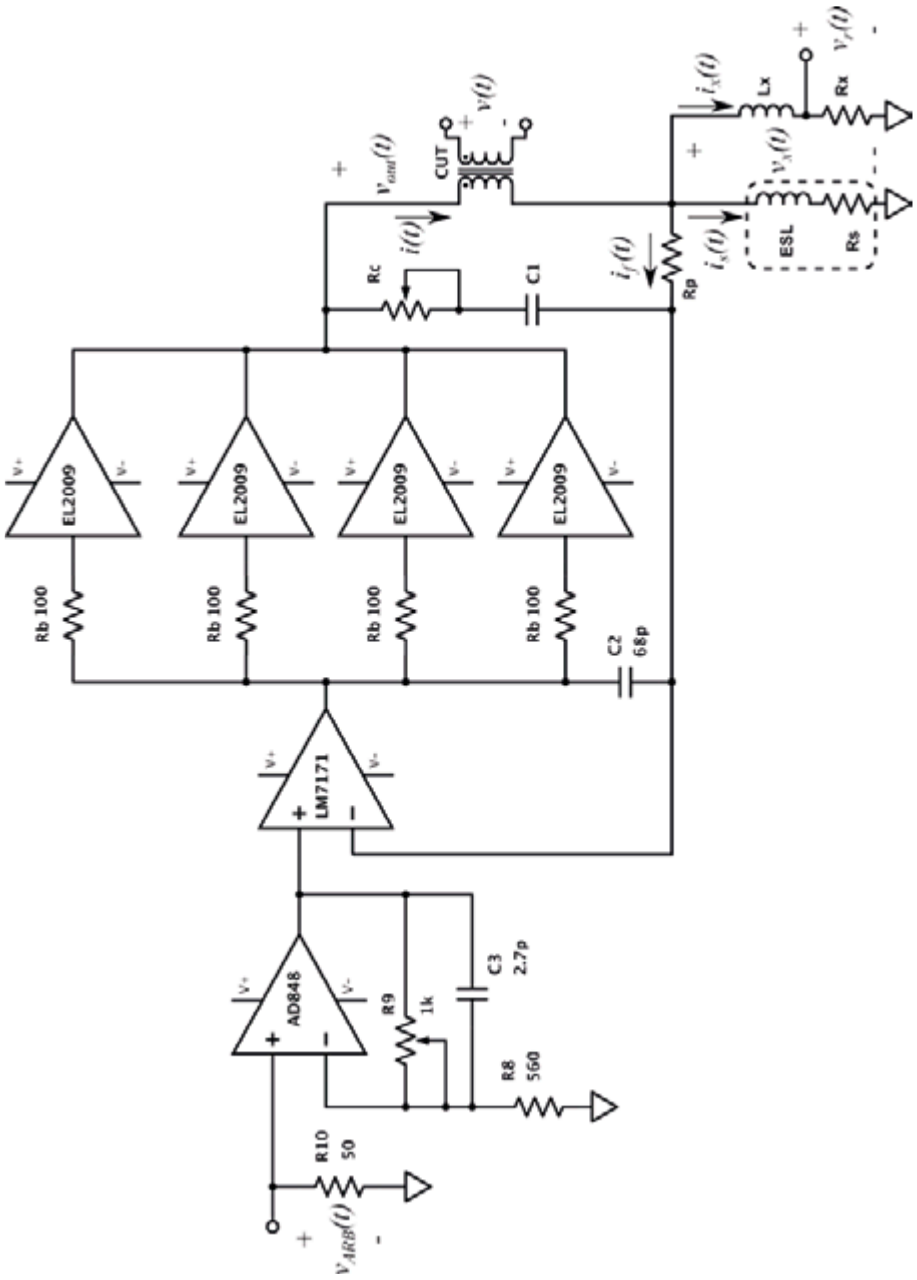

Fig. 5.3. The implemented voltage controlled current source.

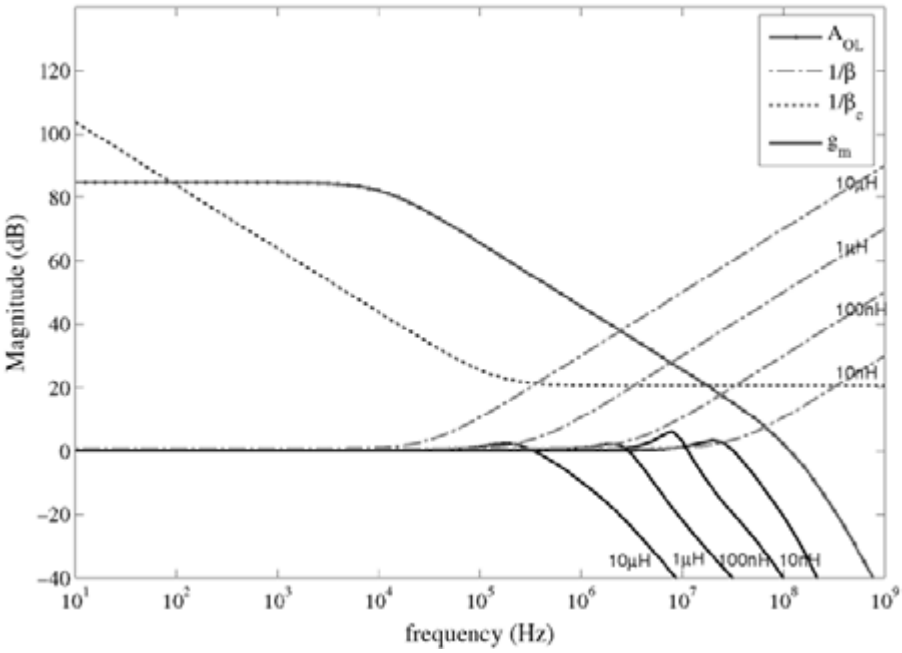

Fig. 5.4. Magnitudes of simulated AC transfer functions of the VCCS for different inductance values of the CUT. A_{OL} is the open loop gain combining LM7171 and EL2009. $1/\beta$ is the reciprocal of the main feedback path transfer function simulated for different values of the CUT. $1/\beta_c$ is the reciprocal of the compensation feedback path transfer function. g_m is the VCCS transconductance transfer function.

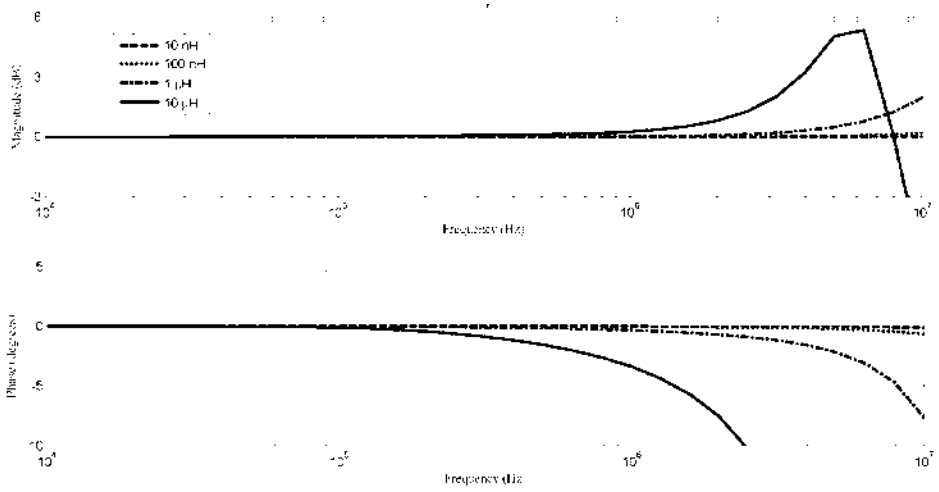

Fig. 5.5. Simulated results of the ratio between CUT current *i(s)* and sensing resistor current $i_s(s)$ for different CUT inductance values.

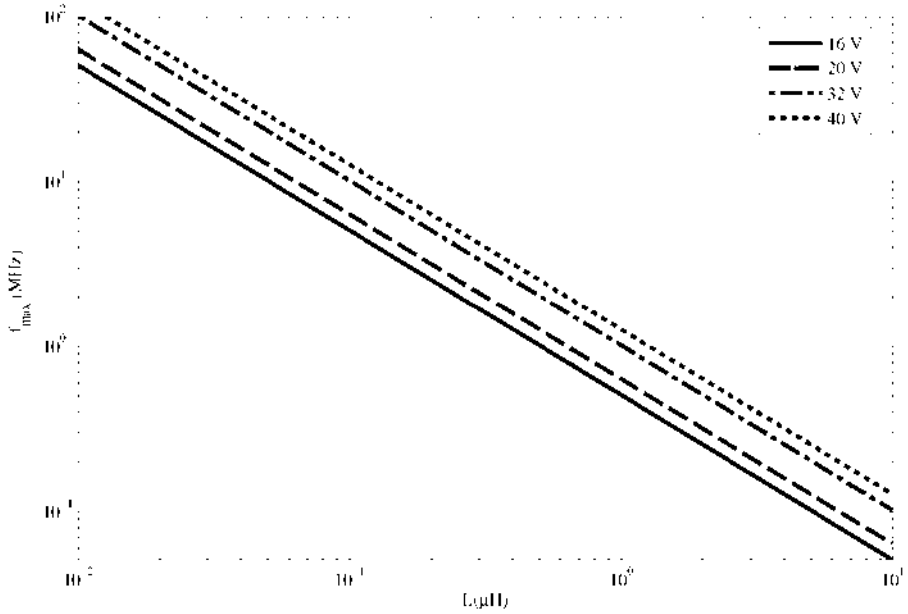

Fig. 5.6. Maximum theoretical limit of full amplitude hysteresis loop frequency as a function of the CUT inductance value. The limit is evaluated for different values of V_{peak} across the CUT.

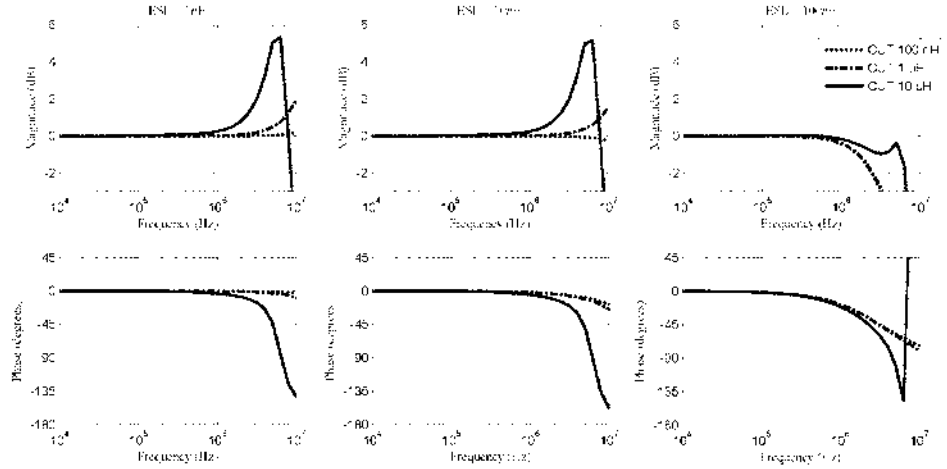

Fig. 5.7. Simulated magnitude and phase of the CUT current *i* over sensing resistor R_s current ratio. The sensing resistor current is estimated through the v_x voltage and considering only the real part R_s of the sensing resistor impedance Z_s. The analysis is shown for different values of the parasitic *ESL* of the sensing resistor proving how this influences the correct estimation of the current *i*.

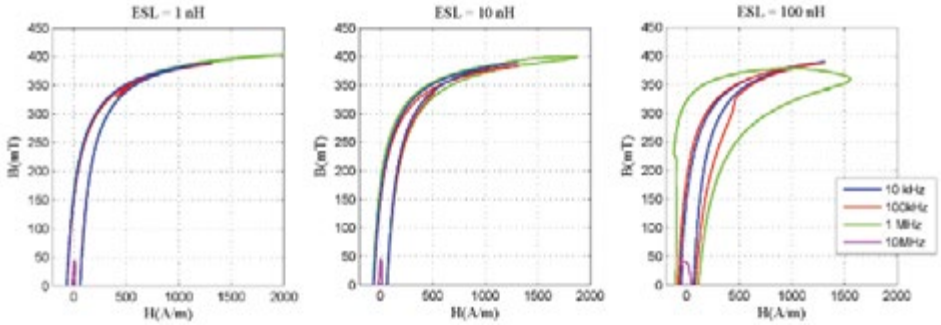

Fig. 5.8. Simulated hysteresis loops at different frequencies and different *ESL* values of the sensing resistor. It is possible to observe how the bigger the *ESL* is, the more significant the loop distortion is.

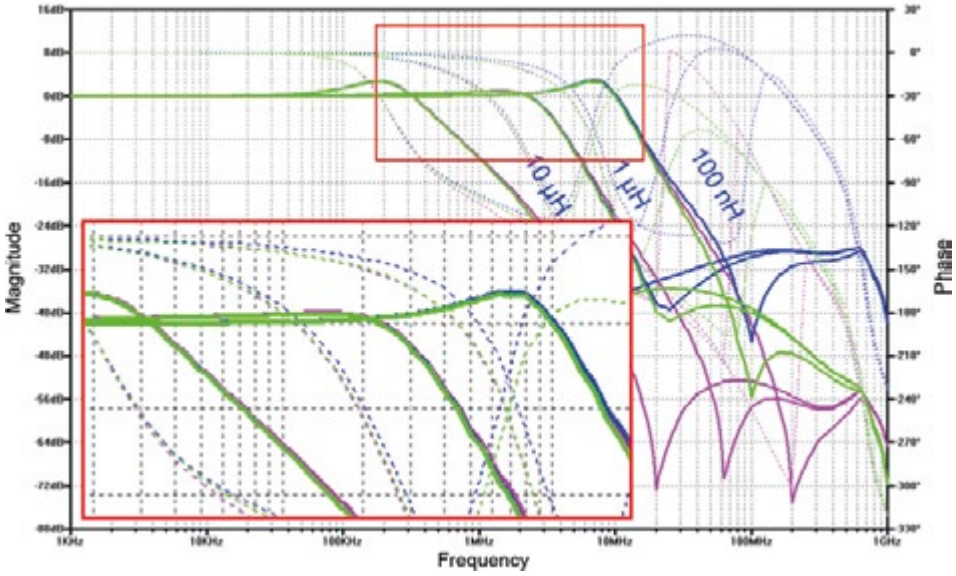

Fig. 5.9. Simulated frequency response comparison of actual CUT current i (magenta), its estimation with v_x/R_s (blue) and its compensated estimation with v_r/R_s (green) for three different CUT values. Solid lines refer to magnitude and dashed lines refer to phase. It is possible to notice how at higher frequencies the compensated estimation is matching i magnitude and phase while the v_x/R_s estimation suffers of a relevant phase error.

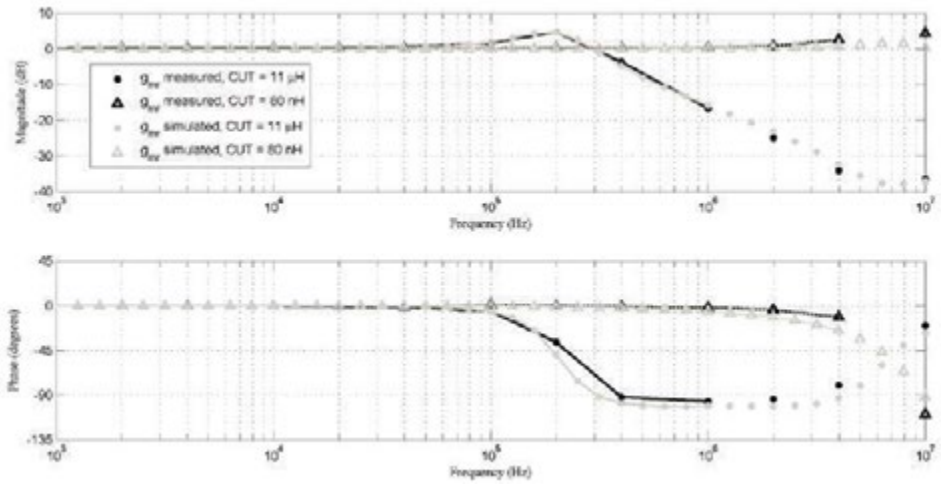

Fig. 5.10. Measured and simulated gmr frequency response obtained with the 11 μH and 80 nH air-core inductors.

Fig. 5.11. Realized test samples.

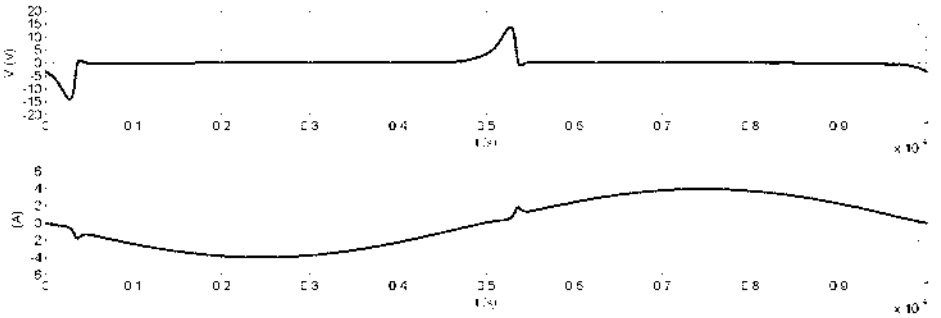

Fig. 5.12. Measured *v(t)* and *i(t)* of sample number 1 (3F45 material) with a sinusoidal excitation at a frequency of *10 kHz*.

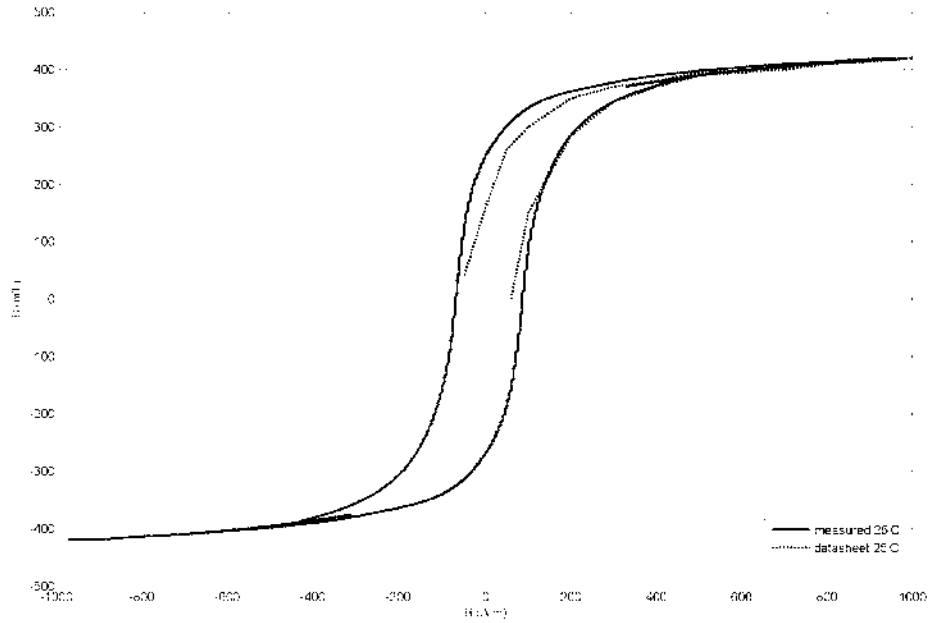

Fig. 5.13. Measured hysteresis loop of sample 1 (3F45 material) with a sinusoidal excitation at a frequency of *10 kHz* compared with material datasheet values.

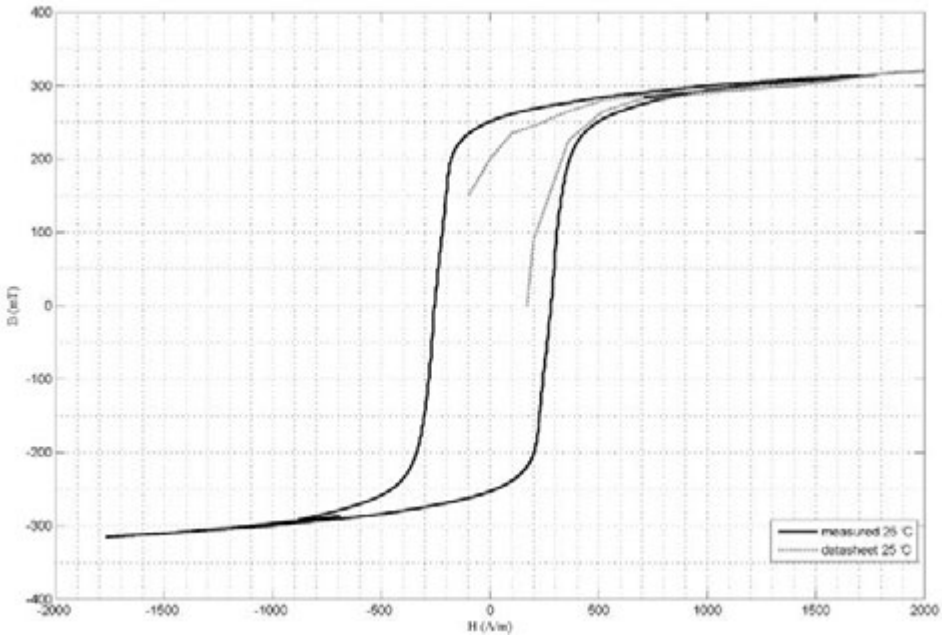

Fig. 5.14. Measured hysteresis loop of sample 2 (4F1 material) with a sinusoidal excitation at a frequency of *10 kHz* compared with material datasheet values.

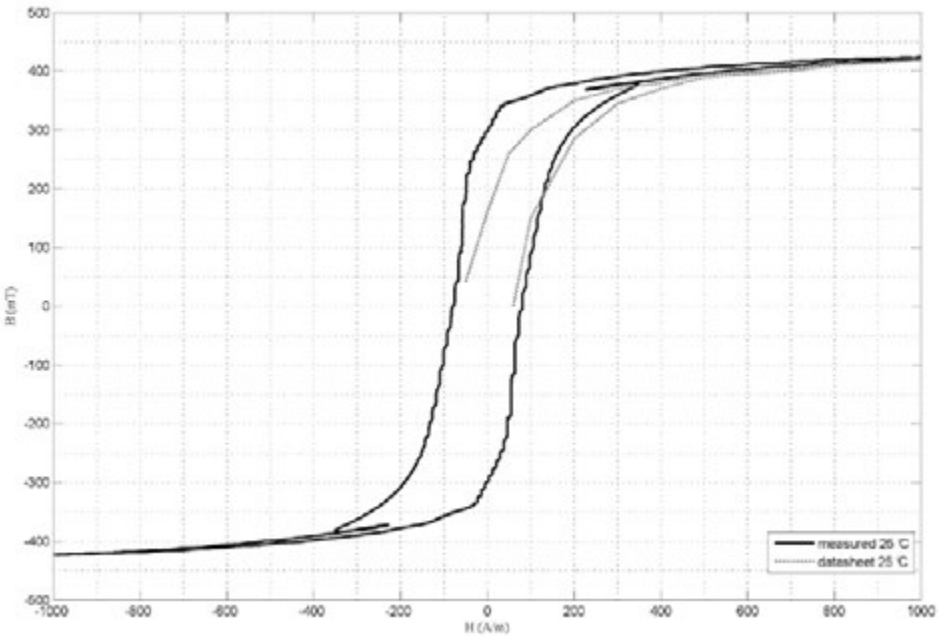

Fig. 5.15. Measured hysteresis loop of sample number 3 (3F45 material) with a sinusoidal excitation at a frequency of *10 kHz* compared with material datasheet values.

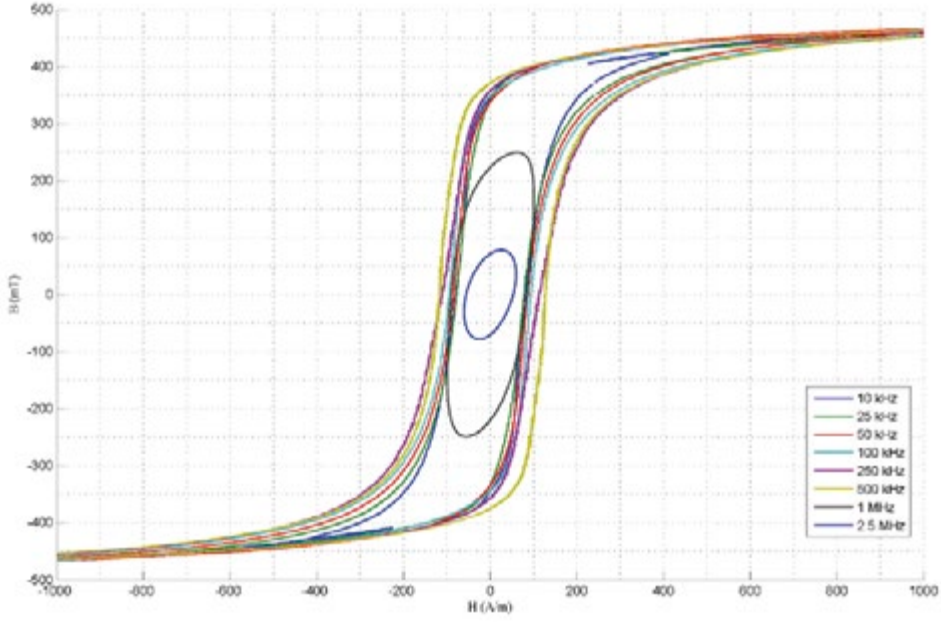

Fig. 5.16. Measured hysteresis loop of sample 3 (3F45 material) with a sinusoidal excitation at different frequencies.

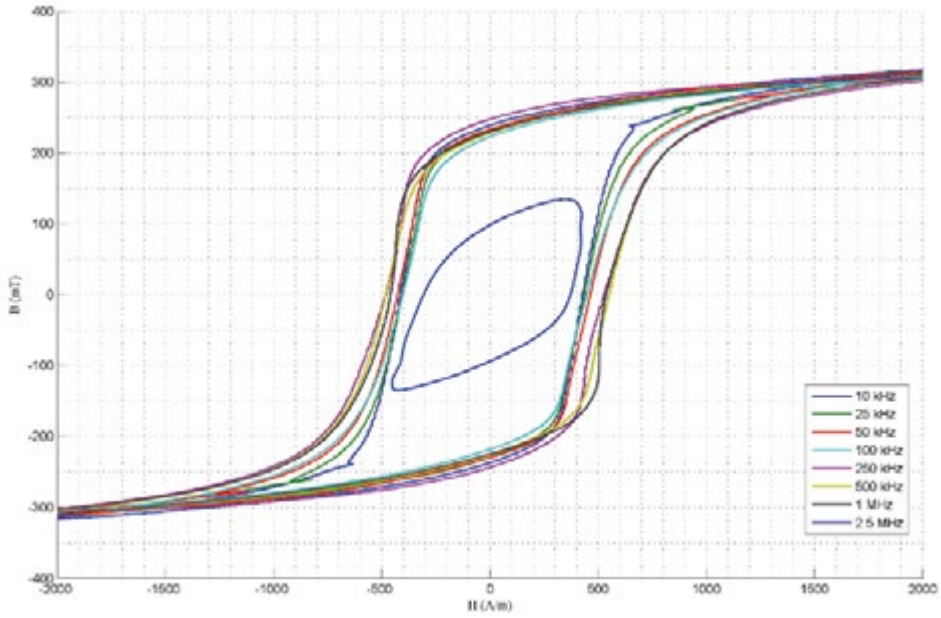

Fig. 5.17. Measured hysteresis loop of sample 4 (4F1 material) with a sinusoidal excitation at different frequencies.

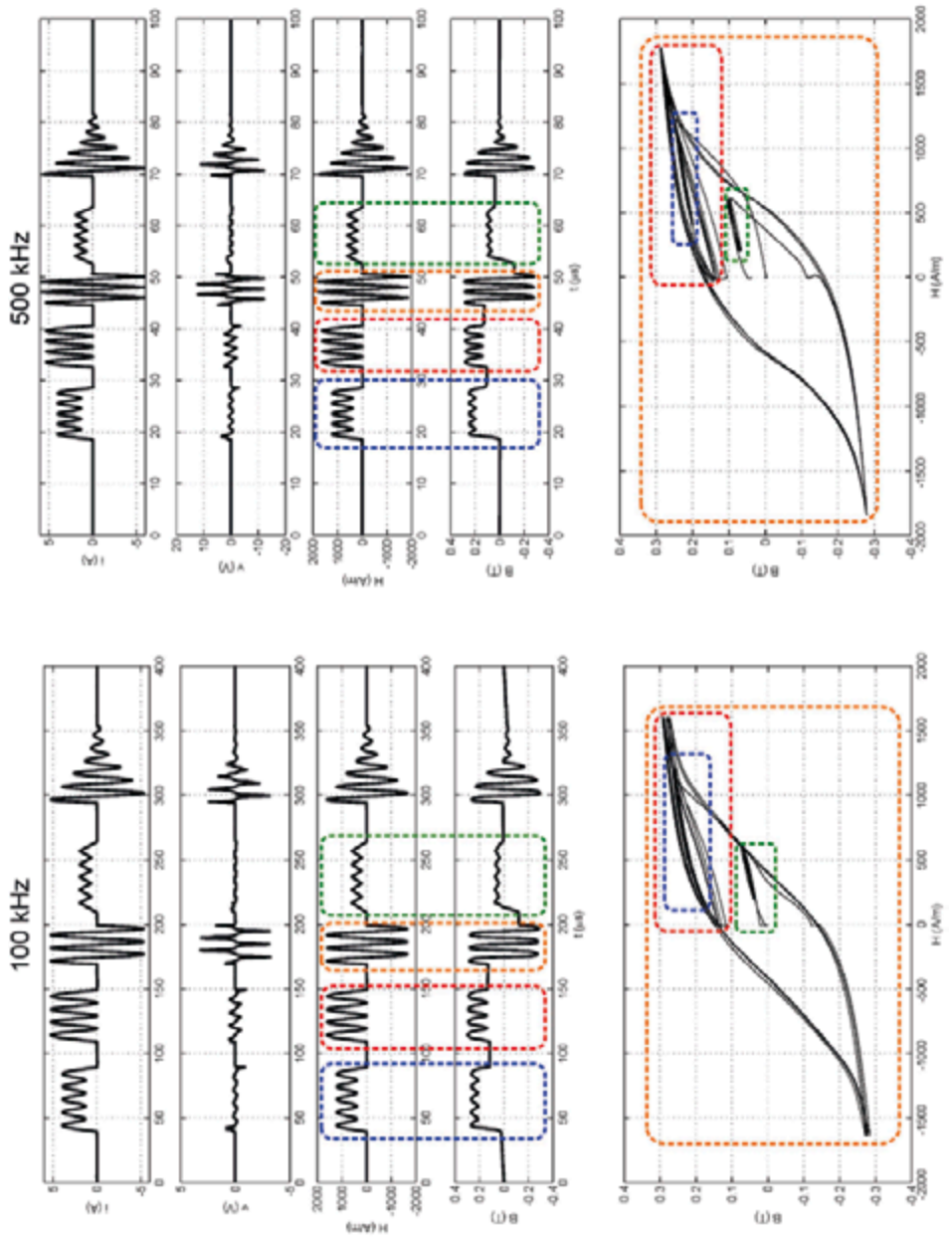

Fig. 5.18. Measured hysteresis loops for a test signal including various current waveform shapes and DC bias values done on sample 5. On top, the measured *v* and *i* are shown, together with the time waveforms of *H* and *B*. The period of the single waveforms is *100 kHz* on left side and *500 kHz* on right side. On the bottom, the B-H loops corresponding to the different waveforms are highlighted.

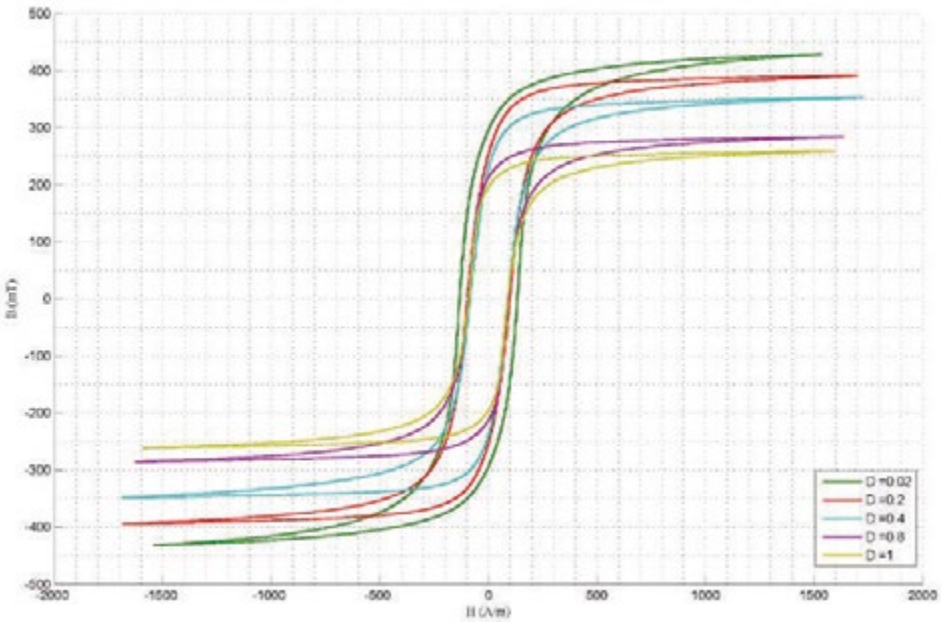

Fig. 5.19. Measured hysteresis loop of sample number 3 (3F45 material) with a *500 kHz* sinusoidal excitation at different values of *D*.

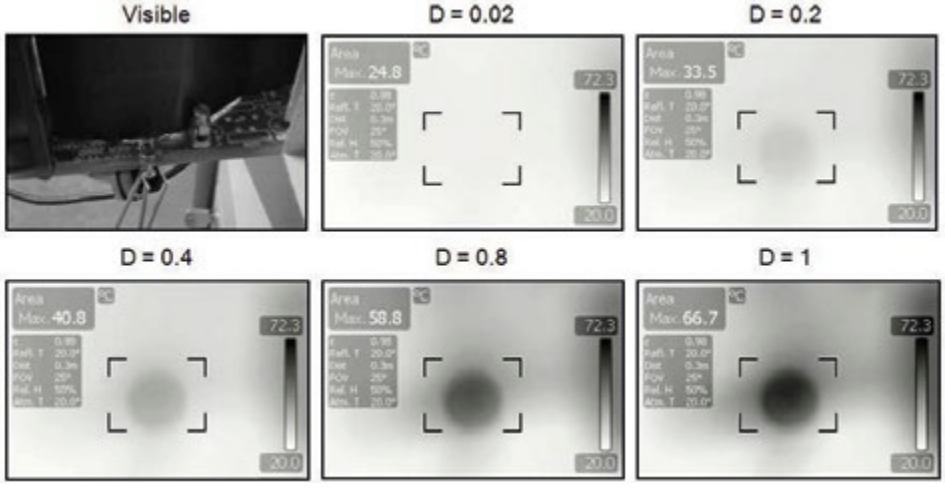

Fig. 5.20. Visible and thermal images of sample number 3 (3F45 material) with a *500 kHz* sinusoidal excitation at different values of *D*. In the centre of the visible image it is possible to see the CUT. The black paperboard behind the CUT shields the radiated emission of the sensing resistor to allow a better estimation of the core temperature.

Chapter 6
Conclusions and future work

In this thesis, many different aspects concerning the miniaturization of specific power converters topologies and components have been studied and applied to practical design implementation. The main focus has been set on HF converter design aiming at high step-down conversion from input to output voltage for low power DC-DC applications.

The implementation of a four phases integrated high step-down multiphase buck converter working in the HF frequency range has been evaluated. Its comparison with multiphase buck converter has shown main advantages in terms of reduced voltage stress on switches, automatic current balancing among the different phases, reduced inductor voltage swing and consequent duty cycle extension for a same voltage conversion ratio. These advantages are enabling the use of higher switching frequencies with respect to multiphase buck, with benefits in terms of passives size reduction and transient response. For these reasons, the high step-down multiphase buck topology has been used to design an integrated converter operating at $10\ MHz$ with $V_i = [10.8, 16]\ V$, $V_o = [0.6, 2]\ V$ and $I_o \leq 2\ A$. The design, implemented in a $0.7\ \mu m$ Texas Instruments process including CMOS, LDMOS and DEMOS, has involved several novel solutions required for this specific topology which have been enabled by the single die integration. Among them, a gate drive architecture providing gate charge recycling and working without the necessity of any additional internal linear regulator has been introduced. Another interesting solution is a start-up logic capable of safely pre-biasing the flying capacitors required by the topology without stressing the power switches with excessive voltages. A steady-state logic capable of providing two different switching schemes enables the possibility of testing the converter under two different operating conditions. The realized converter has been implemented with various power inductor technologies showing the trade-off which is actually existing between maximum efficiency and maximum power density. The measurements have shown a very good matching with respect to the simulated results. Comparing the converter's achievement of $25.3\ mW/mm^2$ in terms of power density over PCB area with previously available solutions has shown a significant increment.

The designed integrated converter has been tested only with inductors $L \approx 100nH$ which is the minimum required value. In order to understand how to optimize its behaviour as a function of the inductance value, additional tests including inductance values in the range $L = [200, 1000]\ nH$ should be conducted. Moreover, this initial version of the converter has been developed in open loop, so next genera-

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tion of the silicon design should also include a control circuit for output closed loop regulation. This can be obtained without a significant area overhead.

The same considerations, in terms of HF implementation, have been applied to a stackable flyback architecture. The target has been an initial investigation of the potential for increased level of integration of this topology, which would allow its use in mobile and other applications where the high power density and small dimensions are of a key importance. Starting from the review of HF flyback designs available in literature, the study has been focused on the development of an inductor optimization script which could define the required inductance values and switching frequency necessary to transfer a certain amount of power with a single module of this architecture. An additional result of this analysis, is a SPICE test-bench which can be used to verify the optimized results together with circuital models of commercially available power switches. A collection of possible solutions for the implementation of primary side switch using in first instance a discrete component has been outlined showing feasible results.

As future work, these preliminary simulation results could be used to design a micro-transformer with optimized inductance values and a test-bench based on discrete components in order to verify the micro-transformer performances as HF flyback inductor. Consequently, the development of a multi-chip module integrated converter or, further down the road, a single chip implementation, with an on-chip integrated inductors could be envisioned.

The analysis of passive components sizes and limitations has suggested that there is a need to better understand and model the losses associated to magnetic materials used for power inductors. This is especially true in terms of new HF materials which are under development. For this reason, a study of magnetic core losses modeling techniques has been pursued showing great differences between the so-called small signal and large signal modeling techniques. As a result, it has been demonstrated that due to the variability of the possible currents applicable for power conversion in terms of waveform shape and DC bias, a large signal model based on Jiles-Atherton hysteresis model with added frequency dependency behavior seems to be a flexible solution for modeling the magnetic hysteresis and core loss. The comparison of core loss estimations obtained by the model with datasheets' measurements for some commercial ferrite materials has shown reasonable agreement.

However, the model requires a deeper understanding of large signal frequency behaviour and an additional calibration to become a reliable design tool. For this reason a measurement campaign and the extraction of model parameters under various operating conditions should be done for a set of magnetic materials relevant in HF power conversion.

In order to start this characterization, a magnetic hysteresis measurement setup has been implemented. It has the capability of testing magnetic material toroidal samples up to few *MHz* while controlling the current and consequently the magnetic field provided to the sample. The actual system can provide a $10\ A_{pp}$ current in a frequency bandwidth up to *500 kHz* depending on the sample's inductance value. The designed system is based on a power VCCS which can provide arbitrary waveforms (including power conversion typical signals such as triangular, sinusoidal and current signals with significant DC components). Measured results have been ob-

tained for several soft ferrite materials samples varying the frequency, temperature and magnetic field waveform.

As a general conclusion, we can say that the increment of switching frequency allows a significant reduction in size of the DC-DC converters. Silicon processes can still prevail higher bandgap semiconductors in point of load low power converters by exploiting their superior integration capabilities. In fact, these allow to associate on a single die all the required active components. In this sense, novel unconventional topologies find a new space for their development based on the reduced impact of parasitics and thus on an easier management of added complexity than in discrete implementations as this thesis has demonstrated for the high step-down buck design. On the other hand, converters working in this region require magnetic passive components, which are beneficial in terms of EMI behaviour and inductance density, but at the same time act as the bottleneck devices towards PwrSiP and PwrSoC implementations. This is mostly related to a lack of technologically reliable solutions for their miniaturization which can be addressable to the complex multidisciplinary design involved in the development of a component which should be of minimum size and cost while having excellent power and electromagnetic behaviour.

Appendix A
Ripple reduction comparison

Much interest has been shown in literature for multiphase buck architectures. Their benefits include the capability of enhancing the power density and transient response of the standard buck architecture without compromising the overall efficiency. This is in part due to the output current ripple reduction which allows the use of smaller output capacitors and trade-offs on the inductors. Moreover, topologies with coupled inductors seems to allow not only for the output current ripple reduction but also for a reduction of the current ripple per each phase. This means that they could relax the specifications on the switches and on the inductors too. Some performance comparisons have already been done as in [104] following the principle described in [105]. However some specific considerations on the inductance values chosen for the comparison between the different topologies differ depending on the final purpose of the analysis.

In our case we are interested in a comparison on ripple reduction between three different topologies: buck, multiphase interleaved buck and multiphase interleaved buck with coupled inductors. We will maintain constant the total amount of inductance used in the circuit to *2L* and describe the coupling using the coupling ratio *k*.

A.1 Buck

For the buck converter of Fig. A.1 is possible to define the output current ripple as:

State 1: *0* to *DT*

$$di = di_{out} = \frac{V_{in} - V_{out}}{2L}\, DT = \frac{V_{in}}{2L}\,(1-D)DT \tag{A.1}$$

State 2: *DT* to *T*

$$di = di_{out} = \frac{-V_{out}}{2L}\,(1-D)T = -\frac{V_{in}}{2L}\,(1-D)DT \tag{A.2}$$

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A.2 Multiphase interleaved buck

In this case the total amount of inductance *2L* is split half per each phase as shown in Fig. A.2 together with the timing of the switches.

The evaluation of ripples on phases and output is divided in two cases.

Case 1: $D \leq 50\%$

When $D \leq 50\%$ there are four different time intervals which identify four different states.

State 1: *0* to *DT*

$$di_1 = \frac{V_{in}}{L}(1-D)DT \tag{A.3}$$

$$di_2 = \frac{V_{in}}{L}(-D)DT \tag{A.4}$$

$$di_{out} = \frac{V_{in}}{L}(1-2D)DT \tag{A.5}$$

State 2: *DT* to *T/2*

$$di_1 = di_2 = -\frac{V_{in}}{L}\left(\frac{1}{2}-D\right)DT \tag{A.6}$$

$$di_{out} = -\frac{V_{in}}{L}(1-2D)DT \tag{A.7}$$

State 3: *T/2* to *T/2 + DT*

$$di_1 = \frac{V_{in}}{L}(-D)DT \tag{A.8}$$

$$di_2 = \frac{V_{in}}{L}(1-D)DT \tag{A.9}$$

$$di_{out} = \frac{V_{in}}{L}(1-2D)DT \tag{A.10}$$

State 4: *T/2 + DT* to *T*

$$di_1 = di_2 = -\frac{V_{in}}{L}\left(\frac{1}{2}-D\right)DT \tag{A.11}$$

$$di_{out} = -\frac{V_{in}}{L}(1-2D)DT \tag{A.12}$$

Combining eq. A.1 with eq. A.5 is possible to define an output ripple reduction factor *δ(D)* between the buck and the multiphase topology.

$$\delta(D)|_{D\leq 0.5} = \frac{di_{out}|_{multip\ hase}}{di_{out}|_{buck}} = \frac{\frac{1-2D}{1-D}}{2} = 2\frac{1-2D}{1-D} \tag{A.13}$$

Case 2: *D > 50%*

When the duty exceeds *0.5* some different considerations need to be done on the inductors connections and time intervals. As before, this leads to four states.

State 1: 0 to T/2 – (T – DT) = (D – ½)T

$$di_1 = di_2 = \frac{V_{in}}{L}(1-D)\left(D-\frac{1}{2}\right)T \tag{A.14}$$

$$di_{out} = \frac{V_{in}}{L}(1-D)(2D-1)T \tag{A.15}$$

State 2: *(D – ½)T* to *T/2*

$$di_1 = \frac{V_{in}}{L}(1-D)(1-D)T \tag{A.16}$$

$$di_2 = -\frac{V_{in}}{L}D(1-D)T \tag{A.17}$$

$$di_{out} = -\frac{V_{in}}{L}(1-D)(2D-1)T \tag{A.18}$$

State 3: *T/2* to *DT*

$$di_1 = \frac{V_{in}}{L}(1-D)\left(D-\frac{1}{2}\right)T \tag{A.19}$$

$$di_2 = \frac{V_{in}}{L}(1-D)\left(D-\frac{1}{2}\right)T \tag{A.20}$$

$$di_{out} = \frac{V_{in}}{L}(1-D)(2D-1)T \tag{A.21}$$

State 4: DT to T

$$di_1 = -\frac{V_{in}}{L}\, D(1-D)T \tag{A.22}$$

$$di_2 = \frac{V_{in}}{L}\, (1-D)(1-D)T \tag{A.23}$$

$$di_{out} = -\frac{V_{in}}{L}\, (1-D)(2D-1)T \tag{A.24}$$

In this case combining eq. A.1 with eq. A.15 the $\delta(D)$ is:

$$\delta(D)|_{D>0.5} = \frac{di_{out}\,|_{multip\ hase}}{di_{out}\,|_{buck}} = \frac{\frac{(1-D)(1-2D)}{(1-D)D}}{2} = 2\frac{1-2D}{D} \tag{A.25}$$

The complessive result is shown in Fig. A.3 where is possible to notice how a theoretical ripple cancellation can be obtained with $D = 50\ \%$. While maintaining the total amount of used inductance to $2L$ is also important to see that there is an effective ripple reduction only in a certain range within the 0.5 duty. Another peculiarity is that the output ripple has a doubled frequency with respect to the phases. This can be seen from the fact that state 1, 3 and state 2, 4 have the same increments.

A.3 Multiphase interleaved buck with coupled inductances:

When coupling the inductors the circuit changes as shown in Fig. A.4 where k is the coupling factor between the two inductances.

The analysis done in [104] describes the coupled inductors as shown in Fig. A.5. The equations of the current ripples in phases and output are obtained for $D \leq 50\%$ and as a function of L_K and L_M the leakage and magnetizing inductance respectively.

From [106] is possible to obtain that for a generic transformer the coupling factor is:

$$k = \sqrt{1 - \frac{L_s}{L_1}} \tag{A.26}$$

where L_s is the inductance measured at port 1 with port 2 shorted while L_1 is the inductance measured at 1 with 2 open. In our case we can obtain a definition of the coupling factor in terms of L_K and L_M by "measuring" it as in Fig. A.6. We will assume equal leakage inductances L_K on both phases.

We have:

$$L_1 = L_K + L_M \tag{A.27}$$

$$L_S = L_K + \frac{L_K L_M}{L_K + L_M} \tag{A.28}$$

Thus:

$$k = \sqrt{1 - \frac{L_s}{L_1}} = \frac{L_M}{L_K + L_M} \tag{A.29}$$

Using the equations from [104] is just a matter of substituting:

$$L_M = kL \tag{A.30}$$

$$L_K = (1 - k)L \tag{A.31}$$

The comparison on ripple reduction can be easily done by referring state by state with the uncoupled solution. We will introduce the notation $di_x' = di_x \cdot c$ where di_x' is the current ripple magnitude in the coupled case (being *x = 1, 2, out*), di_x is the uncoupled case one (from equations A.3 to A.12) and *c* describes the reduction factor.

Case 1: $D \leq 50\%$

State 1: *0* to *DT*

$$di_1' = di_1 \cdot \alpha \tag{A.32}$$

$$di_2' = di_2 \cdot \beta \tag{A.33}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.34}$$

State 2: *DT* to *T/2*

$$di_1' = di_2' = di_1 \cdot \gamma \tag{A.35}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.36}$$

State 3: *T/2* to *T/2 + DT*

$$di_1' = di_1 \cdot \beta \tag{A.37}$$

$$di_2' = di_2 \cdot \alpha \tag{A.38}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.39}$$

State 4: *T/2 + DT* to *T*

$$di_1' = di_2' = di_1 \cdot \gamma \tag{A.40}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.41}$$

Where:

$$\alpha(k, D) = \frac{\frac{1}{1+k} - D}{(1-k)(1-D)} \tag{A.42}$$

$$\beta(k, D) = \frac{\frac{k}{1+k} - D}{(1-k)(-D)} \tag{A.43}$$

$$\gamma(k) = \frac{1}{1-k} \tag{A.44}$$

Case 2: *D > 50%*

Similar considerations work also for *D > 50 %*. The comparison is still done with the same ripples of the states of the uncoupled case.

State 1: *0* to *T/2 – (T – DT) = (D – ½)T*

$$di_1' = di_2' = di_1 \cdot \gamma \tag{A.45}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.46}$$

State 2: *(D – ½)T* to *T/2*

$$di_1' = di_1 \cdot \alpha \tag{A.47}$$

$$di_2' = di_2 \cdot \beta \tag{A.48}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.49}$$

State 3: *T/2* to *DT*

$$di_1' = di_2' = di_1 \cdot \gamma \tag{A.50}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.51}$$

State 4: *DT* to *T*

$$di_1' = di_1 \cdot \beta \tag{A.52}$$

$$di_2' = di_2 \cdot \alpha \tag{A.53}$$

$$di_{out}' = di_{out} \cdot \gamma \tag{A.54}$$

In both cases the reduction factors α, β and γ play the principal role. Figures A.7, A.8 and A.9 show the three parameters.

A.4 Comparison

Is possible to notice that, in any case and state, the output ripple depends only on γ thus it can only increase once the two inductors are coupled. However is important to notice how the current ripple on the two phases changes when the coupling is introduced. For this reason is useful to check α and β to search for a reduction in the ripples amplitude. For doing so we may first rewrite the steady state current ripple balance for the two phases and the output for both $D \leq 50\%$ and $D>50\%$ for both coupled and uncoupled case.

Case 1: *D ≤ 50%*

Multiphase uncoupled:

$$di_{1\_tot} = \frac{V_{in}}{L} DT \left((1-D) - \left(\frac{1}{2} - D\right) + (-D) - \left(\frac{1}{2} - D\right)\right) = 0 \quad \text{(A.55)}$$

$$di_{2\_tot} = \frac{V_{in}}{L} DT \left((-D) - \left(\frac{1}{2} - D\right) + (1-D) - \left(\frac{1}{2} - D\right)\right) = 0 \quad \text{(A.56)}$$

$$di_{out\_tot} = \frac{V_{in}}{L} DT \left((1-2D) - (1-2D) + (1-2D) - (1-2D)\right) = 0 \quad \text{(A.57)}$$

Multiphase coupled:

$$di_{1\_tot}{}' = \frac{V_{in}}{(1-k)L} DT \left(\left(\frac{1}{1+k} - D\right) - \left(\frac{1}{2} - D\right) + \left(\frac{k}{1+k} - D\right) - \left(\frac{1}{2} - D\right)\right) = 0 \quad \text{(A.58)}$$

$$di_{2\_tot}{}' = \frac{V_{in}}{(1-k)L} DT \left(\left(\frac{k}{1+k} - D\right) - \left(\frac{1}{2} - D\right) + \left(\frac{1}{1+k} - D\right) - \left(\frac{1}{2} - D\right)\right) = 0 \quad \text{(A.59)}$$

$$di_{out\_tot}{}' = \frac{V_{in}}{(1-k)L} DT \left((1-2D) - (1-2D) + (1-2D) - (1-2D)\right) = 0 \quad \text{(A.60)}$$

Once again is possible to notice how the output ripple is always increasing as $k > 0$. To obtain an easier comparison between the ripples in each phase in coupled and uncoupled case we can rewrite for a single phase (the other is going to be affected in the same way) as:

$$di'_{1_{tot}} = \frac{V_{in}}{L} DT(a + b - 2c) = 0 \quad \text{(A.61)}$$

Where:

$$a = \frac{\frac{1}{1+k} - D}{1-k} \quad \text{(A.62)}$$

$$b = \frac{\frac{k}{1+k} - D}{1-k} \quad \text{(A.63)}$$

$$c = \frac{\frac{1}{2} - D}{1-k} \quad \text{(A.64)}$$

These can be plotted with the respective term of the uncoupled case as shown in Figures A.10, A.11 and A.12.

From the graphs is possible to see that c is always increasing with respect to the uncoupled case. We can also say that for every k:

$$D \leq 50\,\% \Rightarrow \; a > 0.25, \qquad c > 0 \tag{A.65}$$

From equation A.61 we can easily notice that:

$$\frac{a+b}{2} = c \tag{A.66}$$

which means that the maximum ripple depends on b. This can be seen in figure A.13 together with the different ripples "shapes".

Minimization occurs when $a = b = c$ but this case is practically unreachable as it can be verified only for $k = 1$. For the other cases, as c is always bigger than the uncoupled case, the current ripple on each phase is increased than in the uncoupled case. For the case $D > 50\,\%$ is possible to provide a similar analysis.

A.5 Conclusion

In literature, as can be seen in [104, 105, 107], the comparison is usually done between an uncoupled case in which the inductance per phase is L_K and a coupled case in which the L_K is just the leakage part of a bigger total inductance. The increment in total inductance, provided by the addition of the coupling, provides the reduction in the current ripple per each phase with respect to the uncoupled case. At the same time there is a preservation of the transient response of the system with respect to the uncoupled case. In fact this is ultimately depending only on the part $L_K = (1 - k)L$ of the total inductance of the coupled case (as explained in [107]).

In our analysis, we have done a comparison maintaining a fixed total amount of inductance for both the uncoupled and coupled case. In this way it is not possible to obtain a reduced ripple per each phase while maintaining the same transient response. In fact, the ripples in the phases increase when the coupling k grows. However, as k grows is possible to allow the increment in the output ripple while improving the transient response of the system which benefits of the L_K reduced fraction of the total inductance.

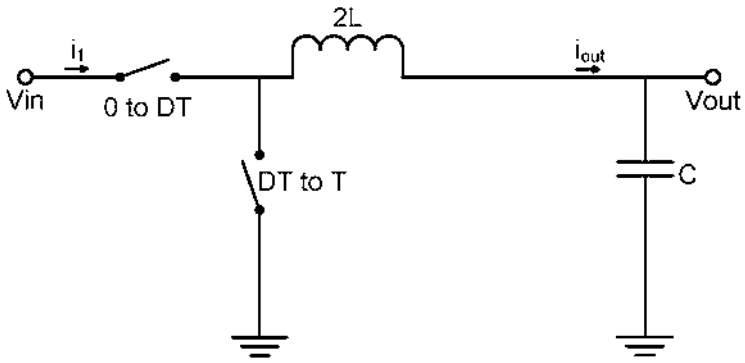

Fig. A.1. Buck.

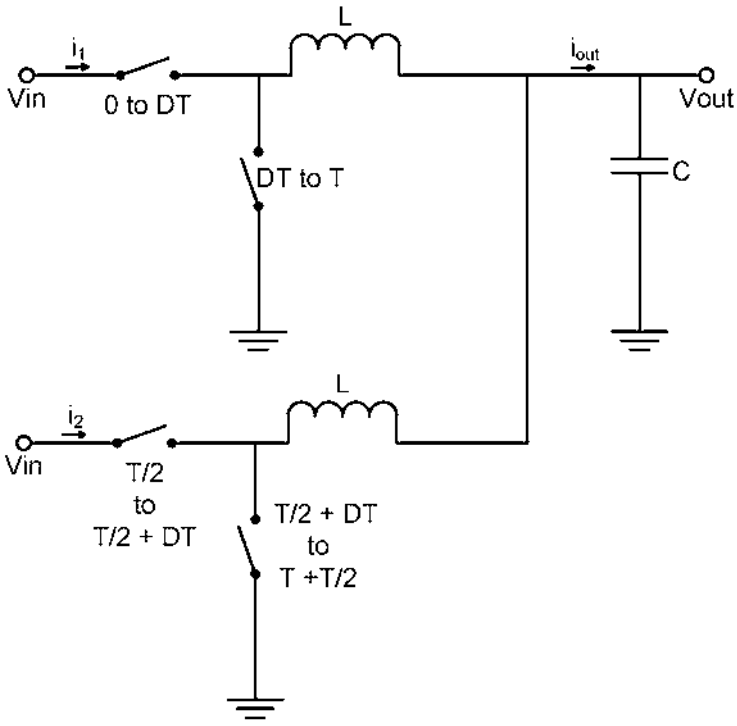

Fig. A.2. Multiphase interleaved buck.

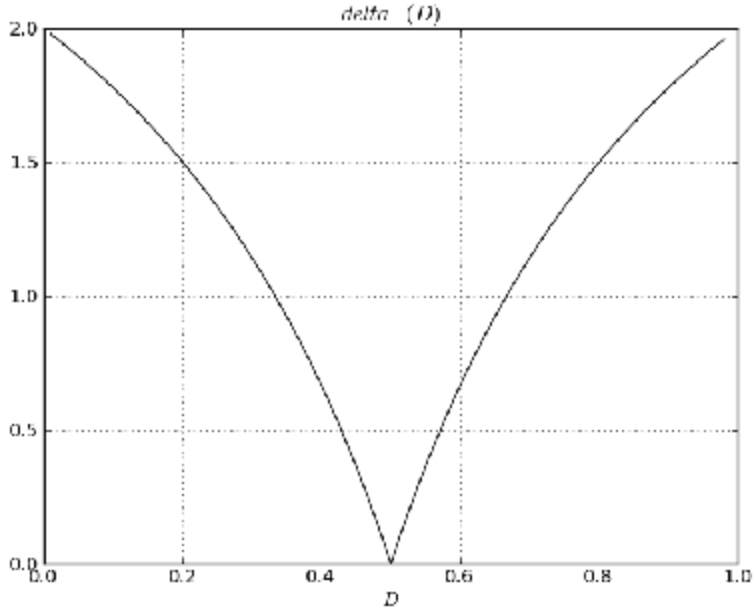

Fig. A.3. Ripple reduction factor *δ(D)* between buck and multiphase.

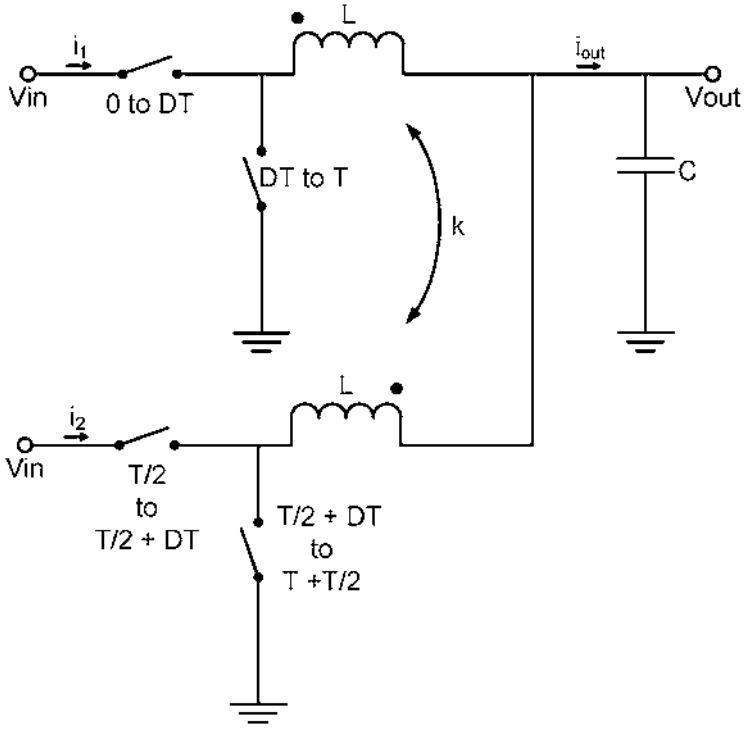

Fig. A.4. Multiphase interleaved buck with coupled inductors.

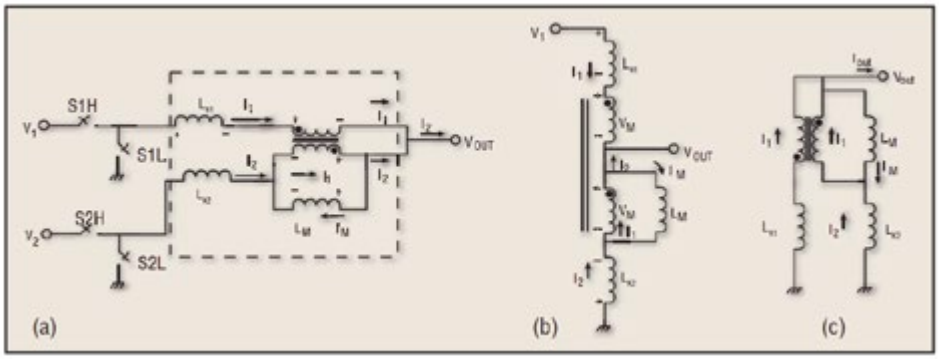

Fig. A.5. Coupled inductors equivalent circuit.

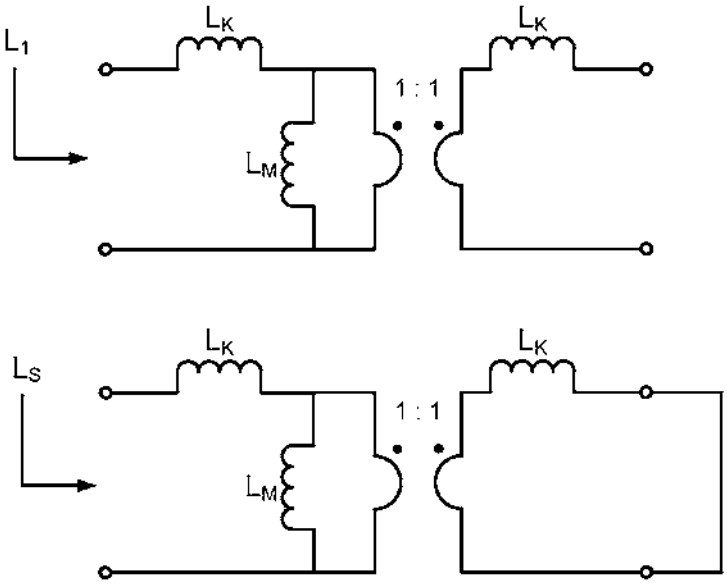

Fig. A.6. Coupling factor measurement.

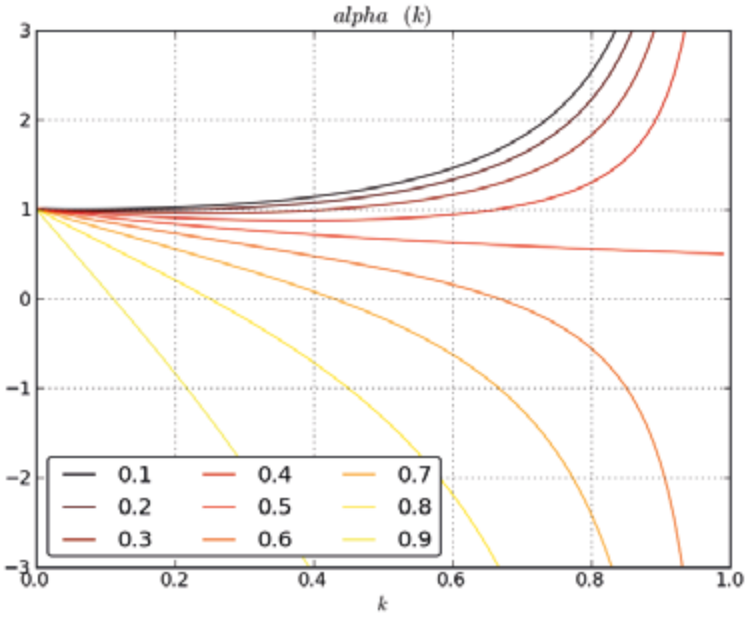

Fig. A.7. *α(k, D)*

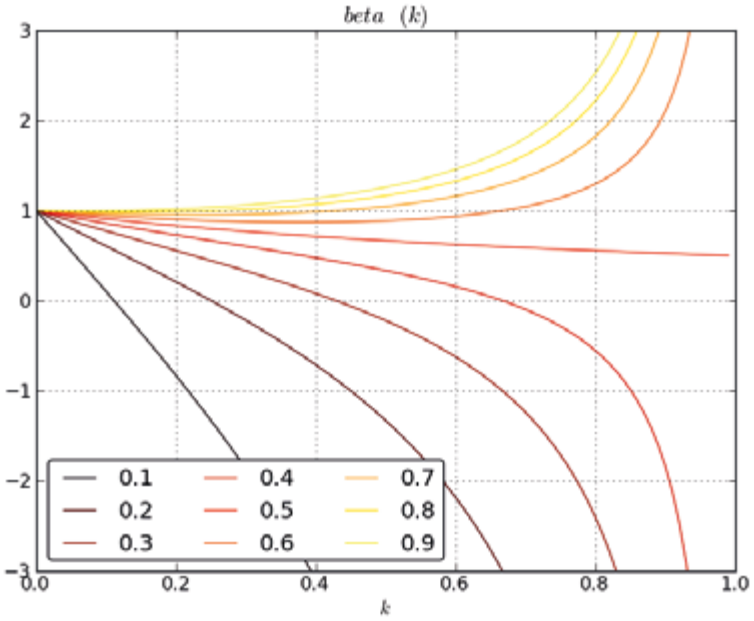

Fig. A.8. *β(k, D)*

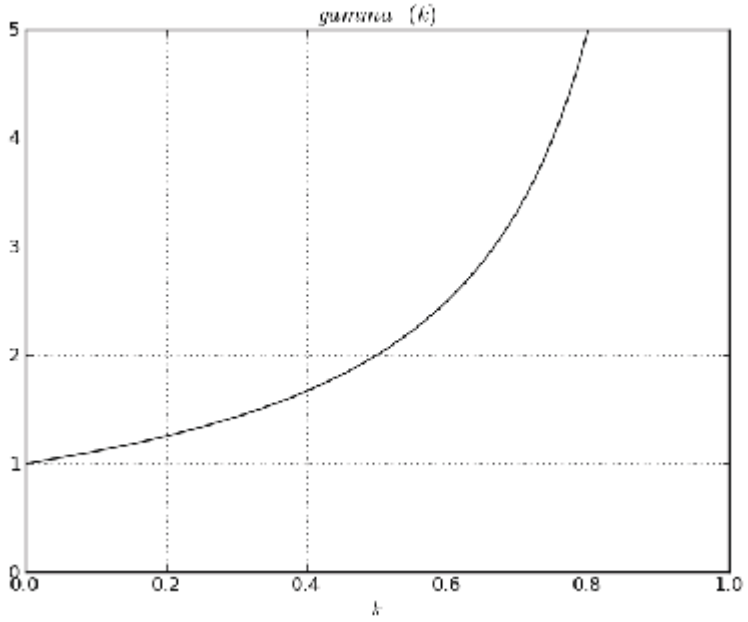

Fig. A.9. *γ(k)*

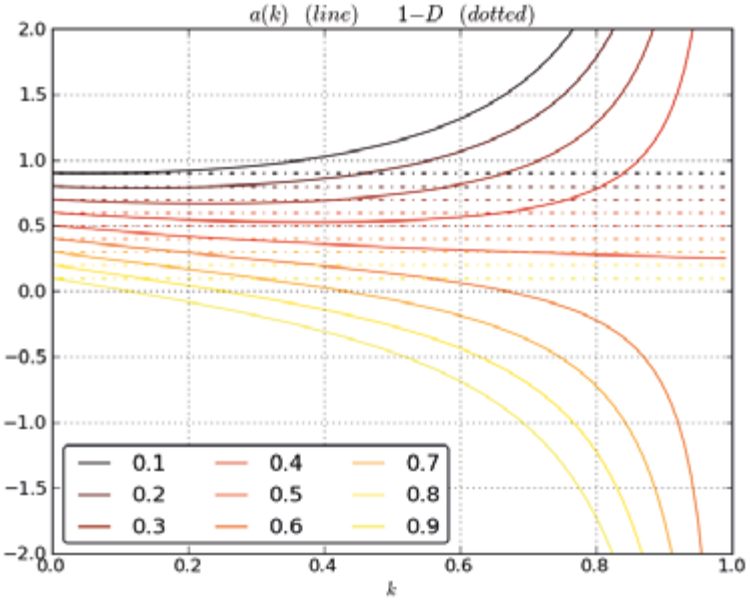

Fig. A.10. *a(k, D)*

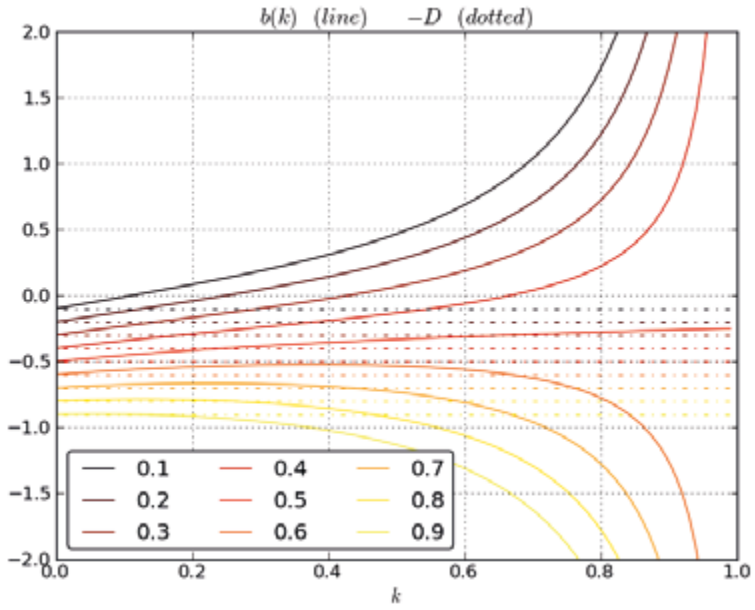

Fig. A.11. *b(k, D)*

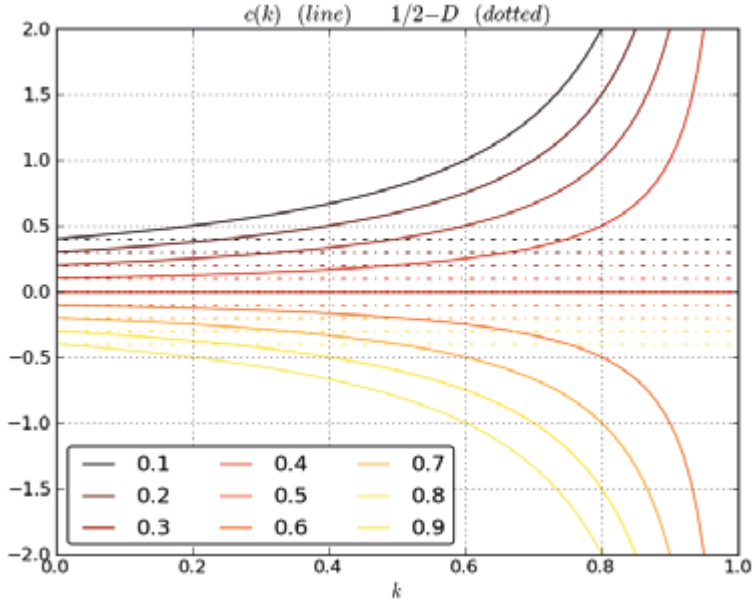

Fig. A.12. *c(k, D)*

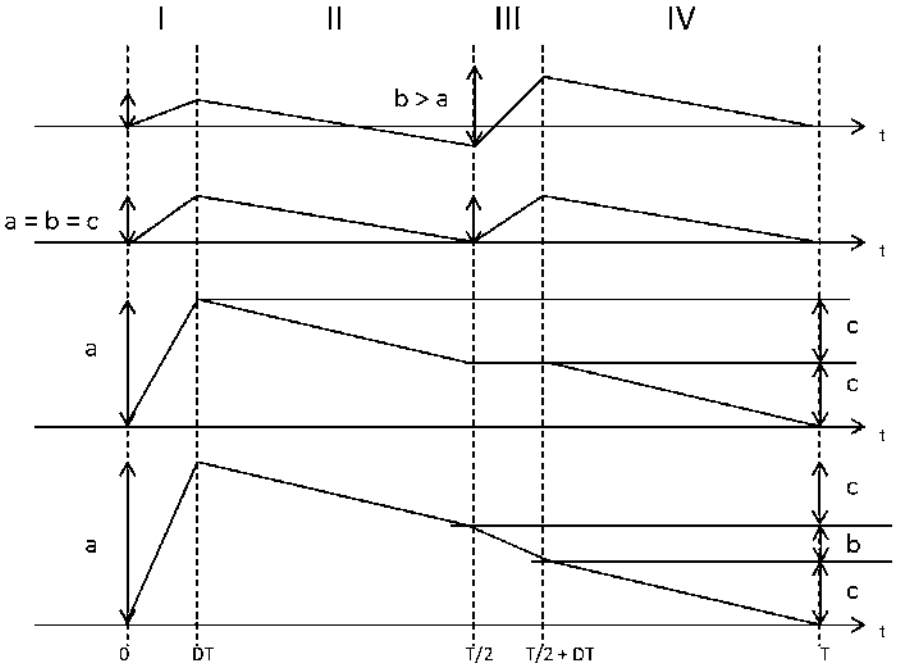

Fig. A.13. Ripple waveforms for a fixed $D < 50\ \%$ as k varies.

Appendix B
Test chip boards schematics

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Fig. B.1. Mother board schematic.

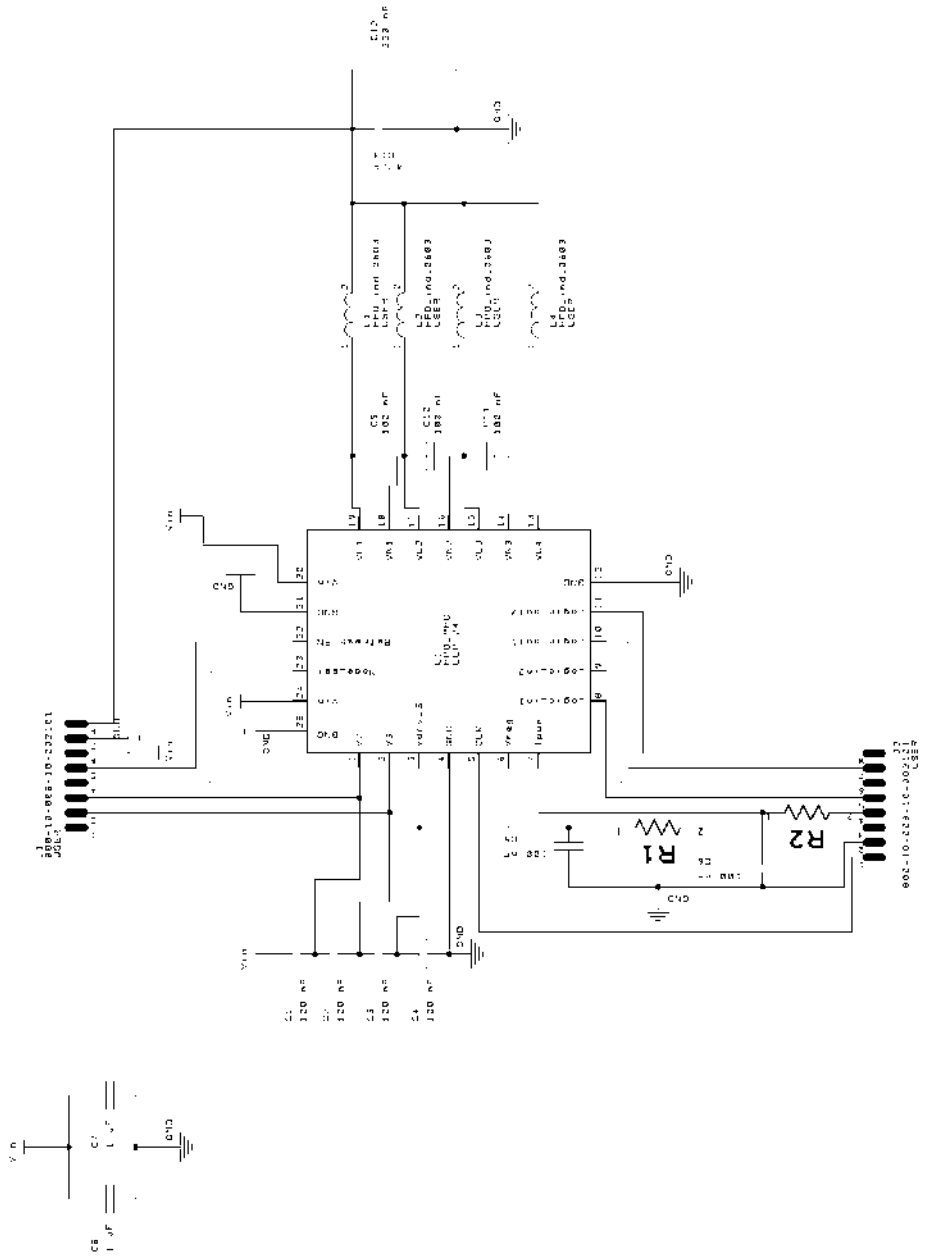

Fig. B.2. Daughter board schematic.

Appendix C
High frequency flyback transformer sizing script

```
%High frequency flyback transformer sizing script
%G.Calabrese, 05 Sep 2014

%Parameter loading
%Inductance range
Lpri_min = 10e-9;
Lpri_max = 200e-9;
steps = 200;
%Minimum on time of primary side switch
ton_min = 3.5e-9;
%Peak current of primary side
Ip = 0.65;
%Switching frequency range
fs_max = 50e6;
%Input voltage values array
Vi_array = [16];%, 5];
%Output voltage
Vo = 1;
%Diode forward voltage
Vd = 0.79;
%Turn ratio n1/n2 (later converted in n2/n1)
n_min = 0.1; %turn ratio n1/n2 min
n_max = 3; %turn ratio n1/n2 max

%Generation of vectors and matrixes
%Primary side inductance vector
Lpri = linspace(Lpri_min, Lpri_max, steps);
%Turn ratio n:1 vector
n = (n_min:0.1:n_max);
%Allocation of space for variables
ton = zeros(1,length(Lpri));
toff = zeros(length(Lpri), length(n));
Pout = zeros(length(Lpri), length(n));
fs = zeros(length(Lpri), length(n));
D = zeros(length(Lpri), length(n));
```

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```
Ipri_rms = zeros(length(Lpri), length(n));
Isec_rms = zeros(length(Lpri), length(n));

%Processing
fig = figure;
temp_legend=[];
%Sweep in Vi
for k = 1:length(Vi_array)
   Vi = Vi_array(k);
   %Sweep in Lpri
   for i = 1:length(Lpri)
      ton(i) = Ip*Lpri(i)/Vi;
      %Exclusion of points outside the constraint
      %on minimum on time of primary side switch
      if ton(i) < ton_min
         ton(i) = NaN;
      end
      %Sweep in n
      for j = 1:length(n)
         toff(i,j) = Lpri(i)*Ip/(n(j)*(Vo + Vd));
         fs_temp = 1/(ton(i)+toff(i,j));  %considering BCM
         %Exclusion of frequency results outside
         %the constraint of maximum frequency
         if not(isnan(fs_temp))
            if fs_temp <= fs_max
               fs (i, j) = fs_temp;
            else
               fs (i, j) = NaN;
            end
         else
            fs (i, j) = fs_temp;
            toff(i,j) = NaN;
         end
         Pout(i, j) = 0.5*Lpri(i)*(Ip^2)* fs(i,j);
         D (i, j) = sqrt(2*Pout(i,j)*Lpri(i)*fs(i,j)/(Vi^2));
         Ipri_rms (i, j) = Ip*sqrt(D(i,j)/3);
         Isec_rms (i, j) = n(j)*Ip*sqrt((1-D(i,j))/3);
      end
   end

%Results display
   h = fig;
   hold on;
   %PLot 1
   subplot(3,2,1);
   [N LPRI] = meshgrid (n, Lpri);
```

```
surfc (N, LPRI*1e9, Pout);
view(-45, 30);
shading flat;
xlabel('n');ylabel('Lpri [nH]');zlabel('Pout [W]');
alpha(0.55);
hold off;
%PLot 2
hold on;
subplot(3,2,2);
[N LPRI] = meshgrid (n, Lpri);
surfc (N, LPRI*1e9, fs/1e6);
view(-45, 30);
shading flat;
xlabel('n');ylabel('Lpri [nH]');zlabel('f_{s} [MHz]');
alpha(0.55);
hold off;
%PLot 3
hold on;
subplot(3,2,3);
[N LPRI] = meshgrid (n, Lpri);
surfc (N, LPRI*1e9, Ipri_rms*1000);
view(-45, 30);
shading flat;
xlabel('n');ylabel('Lpri [nH]');zlabel('Ipri_{rms} [mA]');
alpha(0.55);
hold off;
%PLot 4
hold on;
subplot(3,2,4);
[N LPRI] = meshgrid (n, Lpri);
surfc (N, LPRI*1e9, Isec_rms*1000);
view(-45, 30);
shading flat;
xlabel('n');ylabel('Lpri [nH]');zlabel('Isec_{rms} [mA]');
alpha(0.55);
hold off;
%PLot 5
hold on;
subplot(3,2,5);
[N LPRI] = meshgrid (n, Lpri);
surfc (N, LPRI*1e9, D*100);
view(-45, 30);
shading flat;
xlabel('n');ylabel('Lpri [nH]');zlabel('D [%]');
alpha(0.55);
hold off;
```

```
    end

    %Constraints display
    uistr(1) = {strcat('Constraints:')};
    uistr(2) = {strcat('Ipeak = ',num2str(Ip*1000), ' [mA]')};
    uistr(3) = {strcat('ton_min = ',num2str(ton_min*1e9), ' [ns]')};
    uistr(4) = {strcat('fs_max = ',num2str(fs_max/1e6), ' [MHz]')};
    uistr(5) = {strcat('V_o = ',num2str(Vo), ' [V]')};
    uistr(6) = {strcat('V_i = ',num2str(Vi_array), ' [V]')};
    uicontrol('Style','text','Position',[750 100 100 85],...
            'String',uistr);
```

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